Effect of temperature on heavy ion-induced single event transient on 16-nm FinFET inverter chains

Li Cai(蔡莉)[1,†], Ya-Qing Chi(池雅庆)[3], Bing Ye(叶兵)[1,‡], Yu-Zhu Liu(刘郁竹)[1,2], Ze He(贺泽)[1,2], Hai-Bin Wang(王海滨)[4], Qian Sun(孙乾)[3], Rui-Qi Sun(孙瑞琪)[3], Shuai Gao(高帅)[1,2], Pei-Pei Hu(胡培培)[1], Xiao-Yu Yan(闫晓宇)[1,2], Zong-Zhen Li(李宗臻)[1], and Jie Liu(刘杰)[1,§]

[1] *Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou* 730000, *China*
[2] *University of Chinese Academy of Sciences, Beijing* 100049, *China*
[3] *College of Computer Science, National University of Defense Technology, Changsha* 410073, *China*
[4] *College of IoT Engineering, Hohai University, Changzhou* 213022, *China*

(Received 4 July 2022; revised manuscript received 19 August 2022; accepted manuscript online 2 September 2022)

The variations of single event transient (SET) pulse width of high-LET heavy ion irradiation in 16-nm-thick bulk silicon fin field-effect transistor (FinFET) inverter chains with different driven strengths are measured at different temperatures. Three-dimensional (3D) technology computer-aided design simulations are carried out to study the SET pulse width and saturation current varying with temperature. Experimental and simulation results indicate that the increase in temperature will enhance the parasitic bipolar effect of bulk FinFET technology, resulting in the increase of SET pulse width. On the other hand, the increase of inverter driven strength will change the layout topology, which has a complex influence on the SET temperature effects of FinFET inverter chains. The experimental and simulation results show that the device with the strongest driven strength has the least dependence on temperature.

Keywords: heavy ion, single event effect, single event transient, FinFET, inverter chain

PACS: 61.82.Fk, 61.80.Jh, 85.30.De **DOI:** 10.1088/1674-1056/ac8e9c

1. Introduction

As the gate oxide thickness, depletion layer width, and channel length of semiconductor devices continuously shrink, problems such as degradation of subthreshold characteristics caused by the short-channel effect (SCE) are becoming increasingly obvious. Especially as the feature size decreases to nano-scale, the limitations of traditional planar technology are becoming more and more prominent.[1,2] The emergence of the fin field-effect transistor (FinFET) can well suppress the SCE of traditional planar devices and gradually becomes the mainstream device of nano-scale technology.[3] Most of the state-of-the-art devices (14 nm/16 nm in feature size) use FinFET technology.[4,5]

However, the influences of single event effects (SEEs) on integrated circuits (ICs) fabricated with nano-scale FinFET technology are severe due to their reduced critical charge ($Q_{\rm crit}$) and supply voltage.[6–8] The SEE tolerance performance of advanced FinFET devices and ICs have become part of the main factors restricting their applications in radiation environments.[9] Therefore, the characterization and study of the mechanisms of SEEs are crucial for the safety and reliability of advanced FinFET devices used in space, near-earth space, and nuclear radiation environments.

In addition, extreme temperature conditions exist in the space environment. For instance, the average temperature of Titan's surface is only about 90 K,[10] while it is as high as 740 K for Venus.[11] Although the thermal control subsystem can maintain the function of devices in a wide temperature range, these subsystems will increase the weight and reduce the effective load of the satellite.[12] Moreover, even with a thermal control subsystem, some semiconductor devices' working temperature of semiconductor devices is in a ranges from 218 K to 418 K.[13] In such a wide temperature range, the influence of temperature on SEEs must be considered. In recent years, the study has intensely focused on the influence of temperature on SEE in semiconductor devices.[13–20] Moreover, many researches have shown that temperature has a strong influence on SEEs. For example, Farjallah *et al.* evaluated the variation of $Q_{\rm crit}$ with temperature for 65-nm, 45-nm, 32-nm, and 22-nm bulk silicon CMOS technologies in a temperature range from −50 °C to 150 °C. The SPICE simulation results indicated that $Q_{\rm crit}$ decreases significantly as temperature increases for 6T-SRAM and DICE units, the calculated $Q_{\rm crit}$ changes 88.4% and 99.9% respectively.[21] In 2016, Zhang *et al.* characterized the soft error rate (SER) triggered by α particles in 20-nm bulk silicon planar device and 16-nm bulk silicon FinFET technology at different temperatures and power supply voltages. The test results showed that

†Corresponding author. E-mail: caili@impcas.ac.cn
‡Corresponding author. E-mail: yebing@impcas.ac.cn
§Corresponding author. E-mail: j.liu@impcas.ac.cn

© 2023 Chinese Physical Society and IOP Publishing Ltd

in the same temperature range, the SER of 16-nm FinFET did not change significantly with temperature, while the SER of the 20-nm planar device increases about twice at elevated temperature.[22]

Three-dimensional technology computer aided design (3D TCAD) is a commonly used simulation tool with good operability and repeatability, and is useful in providing an insight into the physical mechanisms of SEEs and is widely used in the radiation effect research field.[23–25] Numerous heavy ion irradiation tests and TCAD simulation results have shown that the SET pulse width increases significantly with temperature rising,[26–33] and the number of measured SETs also increases. Cao *et al.* investigated the variation of SEE cross section with temperature and frequency of 7-nm bulk silicon FinFET devices for α particle incidence.[34] Because the SEE cross section of the logic circuit is proportional to the SET pulse width and the frequency, the slope of the SEE cross section increases when the temperature rises to 85 °C, indicating that the SET pulse width increases with temperature rising. However, there is little research on the SET dependence of temperature, with high LET heavy ions irradiating FinFET devices.

In this work, the variation of SET pulse width with temperature for 16-nm bulk silicon FinFET inverter chains is fully characterized by our detailed heavy ion with high LET value irradiation tests. Furthermore, the 3D TCAD simulations were used to investigate the impact of temperature on SET pulse width and saturation current of 16-nm bulk FinFET inverter chain in this paper.

2. Experimental setup

The device under test (DUT) was designed and fabricated in a commercial 16-nm bulk FinFET process, with an IO voltage of 1.8 V and a core voltage of 0.8 V. It was packaged in BGA-32 and the operating current was about 100 mA. The specific information about the DUT is shown in Table 1.

Table 1. Characteristic parameters of inverters in SET test chip.

Inverter	W (nm)/H (nm)	Fins	Drain area (cm^2)
INV1	180/576	4	9.81×10^{-11}
INV2	270/576	8	9.81×10^{-11}
INV4	450/576	16	1.96×10^{-10}

The INV1, INV2, and INV4 inverter chains were designed to have the same threshold voltage but different current driving strengths (different gate sizes) as shown in Fig. 1. The active area of the N-type or P-type FinFET in the INV1 inverter was about 180 nm×109 nm, which is 67% of the INV2 and 40% of the INV4. The drain area of the N-type or P-type FinFET in the INV1 inverter was about 90 nm×109 nm, the same as that in INV2 but half that of the INV4. The densities and distances of the well contact of these inverters were the same to maintain the same well voltage.

Very early, Kaul *et al.*[35] and Buchner and Baze[36] cited the SET pulse-width as a key factor determining the vulnerability of combinational circuitry. Gadlage *et al.*[37] also pointed out that a key factor affecting soft-error rates is the time duration of SET induced by heavy ions. The probability of the transient falling with the setup-and-hold time of the latch, leading to erroneous data storage in the latch, was directly proportional to the transient pulse width.[38] Because of this critical dependence of soft-error rate (SER) on SET pulse width, the experimental study focused on the temperature effect on SET pulse width. Based on the self-triggered SET capture and pulse width measurement technology,[39] each output was connected to a pulse width measurement circuit, the measurement range was increased by up to 3.12 ns, and the pulse width resolution was 26 ps.

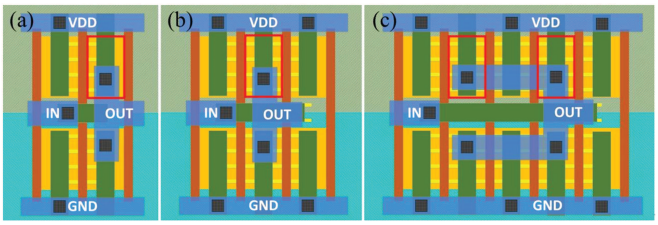


Fig. 1. FinFET inverters with different driving strengths. (a) INV1, (b) INV2, and (c) INV4.

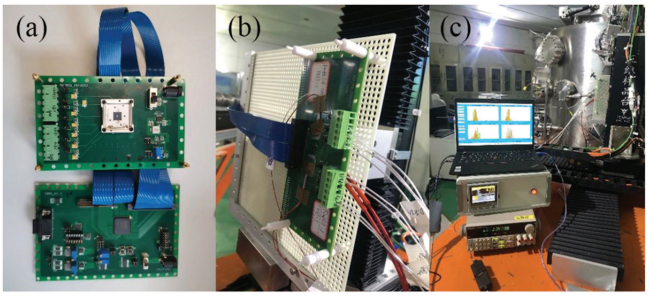


Fig. 2. Photos of heavy ion irradiation experiment: (a) DUT, (b) sample holder and DUT, (c) SET test system and temperature measurement and control system.

The heavy ion irradiation test was carried out on the SEE facility of the Heavy Ion Research Facility in Lanzhou (HIRFL). The ion used in the test was Xe with the initial energy of 19.5 MeV/u. The residual energy of the Xe ion was 1870.3 MeV when it reached the surface of DUT after passing through a scintillator detector with a thickness of 12.5 μm, a titanium window with a thickness of 14.7 μm, and 50-mm thick air. The DUT is in flip-chip packing. After Si substrate thinning, there was a 50-μm thick silicon layer on the sensitive area of DUT. The energy of the Xe ion was 1230.0 MeV when it reached the sensitive region with an LET of 60.0 MeV·cm^2/mg, which has a range of 89.8 μm in silicon. It was found that the current of the chip increases with the temperature rising during the preparation (this phenomenon was not observed in uncapped devices). When the temperature of DUT exceeded 50 °C, the chip's current increased to ampere level, causing the DUT to burn out. Therefore, the DUT was

irradiated at room temperature (25 °C), 40 °C, and 47 °C. The total fluence was accumulated to 10^7 ions/cm^2 for each measurement during irradiation to obtain sufficient statistics. The photos of the heavy ion irradiation experiment are shown in Fig. 2.

3. Experimental results and discussion

The SET distribution of INV1, INV2, and INV4 for Xe ion irradiation are shown in Figs. 3–5, respectively. The parameters of SET generated in INV1, INV2, and INV4 are given in Tables 2–4. The histograms in Figs. 3–5 show the distributions of the experimentally measured SET pulse widths, and the dotted curves show the Gaussian distributions of their fittings, respectively. It can be seen that the peak pulse width of INV1, INV2, and INV4 at elevated temperature are all greater than their corresponding peak pulse widths at room temperature. For INV1 and INV2, their average pulse widths at 47 °C are the largest, but for INV4, the average pulse width is almost unchanged with temperature. The maximum pulse width of the INV1 inverter chain increases with temperature rising, the maximum pulse width of the INV2 does not change with temperature, and the maximum pulse width of the INV4 decreases with temperature increasing. For all three inverter chains, the total number of SET changes litter with temperature, which means that the SET cross sections of these three different inverter chains do not change with temperature. It can also be seen that the SET cross section of INV1 and INV2 are roughly the same, meanwhile the SET cross section of INV4 is about twice that of INV1 and INV2. As mentioned above, the drain area of the N-type or P-type FinFET in the INV1 inverter is the same as that of INV2 and half that of the INV4, which is consistent with the experimental result.

Tables 2–4 suggest that the average SET pulse wide of INV1 is larger than that of INV2 at room temperature (RT). As is well known, the SET pulse width induced by heavy ion in the inverter chain is affected by two factors: the collected charge in sensitive volume (SV) and the saturation current of the device. The larger the collected charge, the larger the SET pulse width is; the larger the saturation current, the narrower the SET pulse width is. The drain area of INV2 is the same as that of INV1, but the channel width of INV2 is larger than that of INV1. The saturation current of the INV2 inverter is twice that of INV1, which is the leading cause for a smaller average SET pulse width of INV2 relative to that of INV1. The average SET pulse width of INV4 is the largest. As is known, the INV4 has the strongest driving capability, but the drain area of INV4 is twice that of INV2 and INV1, which will double the maximum charge collection. These two factors compete with each other, resulting in the maximum average SET pulse width of the INV4 inverter.

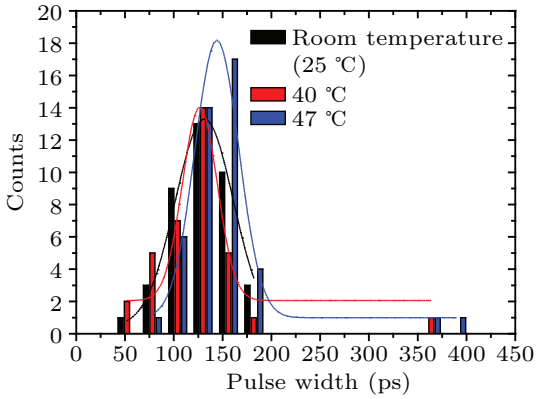


Fig. 3. SET pulse width distributions of the INV1 inverter chain for Xe ion irradiation at different temperatures.

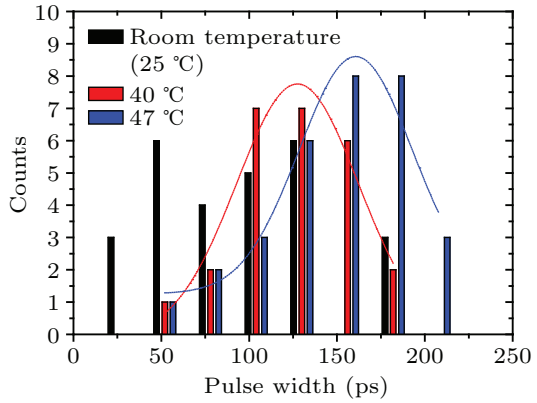


Fig. 4. SET pulse width distributions of INV2 inverter chain for Xe ion irradiation at different temperatures.

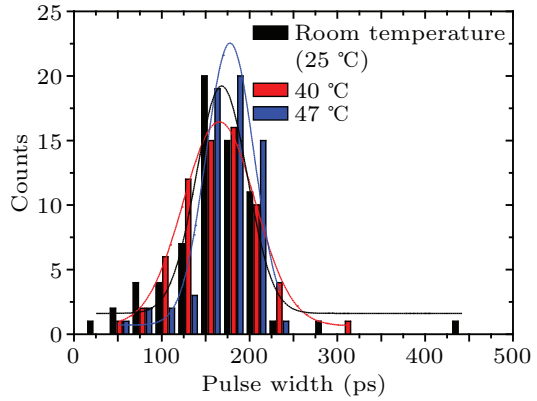


Fig. 5. SET pulse width distributions of INV4 inverter chain for Xe ion irradiation at different temperatures.

Table 2. Detailed results of SET generated in INV1 inverter chain.

Temperature (°C)	Total SET	Minimum pulse width (ps)	Maximum pulse width (ps)	Peak pulse width (ps)	Average pulse width (ps)	Standard deviation (ps)	SET cross section (10^{-10} cm^2/gate)
RT	39	52	182	130	129	30	2.77
40	35	52	364	130	125	51	2.49
47	44	78	390	156	151	55	3.13

Table 3. Detailed results of SET generated in INV2 inverter chain.

Temperature (°C)	Total SET	Minimum pulse width (ps)	Maximum pulse width (ps)	Peak pulse width (ps)	Average pulse width (ps)	Standard deviation (ps)	SET cross section (10^{-10} cm^2/gate)
RT	27	26	182	130	94	46	1.92
40	25	52	182	130	126	32	1.78
47	31	52	182	182	149	39	2.20

Table 4. Detailed results of SET generated in INV4 inverter chain.

Temperature (°C)	Total SET	Minimum pulse width (ps)	Maximum pulse width (ps)	Peak pulse width (ps)	Average pulse width (ps)	Standard deviation (ps)	SET cross section (10^{-10} cm^2/gate)
RT	67	26	442	156	162	57	4.76
40	67	52	312	182	164	44	4.76
47	63	52	234	182	171	35	4.47

The peak pulse width and average pulse width at elevated temperature are larger than those at room temperature, indicating that the SET pulse width increases with temperature rising, which is due to the parasitic bipolar amplification effect of the device. The driving strength of INV2 FinFET inverter is twice that of INV1, resulting in the average pulse width of INV1 at room temperature being greater than the average pulse width of INV2, but at elevated temperatures (40 °C and 47 °C), the average pulse width of INV1 and INV2 are almost the same, this means that the drive strength induces the decrease of SET pulse width, and the increase of pulse width caused by the temperature rising are competitive. The INV4 inverter has the largest sensitive area, in consequence, the number of SET generated in the INV4 inverter chain is the largest, that is its SET cross-section is the highest. However, the INV4 inverter has the largest driving strength at the same time. The competition between the driving strength and temperature leads the SET average pulse width of INV4 almost not to change with temperature.

4. TCAD simulations

4.1. Simulation model establishment

A 3D TCAD model of 16-nm bulk FinFET NMOS and PMOS transistors is shown in Fig. 6. The TCAD model of the FinFET device was calibrated according to the 16-nm FinFET PDK library. High-K and metal gate (HKMG) model were used to improve the control of the gate to channel. Strained silicon technology was also used, and the strained materials embedded in NMOS and PMOS were SiC and SiGe, respectively. Unlike the planar bulk silicon process, the FinFET technology adopted a lightly doped or even undoped channel to reduce the influence of the random fluctuation of doping in the channel region during device fabrication and significantly improve the carrier mobility. The doping concentration was 2×10^{20} cm^{-3} in source/drain and 1×10^{17} cm^{-3} in the channel.

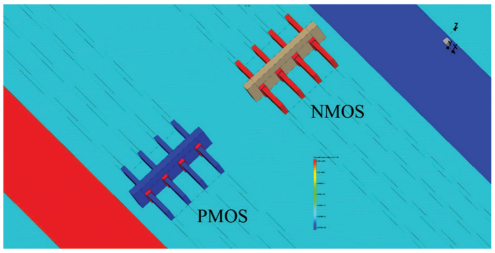


Fig. 6. TCAD model of 16-nm FinFET device.

The inverters INV1, INV2, and INV4 were the same as those used in the irradiation tests, including their threshold voltage and different current driving capabilities (different gate dimensions). As shown in Fig. 1, the NMOS transistor of INV1 had one fin, and the PMOS transistor of INV1 had four fins, the NMOS and PMOS transistor of INV2 had two fins and eights fins, respectively, and the NMOS and PMOS transistor in INV4 had four fins and sixteen fins, respectively. As mentioned above, the current driving capability of INV4 was twice that of INV2, and INV2 was twice that of INV1. The drain size for both the NMOS and PMOSin INV1 was $\sim$ 90 nm$\times$109 nm, which is the same as that for the INV2, but half that of the INV4. In order to maintain the same well voltage, the density and distance of the well contact of these three inverters were the same. The design parameters of INV1, INV2 and INV4 used in the SET simulation are shown in Table 1.

For the 16-nm bulk FinFET inverter, the supply voltage V_{DD} was 0.8 V, the entire simulation time was 300 ps, and the heavy ions were incident normally at 100 ps. The LET of ion used for simulation was 60 MeV·cm^2/mg. The heavy ion irradiation position was uniformly arranged from the source region to the drain region of the FinFET inverter, and the space between the two positions was 30 nm.

4.2. Simulation results and discussion

The SET pulse width distributions are shown in Table 5. For INV1 and INV2, the maximum pulse width occurs when heavy ion irradiates the center of the gate, and the gate and

drain region are both SET sensitive regions. The closer to the source region, the lower the sensitivity is. However, for the INV4, the source region exhibits a similar SET sensitivity to the drain region. This is because of the topology of INV4 as shown in Fig. 1, INV4 has several adjacent drain regions separated by source regions, the source region between two adjacent drain regions is also sensitive to SET as the drain region. This is due to separated drain regions that can collect more adjacent deposited charges.

Table 5. SET pulse width distributions in inverters with different gate areas.

Inverter	Minimum pulse width (ps)	Maximum pulse width (ps)	Average pulse width (ps)	Standard deviation (ps)
INV1	57.44	127.35	102.98	21.23
INV2	32.25	75.88	61.76	12.89
INV4	19.87	62.76	48.91	13.01

Table 5 shows that the minimum, maximum, and average pulse width of INV1 are all the largest, while those values of INV4 are the fewest. These results are different from experimental results. This is due to the fact that the incident heavy ion determines the location during TCAD simulation, and the number of statistics is small. For the heavy ion irradiation experiment, the location where the heavy ion is incident is random. Another possible reason is that there is only one device in the well for TCAD simulation, while for the real device, there are several devices (not only INV4, also other inverters and logical devices) in the same well, charge sharing will occur between different devices when irradiated by ions, the quantity of charge collected depends on the sensitive area of device. The INV4 has the largest sensitive area, more than twice that of INV1, results in the largest SET pulse width.

The simulated SET pulse width for heavy ion incident in the center of INV1, INV2, and INV4 NMOS transistor gate as a function of temperature are shown in Fig. 7. It can be seen that the SET pulse width increases with temperature increasing, which is consistent with the enhancement of the parasitic bipolar amplification effect of bulk silicon devices at elevated temperatures as discussed below. Figure 8 shows the variation of the saturation current of INV1, INV2, and INV4 NMOS transistors with temperature, exhibiting that the saturation currents decrease with temperature increasing, and also leading the SET pulse width to increase with temperature increasing.

The transient current can be qualitatively described by a simple equation, and given below:[40]

$$i(t) = -eN\mu' E_0\left(\mathrm{e}^{-\mu' E' t} - \mathrm{e}^{-\beta t}\right), \tag{1}$$

where N is the total collected charge, E_0 is the maximum electric field, β is the track formation time constant, μ' is an average mobility function which describes the mobility transition from ambipolar to normal carrier transport and expressed as $\mu' = (1/2)\left(\mu_\mathrm{n} + \mu_\mathrm{p}\right) F(E)$, where μ_n and μ_p are the electron mobility and hole mobility, respectively, and $F(E)$ is a correction factor.[41] It can be seen intuitively from Eq. (4.1) that the carrier mobility has a direct effect on the SET pulse width. With temperature increasing, the lower mobility results in a decreased drift velocity and a longer pulse width. This conclusion is confirmed by experimental and simulation results, except for the experimental results of INV4. This is because the scaling down in feature size from bulk silicon planar to FinFET processes complicates the understanding of device SET vulnerability.

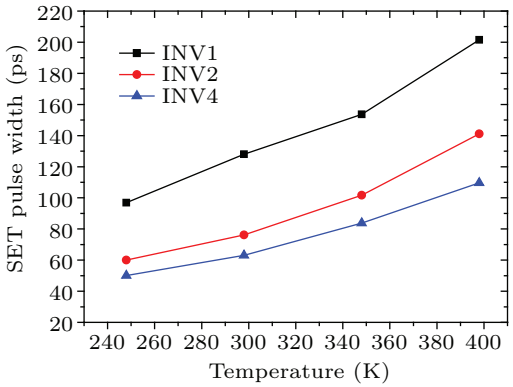


Fig. 7. Variations of SET pulse width with temperatures, with heavy ions incident on the center of gates of NMOS devices with different gate sizes.

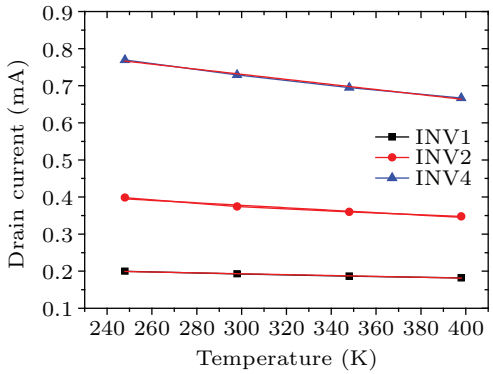


Fig. 8. Variation of saturation current with temperatures of INV1, INV2, and INV4.

The parasitic bipolar amplification effect depends on equivalent access resistance and the calculated source current.[42] The resistance between the base of the bipolar transistor and the N-well contact (named R_NW) can be described by the following equation:[43]

$$R_\mathrm{NW} \propto \frac{1}{qn\mu}. \tag{2}$$

It can be seen from Eq. (2) that since the mobility μ decreases with temperature increasing, the R_NW increases with temperature increasing. According to Ohm's law, when the I–R drop is the same, the majority carrier current to the N-well contact can be smaller. We have already known that the charges generated by the ion incidence is constant, the smaller N-well contact current means that the current to the N-well can last a longer time, hence the parasitic bipolar transistor can be turned on

for a longer time, and the parasitic bipolar effect is enhanced, resulting in longer SET pulse width.

According to the experimental results listed in Table 2 to Table 4, the experimentally measured average pulse width of INV1 and INV2 both increase with temperature increasing, but the influence of temperature on the SET pulse width of INV1 is much smaller than that of INV2, this is because the changing of saturation current with the temperature of INV2 is more significant. Linear fittings are performed on the saturation current charge curves of INV1, INV2, and INV4 as shown in Fig. 8, and the slopes of the INV1, INV2, and INV4 curves are -1.18×10^{-7}, -3.32×10^{-7}, and -6.85×10^{-7}, respectively.

Although the INV4 saturation current changes most with temperatures, the measured SET pulse width of INV4 almost does not change with temperatures. This is because the INV4 has the largest sensitive area and the strongest driving capability, these two factors compete with each other so that the temperature has almost no influence on the SET pulse width. As is well known, the SET width is directly related to the charge collection and the saturation current of the transistor. According to the experimental results, the charge collection dominates the SET pulse width of INV4, and simulation results (as shown in Fig. 9) indicate that the collected charge almost has no change with temperature increasing. Although the trend of the simulated SET pulse width as a function of temperature is different from that of experimental results, the variation of SET pulse width with the temperature of INV4 is also the smallest according to the simulation result.

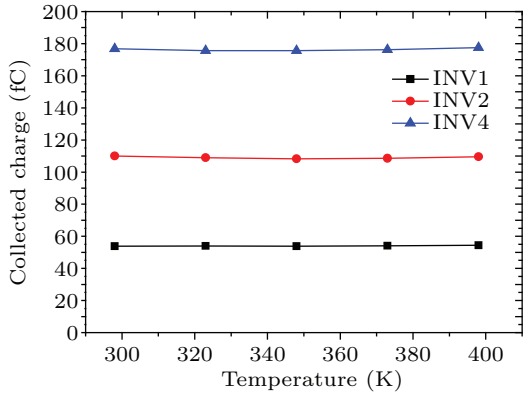


Fig. 9. Simulated charge collection *versus* temperature of INV1, INV2, and INV4.

5. Conclusions

This work has investigated the SET induced by high LET heavy ion irradiation on 16-nm bulk silicon FinFET inverter chains with different gate areas at different temperatures. Experimental results indicate that the parasitic bipolar effect of bulk silicon device will be enhanced by increasing temperature, resulting in an increase in the SET pulse width, but the increase of inverter driving strength will change the layout topology of the device, which will have a complex influence on temperature response of bulk FinFET inverter chain. As a result, the SET pulse width of the device with strong driven strength almost does not change with temperatures. The 3D TCAD simulation results show that the saturation current of FinFET devices decreases as temperature increases, leading the SET pulse width to increase with temperature rising. The heavy ion ionization-induced charges are known to increase with temperature increasing. Therefore, the SET pulse width increases with temperature increasing. Besides, the simulation result also shows that the SET pulse width of the device with the strongest driven strength has the least dependence on temperatures. These results are important for designing the electronic circuits based on FinFET technology in hope of being workable at higher temperatures (higher ambient temperature or higher device temperature due to the device's self-heating effect).

Acknowledgements

The authors would like to thank the team working at the Heavy Ion Research Facility in Lanzhou (HIRFL) for their technical assistant during the heavy ion tests. We also thank Dr. Chang Cai from Fudan University for fruitful discussion.

Project supported by the National Natural Science Foundation of China (Grant Nos. 12035019, 12105339, and 62174180) and the Opening Special Foundation of State Key Laboratory of Intense Pulsed Radiation Simulation and Effect, China (Grant No. SKLIPR2113).

References

[1] Taur Y, Buchanan D A, Chen W, Frank D J, Ismail K E, Lo S H, Halasz G S, Viswanathan R G, Wann H J and Wind S J 1997 *Proc. IEEE* **85** 486

[2] Frank D J, Dennard R H, Nowak E, Solomon P M, Taur Y and Wong H P 2001 *Proc. IEEE* **89** 259

[3] Hisamoto D, Lee W C, Kedzierski J, Takeuchi H, Asano K, Kuo C, Anderson E, King T J, Bokor J and Hu C 2000 *IEEE Trans. Electron Dev.* **47** 2320

[4] Wu S Y, Lin C Y, Chiang M C, Liaw J J, Cheng J Y, Yang S H, Chang S Z, Liang M, Miyashita T, Tsai C H, Chang C H, Chang V S, Wu Y K, Chen J H, Chen H F, Chang S Y, Pan K H, Tsui R F, Yao C H, Ting K C, Yamamoto T, Huang H T, Lee T L, Lee C H, Chang W, Lee H M, Chen C C, Chang T, Chen R, Chiu Y H, Tsai M H, Jang S M, Chen K S and Ku Y 2014 *IEEE International Electron Devices Meeting*, December 15–17, 2014, San Francisco, USA, p. 3.1.1

[5] Huang R, Jiang X B, Guo S F, Ren P P, Hao P, Yu Z Q, Zhang Z, Wang Y Y and Wang R S 2017 *IEEE International Electron Devices Meeting*, December 2–6, 2017, San Francisco, USA, p. 12.4.1

[6] Narasimham B, Hatami S, Anvar A, Harris D M, Lin A, Wang J K, Chatterjee I, Ni K, Bhuva B L, Schrimpf R D, Reed R A and McCurdy M W 2015 *IEEE Trans. Nucl. Sci.* **62** 2578

[7] Karp J, Hart M J, Maillard P, Hellings G and Linten D 2018 *IEEE Trans. Nucl. Sci.* **65** 217

[8] Li D Q, Liu T Q, Wu Z Y, Cai C, Zhao P X, He Z and Liu J 2020 *Microelectron. Reliab.* **114** 113901

[9] Agboola O 2020 *A Comparative Study of Radiation Effects on CMOS and FinFET Nano Scale Transistors in Space Applications*, Ph.D. Dissertation (Kingsville: Texas A&M University)

[10] Jennings D E, Cottini V, Nixon C A, Achterberg R K, Flasar F M, Kunde V G, Romani P N, Samuelson R E, Mamoutkine A, Gorius N J P, Coustenis A and Tokano T 2016 *Astrophys. J.* **816** L17

[11] Basilevsky A T and Head J W 2003 *Rep. Prog. Phys.* **66** 1699

[12] Nazari A and Emami H 2008 *Int. Arch. Photogramm. Remote Sens. Spat. Inf. Sci.* **37** 949

[13] Truyen D, Boch J, Sagnes B, Renaud N, Leduc E, Arnal S and Saigne F 2007 *IEEE Trans. Nucl. Sci.* **54** 1025

[14] Stapor W J, Johnson R L, Xapsos M A, Fernald K W, Campbell A B, Bhuva B L and Diehi S E 1986 *IEEE Trans. Nucl. Sci.* **33** 1610

[15] Cooper M S, Retzler J P and Messenger G C 1978 *IEEE Trans. Nucl. Sci.* **25** 1538

[16] Johnston A H, Hughlock B W, Baze M P and Plaag R E 1991 *IEEE Trans. Nucl. Sci.* **38** 1435

[17] Alles M L, Massengill L W and Kerns S E 1992 *IEEE International SOI Conference,* October 6–8, 1992, Ponte Vedra Beach, USA, p. 96

[18] Sanathanamurthy S 2008 *Simulated temperature dependency of SEU sensitivity in a 0.5-*µm *CMOS SRAM*, Ph.D. Dissertation (State of Tennessee: Vanderbilt University)

[19] Boruzdina A B, Sogoyan A V, Smolin A A, Ulanova A V, Gorbunov M S, Chumakov A I and Boychenko D V 2015 *IEEE Trans. Nucl. Sci.* **62** 2860

[20] Qin J R, C S M and Qin J R 2012 *Chin. Phys. B* **21** 89401

[21] Farjallah E, Gherman V, Armani J M and Dilillo L 2018 13*th International Conference on Design Technology of Integrated Systems In Nanoscale Era,* April 9–12, 2008, Taormina, Italy, p. 1

[22] Zhang H, Jiang H, Assis T R, Ball D R, Ni K, Kauppila J S, Schrimpf R D, Massengill L W, Bhuva B L, Narasimham B, Hatami S, Anvar A, Lin A and Wang J K 2016 *IEEE International Reliability Physics Symposium*, April 17–21, 2016, California, USA, p. 5C-3-1

[23] Atkinson N M, Ahlbin J R, Witulski A F, Gaspard N J, Holman W T, Bhuva B L, Zhang E X, Chen L and Massengill L W 2011 *IEEE Trans. Nucl. Sci.* **58** 2578

[24] Chen J, Chen S, He Y, Chi Y, Qin J, Liang B and Liu B 2012 *IEEE Trans. Nucl. Sci.* **59** 2859

[25] Fang T, Li L Q, Xia G R and Yu Y H 2021 *Chin. Phys. B* **30** 27301

[26] Laird J S, Hirao T, Onoda S, Mori H and Itoh H 2001 6*th European Conference on Radiation and Its Effects on Components and Systems*, September 10–14, 2001, Grenoble, France, p. 125

[27] Gadlage M J, Ahlbin J R, Narasimham B, Bhuva B L, Massengill L W and Schrimpf R D 2011 *IEEE Trans. Dev. Mater. Reliab.* **11** 179

[28] Guo G, Hirao T, Laird J S, Onoda S, Wakasa T, Yamakawa T and Kamiya T 2004 *IEEE Trans. Nucl. Sci.* **51** 2834

[29] Truyen D, Boch J, Sagnes B, Vaille J R, Renaud N, Leduc E, Briet M, Heng C, Mouton S and Saigné F 2008 *IEEE Trans. Nucl. Sci.* **55** 2001

[30] Gadlage M J, Ahlbin J R, Ramachandran V, Gouker P, Dinkins C A, Bhuva B L, Narasimham B, Schrimpf R D, McCurdy M W and Alles M L 2009 *IEEE Trans. Nucl. Sci.* **56** 3115

[31] Gadlage M J, Ahlbin J R, Narasimham B, Ramachandran V, Dinkins C A, Pate N D, Bhuva B L, Schrimpf R D, Massengill L W and Shuler R L 2009 *IEEE Trans. Dev. Mater. Reliab.* **10** 157

[32] Chen S M, Liang B, Liu B W and Liu Z 2008 *IEEE Trans. Nucl. Sci.* **55** 2914

[33] Liu B W, Chen S M, Liang B, Liu Z and Zhao Z Y 2009 *IEEE Trans. Nucl. Sci.* **56** 2473

[34] Cao J, Xu L, Wen S J, Fung R, Narasimham B, Massengill L W and Bhuva B L 2020 *IEEE International Reliability Physics Symposium*, April 28–May 30, 2020, Texas, USA, p. 1

[35] Kaul N, Bhuva B L and Kerns S E 1991 *IEEE Trans. Nucl. Sci.* **38** 1514

[36] Buchner S and Baze M 2001 *Nuclear and Space Radiation Effects Conference*, July 16–20, 2001, Vancouver, Canada, p. 105

[37] Gadlage M J, Ahlbin J R, Bhuva B L, Massengill L W and Schrimpf R D 2010 *IEEE International Reliability Physics Symposium*, May 2–6, 2010, California, USA, p. 763

[38] Ahlbin J R, Atkinson N M, Gadlage M J, Gaspard N J, Bhuva B L, Loveless T D, Zhang E X, Chen L and Massengill L W 2011 *IEEE Trans. Nucl. Sci.* **58** 2585

[39] Narasimham B, Ramachandran V, Bhuva B L, Schrimpf R D, Witulski A F, Holman W T, Massengill L W, Black J D, Robinson W H and McMorrow D 2006 *IEEE Trans. Dev. Mater. Reliab.* **6** 542

[40] Laird J S, Hirao T, Onoda S, Mori H and Itoh H 2001 *European Conference on Radiation and Its Effects on Components and Systems*, September 10–14, 2001, Grenoble, France, p. 125

[41] Messenger G C 1982 *IEEE Trans. Nucl. Sci.* **29** 2024

[42] Artola L, Hubert G and Schrimpf R D 2013 *IEEE International Reliability Physics Symposium (IRPS)*, April 14–18, 2013, California, USA, p. SE.1.1

[43] Liu B, Chen S, Liang B, Liu Z and Zhao Z 2009 *IEEE Trans. Nucl. Sci.* **56** 2473