

High-performance vertical GaN field-effect transistor with an integrated self-adapted channel diode for reverse conduction

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High-performance vertical GaN field-effect transistor with an integrated self-adapted channel diode for reverse conduction

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A vertical GaN field-effect transistor with an integrated self-adapted channel diode (CD-FET) is proposed to improve the reverse conduction performance. It features a channel diode (CD) formed between a trench source on the insulator and a P-type barrier layer (PBL), together with a P-shield layer under the trench gate. At forward conduction, the CD is pinched off due to depletion effects caused by both the PBL and the metal–insulator–semiconductor structure from the trench source, without influencing the on-state characteristic of the CD-FET. At reverse conduction, the depletion region narrows and thus the CD turns on to achieve a very low turn-on voltage (V_F), preventing the inherent body diode from turning on. Meanwhile, the PBL and P-shield layer can modulate the electric field distribution to improve the off-state breakdown voltage (BV). Moreover, the P-shield not only shields the gate from a high electric field but also transforms part of C_{GD} to C_{GS} so as to significantly reduce the gate charge (Q_{GD}), leading to a low switching loss (E_{switch}). Consequently, the proposed CD-FET achieves a low V_F of 1.65 V and a high BV of 1446 V, and V_F, Q_{GD} and E_{switch} of the CD-FET are decreased by 49%, 55% and 80%, respectively, compared with those of a conventional metal–oxide–semiconductor field-effect transistor (MOSFET).

Keywords: GaN field effect transistor, reverse conduction, integrated diode, turn-on voltage

PACS: 85.30.De, 85.30.Tv, 73.40.Qv, 51.50.+v **DOI:** 10.1088/1674-1056/ac8ce6

1. Introduction

GaN power devices perform at high frequency, high efficiency and high power density in power conversion systems.[1–3] At present, GaN horizontal high electron mobility transistors (HEMTs)[4–6] have been successfully commercialized because the two-dimensional electron gas (2DEG) causes low on-resistance and low loss, but it is difficult to obtain a breakdown voltage (BV) higher than 1.2 kV. Vertical GaN devices could improve BV by increasing the thickness of the vertical drift region without increasing the chip area, and thus an improved power density and a reduced power loss can be achieved. Moreover, the peak electric field (E-field) of a vertical GaN device is far from the surface, and is less affected by traps or defects in the surface, thus achieving better reliability. Several vertical GaN devices have been reported, such as the current aperture vertical electronic transistor (CAVET),[7–9] the metal–oxide–semiconductor field-effect transistor (MOSFET) with a trench gate[10–12] and GaN vertical fin transistors.[13–15]

In practical power electronics applications, a freewheeling diode (FWD) is necessary to provide a reverse current flow path.[16] The inherent p–i–n diode in a vertical GaN MOSFET as a FWD has a high turn-on voltage (typically $V_F \approx 3$ V),[17] and its bipolar effect also degrades the reverse conduction performance. Generally, a Schottky barrier diode (SBD) anti-paralleled externally with a conventional MOSFET[18] can address the issue, but it increases the area and introduces extra parasitic inductance and capacitance, leading to increased power loss. To solve the above problems, vertical GaN transistors with an integrated unipolar diode are a better choice.[19,20] However, there are few reports on the related structures.

In this paper, a novel vertical GaN MOSFET with an integrated channel diode (CD-FET) is proposed to improve the reverse conduction performance, maintaining high performance in the on-state, blocking state and switching state. The reverse turn-on voltage (V_F) of the proposed device is significantly reduced compared with that of a conventional MOSFET with an inherent body diode as a FWD. In addition, the integrated channel diode (CD) does not add an extra parasitic parameter.

2. Device structure and mechanism

Figure 1(a) shows a schematic section of the proposed CD-FET. Its main feature is the integrated CD under the trench source to realize reverse conduction. The vertical extended side of the trench source contacts with N-drift as the anode of the CD, and the other surface side is embedded in the P-base to avoid latch-up. Both the P-type barrier layer (PBL) and the P-shield layer are shorted with the source. The body diode (BD) acts as a FWD in a conventional MOSFET, as marked in Fig. 1(b).

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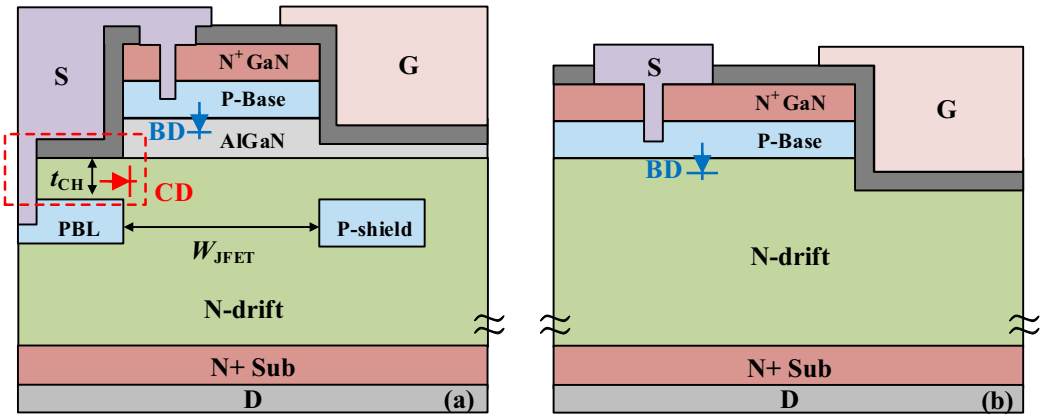
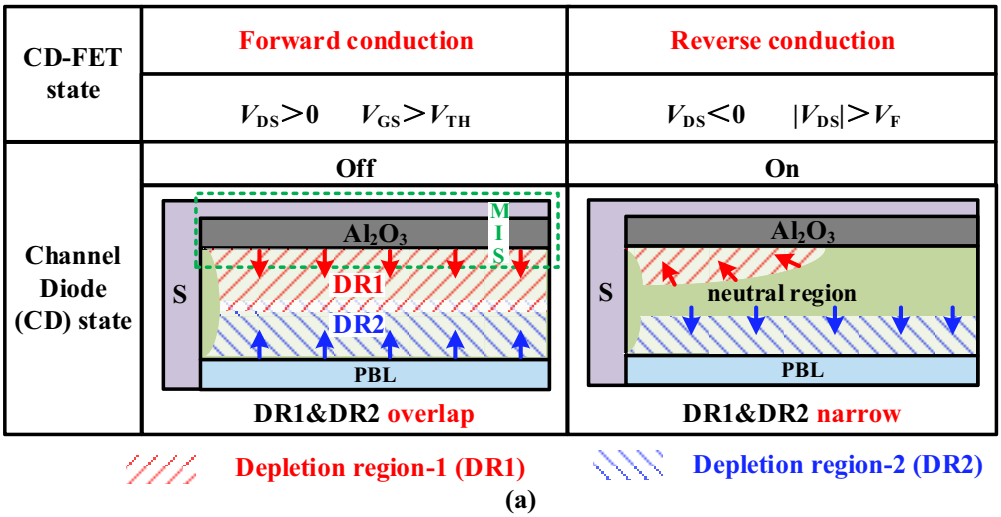
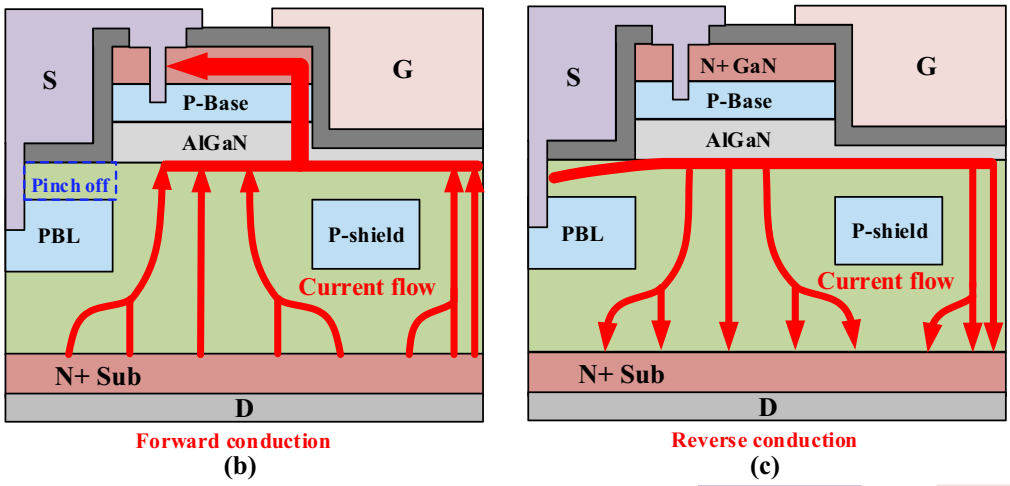


Fig. 1. Schematic cross section of (a) the CD-FET and (b) a conventional MOSFET.





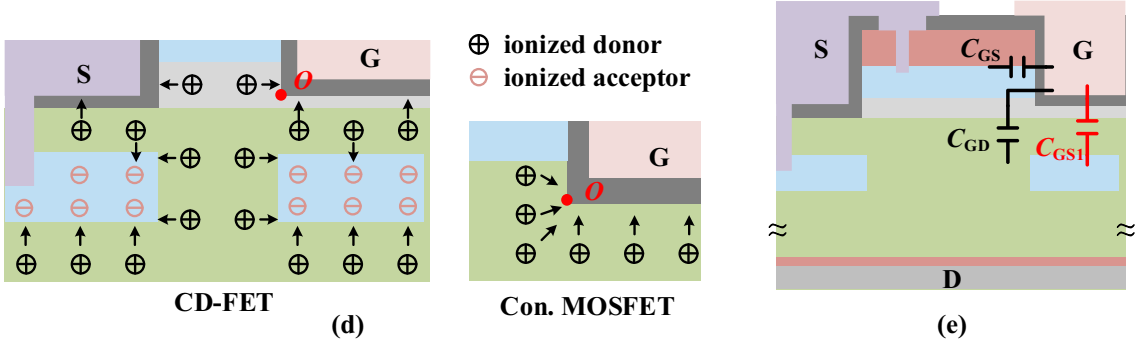


Fig. 2. (a) States of the CD-FET and CD. Operation mechanism at (b) forward conduction and (c) reverse conduction for the CD-FET. (d) Blocking state for the CD-FET and conventional MOSFET. (e) C_{GD} and C_{GS} for the CD-FET.

The t_{CH} is the channel thickness of the CD and W_{JEFT} is the distance between the PBL and the P-shield layer. The thickness of the AlGaN, PBL and P-shield layers is 80 nm, 800 nm and 800 nm, respectively. The thickness of the N-drift and P-base for the CD-FET and conventional MOSFET is 10 μm and 400 nm, respectively. Simulations have been carried out in Sentaurus TCAD,[21] and physics models are used to make the simulation accurate, for example, the doping dependence model, the Auger model, the Shockley–Read–Hall recombination model, the high-field saturation model, the piezoelectric polarization (strain) model and the avalanche (van Overstraeten) model. The effective electron mobility in the GaN N-drift region is set as 900 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [22] and the effective electron mobility on the sidewalls of the gate is set as 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$, owing to the etch damage.[22]

Figure 2(a) illustrates the states of the CD-FET and CD. The trench source metal/Al_2O_3/GaN forms the metal–insulator–semiconductor (MIS) structure. Owing to the work function difference between the metal and GaN in the MIS, depletion region-1 (DR1) is formed. Depletion region-2 (DR2) is formed by the PN junction composed of the N-drift region and the PBL. At $V_{DS} > 0$ and $V_{GS} > V_{TH}$, the CD-FET is in the forward conduction state, and DR1 and DR2 overlap to pinch-off the CD channel. In this case, the forward current flows via the inversion layer along the sidewall of the gate, as denoted by the red arrow in Fig. 2(b). In the reverse conduction state, when $|V_{DS}| > V_F$, the depletion region narrows and the CD turns on in Fig. 2(a). Thus, the CD provides a reverse current path as denoted in Fig. 2(c). It is worth noting that V_F of the CD is much smaller than that of the body diode, because the on-state voltage of the PN junction is high for a wideband semiconductor. Figure 2(d) shows that the P-shield layer in the CD-FET alleviates E-field crowding at the corner of gate (O) in the off-state, compared with the conventional MOSFET. Moreover, the PBL and P-shield layer modulate the E-field distribution in the drift region, and the electric field between the PBL and P-shield weakens these so as to further improve BV. Furthermore, the P-shield layer also effectively transforms part of C_{GD} into C_{GS}, as shown is Fig. 2(e), which effectively reduces the switching loss of the device. The 2DEG in the AlGaN/N-drift GaN interface acts as a current distribution layer to decrease the on-resistance.

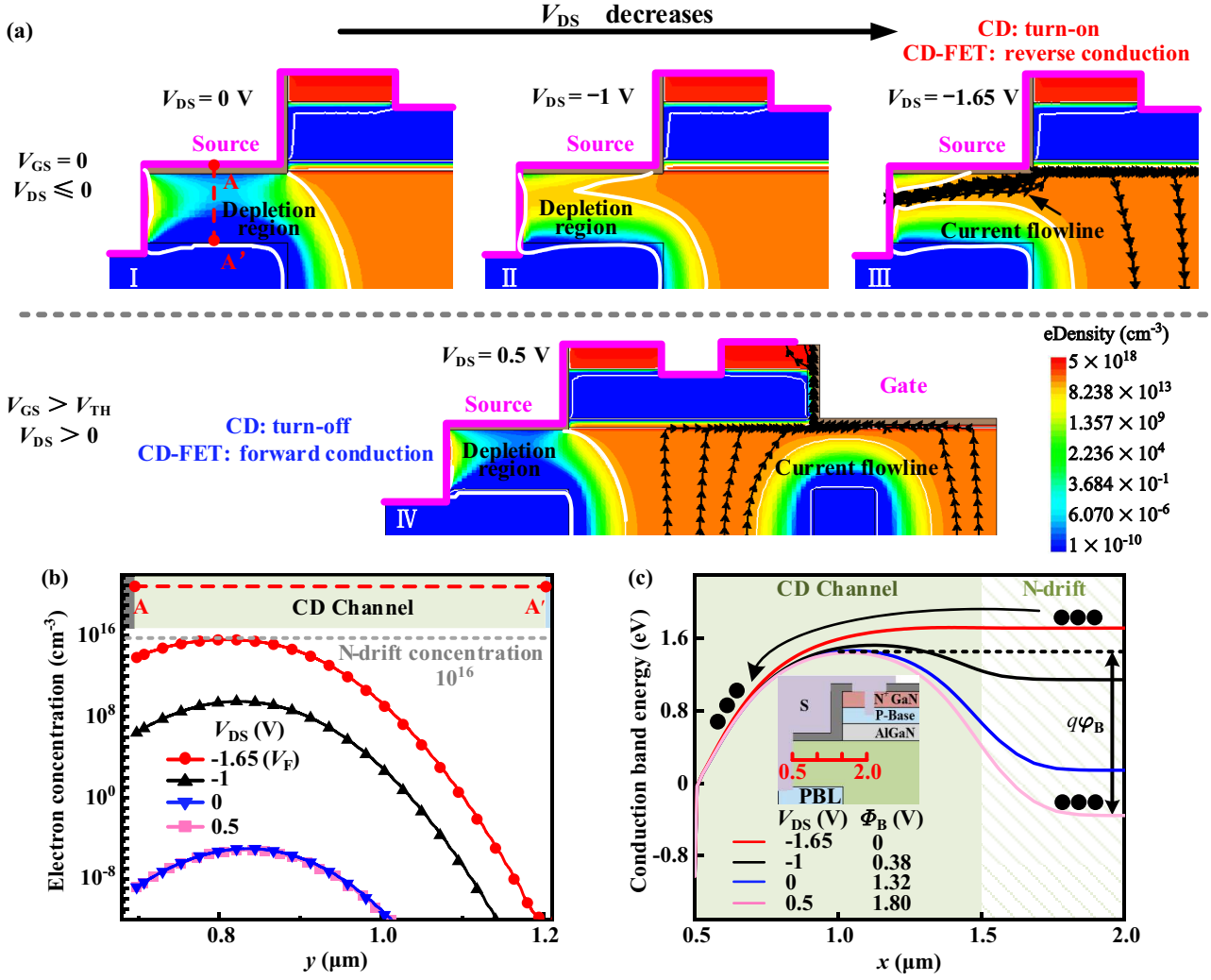


Fig. 3. (a) Electron concentration contours at different V_{DS}. (b) Electron concentration distribution at the line AA′. (c) Conduction band energy along the CD lateral channel at different V_{DS}.

3. Results and discussion

Figure 3(a) shows the electron concentration contour of the CD region at different V_{DS}. At $V_{DS} = 0$ and -1 V, the depletion regions are merged and the CD is in the off-state as illustrated by I and II in Fig. 3(a). The electron concentration in the CD channel is much less than the N-drift doping, N_d, of 1×10^{16} cm^{-3} as shown in Fig. 3(b). The depletion regions narrow with decreasing V_{DS}, and the current path is turned on as shown in III in Fig. 3(a), with the highest electron concentration in the CD up to N_d. V_F is defined as the $|V_{DS}|$ at $I_{DS} = -100$ A·cm^{-2}, so $V_F = 1.65$ V. It is worth mentioning that the CD channel is pinched off at CD-FET forward conduction ($V_{DS} > 0$), as shown by IV in Fig. 3(a). Figure 3(c) shows the extracted conduction band energy curves along the CD lateral channel. The barrier height ($q\varphi_B$) along the CD channel increases with increasing V_{DS}, which is affected by the depletion effect. When $V_{DS} > -1.65$ V, the barrier prevents electrons from flowing toward the anode of the CD. At $V_{DS} = -1.65$ V, the electronic barrier disappears and the CD turns on.

Figure 4 shows the reverse conduction characteristic and the corresponding equivalent circuits for the CD-FET and conventional MOSFET. The non-junction CD as a FWD in the CD-FET turns on prior to the body diode, as shown in Fig. 4(b), achieving a very low V_F. Therefore, V_F of the CD-FET is significantly reduced to 1.65 V from 3.24 V in the conventional MOSFET with a body diode as the FWD.

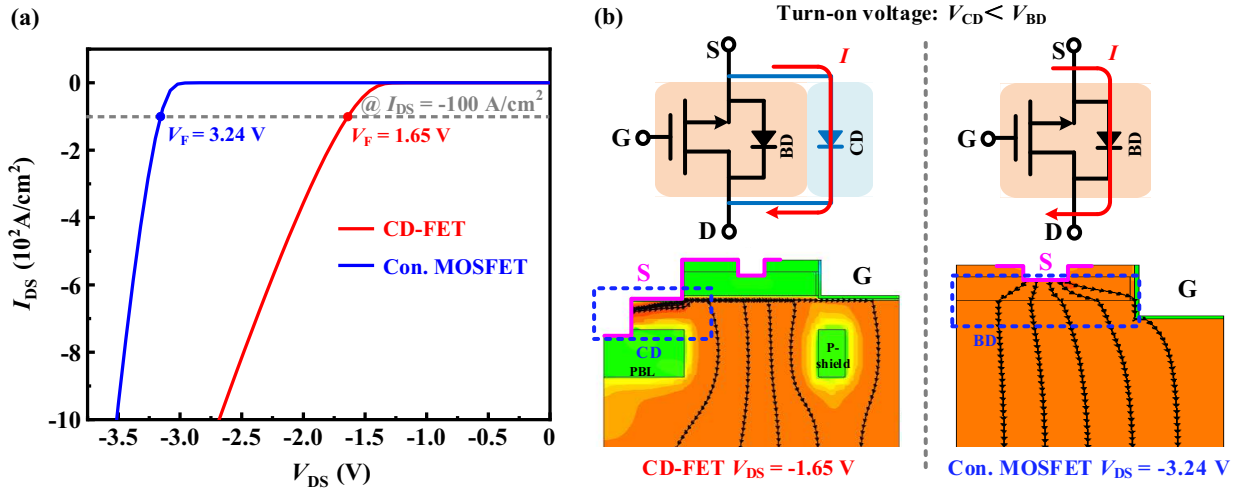


Fig. 4. Reverse conduction characteristics of a CD-FET and a conventional MOSFET: (a) *I*–*V* curves and (b) equivalent circuit and current density distribution (@$|V_{DS}| = V_F$).

Figure 5 shows the gate charge characteristics of the two devices. The gate charge (Q_{GD}) of the CD-FET is 519 nC·cm^{-2}, which is far less than the 1160 nC·cm^{-2} of the conventional MOSFET. The reason is that the overlap area between the gate and drain is reduced by the P-shield layer (shorted to the source), and thus part of the C_{GD} transforms to the C_{GS}, leading to a reduced Q_{GD} for the CD-FET. Q_{GD} will determine the switching loss.

Figure 6(a) shows the test circuit for simulation of the switching characteristic. The load inductance and load current used in the simulation are 10 nH and 100 A·cm^{-2}, respectively. Figures 6(b) and 6(c) show the turn-on waveforms at $R_G = 5$ Ω and turn-off waveforms under different R_G values, respectively. Owing to the ultralow Q_{GD} for the CD-FET, much higher dV/dt values are obtained during switching. Therefore, the CD-FET contributes to a reduction in turn-on loss (E_{on}) and turn-off loss (E_{off}) of 82% and 78%, respectively, compared with those of a conventional MOSFET. Meanwhile, the current and voltage oscillations decrease while the switching time increases with increasing R_G. Figures 6(d) and 6(e) show the dependence of switching loss ($E_{switch} = E_{on} + E_{off}$) on R_G, respectively. Compared with a conventional MOSFET, the CD-FET exhibits a low switching loss under different R_G values, and reduces the switching loss by 80% at $R_G = 5$ Ω. As R_G increases, the difference in the switching loss between the two devices increases.

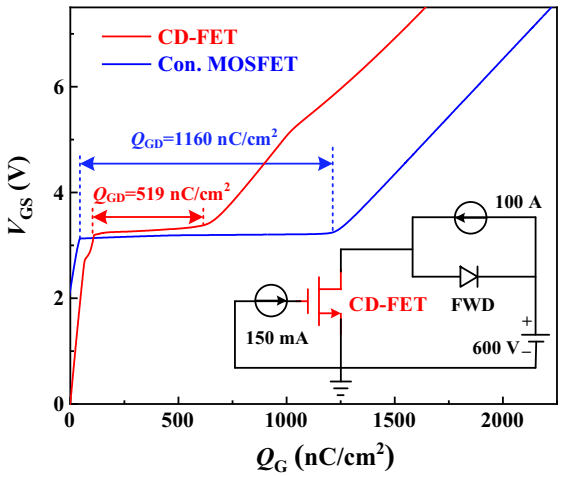


Fig. 5. Gate charge characteristics and the test circuit for simulation.

Figures 7(a) and 7(b) compare the E-field distribution of the two devices at breakdown. The breakdown criterion is defined as when I_d reaches 0.1 A·cm^{-2}.[23,24] For the CD-FET, the P-shield layer and PBL introduce new E-field peaks (at $P1$ and $P2$) and enhance the E-field strength in the drift region. Meanwhile, the P-shield layer alleviates E-field crowding at the bottom corner of the gate (O), leading to a reduced E-field at the gate corner, with $E_O = 1.28$ MV·cm^{-1} even at $V_{DS} = 1446$ V, as illustrated in Fig. 7(b). For the conventional MOSFET, E-field crowding results in $E_O = 3.49$ MV·cm^{-1}, and premature breakdown occurs at BV = 833 V in Fig. 7(c). Table 1 summarizes the comprehensive performances of the two devices. Compared with the conventional MOSFET, the CD-FET exhibits high performance, including a high value for Baliga's figure of merit (FOM = BV^2/$R_{on,sp}$), low V_F, high BV and ultralow Q_{GD} and switching loss.

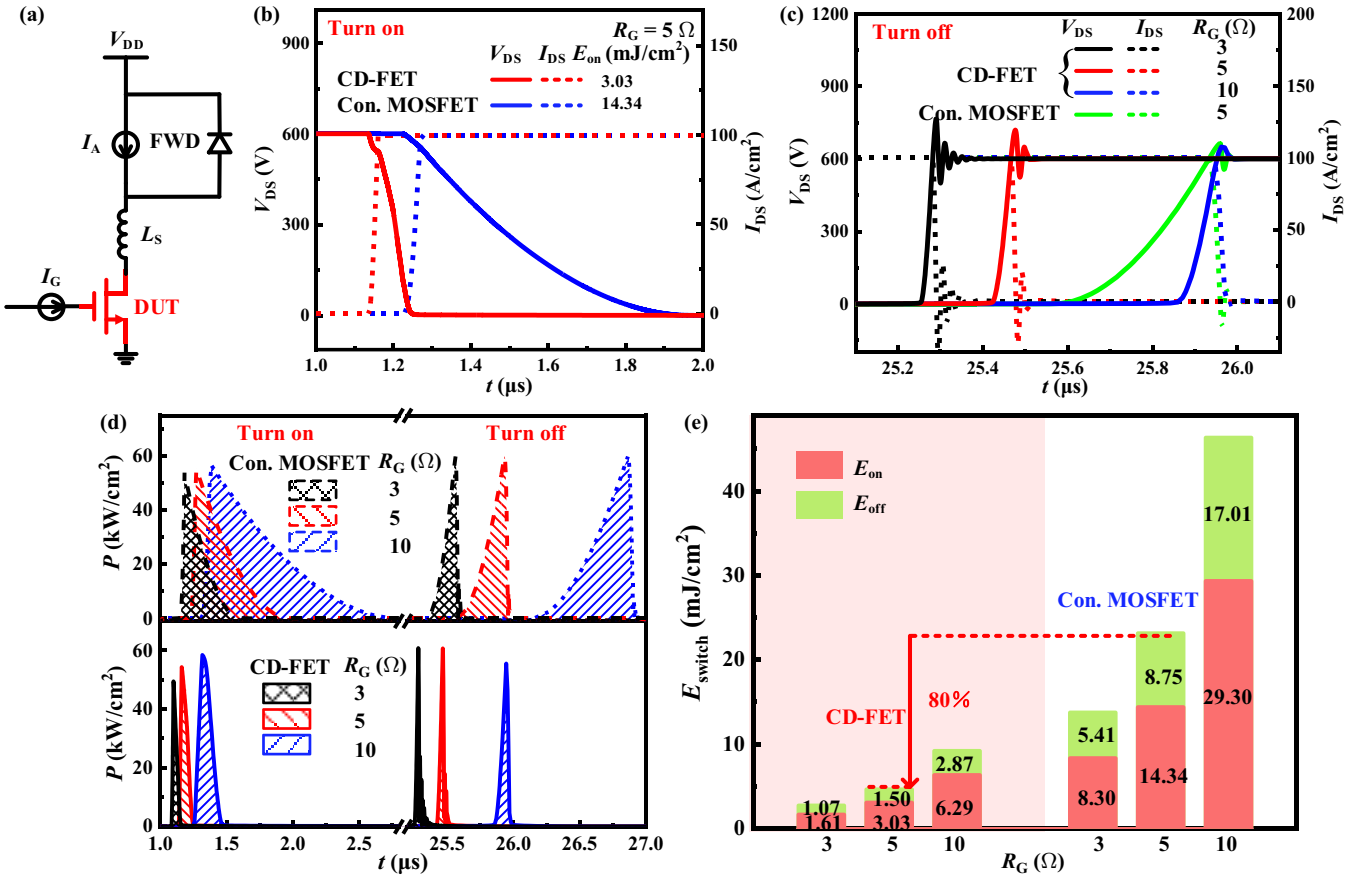


Fig. 6. (a) Test circuit for simulation of the switching characteristic. (b) Turn-on waveforms at $R_G = 5$ Ω and (c) turn-off waveforms under different R_G values for the two devices. Panels (d) and (e) compare switching losses of the two devices at different R_G.

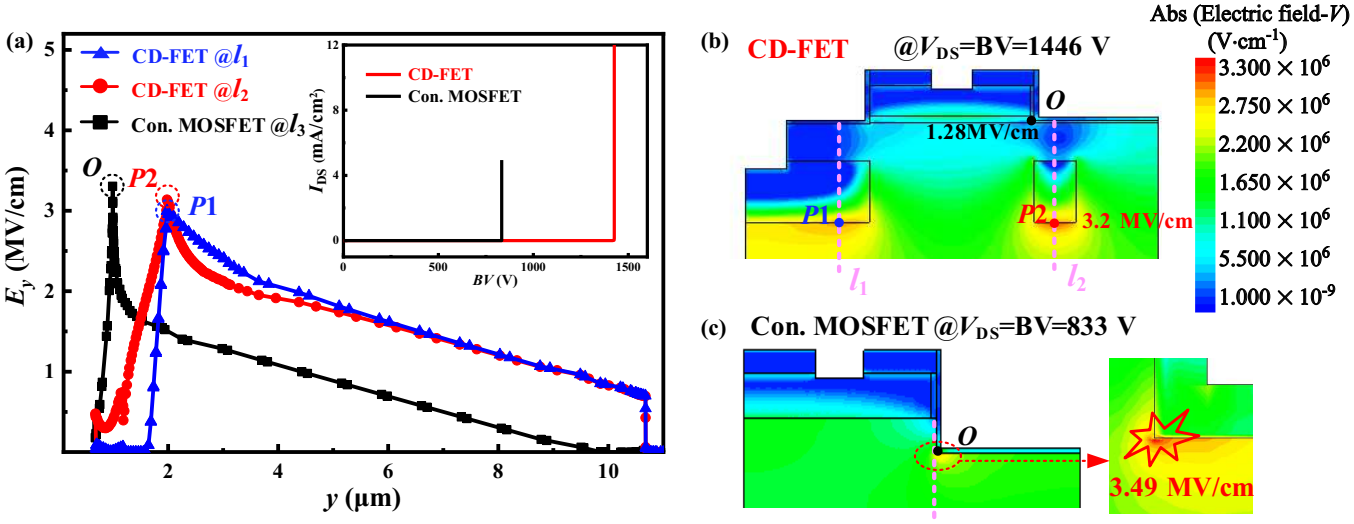


Fig. 7. (a) The I–V curves, and E_y along l_1, l_2 andl_3 at breakdown. E-field distribution at breakdown for (b) a CD-FET and (c) a conventional MOSFET.

Table 1. Performance comparison of the two devices.

	V_F (V)	BV (V)	$R_{on,sp}$ (mΩ/cm²)	FOM (MW/mm²)	Q_{GD} (nC/cm²)	E_{switch} (mJ/cm²)
CD-FET	1.65	1446	0.85	2.47	519	4.53
Con. MOSFET	3.24	833	0.64	1.08	1160	23.09

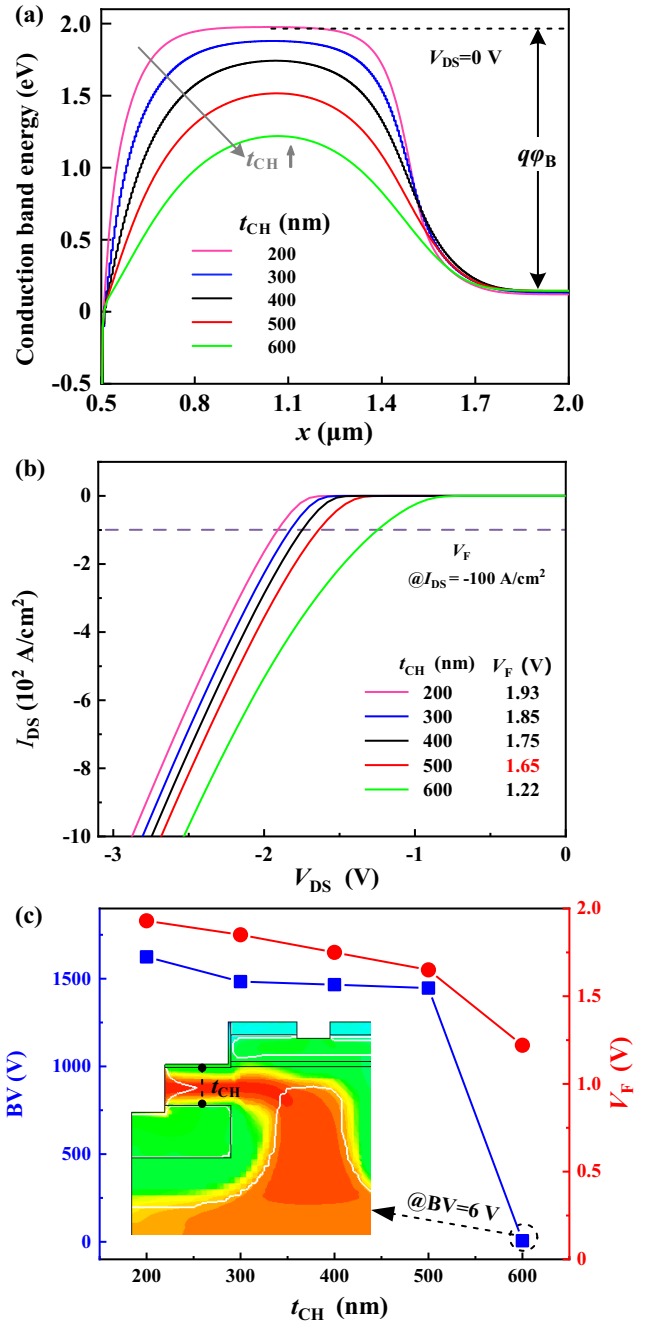


Fig. 8. (a) Conduction band energy along the CD channel at different t_{CH}. (b) Reverse conduction characteristics at different t_{CH}. (c) Dependence of V_F and BV on t_{CH}.

Figures 8(a) and 8(b) show the influence of t_{CH} on the reverse conduction characteristics. The increase in t_{CH} weakens the pinch-off effect, and thus $q\varphi_B$ and V_F decrease. Unfortunately, the leakage current in the CD channel is increased, and thus BV decreases, as shown in Fig. 8(c). The device with $t_{CH} \leq 500$ nm has a high BV which is less sensitive to change in t_{CH} because of the strong pinch-off effect. For $t_{CH} = 600$ nm, the CD channel fails to be pinched-off and the excessive leakage current leads to premature breakdown at 6 V with $I_d = 0.1$ A·cm^{-2}. It is worth mentioning that $R_{on,sp}$ is insensitive to the change in t_{CH} because the forward current of the CD-FET does not flow through the CD channel.

Figure 9 demonstrates the influences of N_P and W_{JFET} on $R_{on,sp}$, BV and V_F for the CD-FET. With increasing N_P, the E-fields of $P1$ and $P2$ increase (see Figs. 7(b) and 7(c)), and the leakage current decreases owing to the enhancement of the pinch-off effect by the PBL, and thus BV increases. However, when $N_P > 5 \times 10^{17}$ cm^{-3}, the high E-field of $P2$ causes premature breakdown, and BV decreases as N_P increases. $R_{on,sp}$ hardly changes because the variation of N_P has little influence on the long current path in the drift region. V_F is constant because the pinch-off effect is strong enough and the CD is always in the off-state when $N_P \geq 1 \times 10^{17}$ cm^{-3}. The opening of the CD mainly depends on DR1 narrowing, as shown in Fig. 3(a). With decreasing W_{JFET}, the depletion effect for the junction field-effect transistor region is enhanced, the leakage current decreases in the off-state and thus BV increases. Meanwhile, the current path is narrowed in the on-state, leading to an increase in $R_{on,sp}$. The opening of the CD channel is limited by the narrower t_{CH}, so V_F is constant.

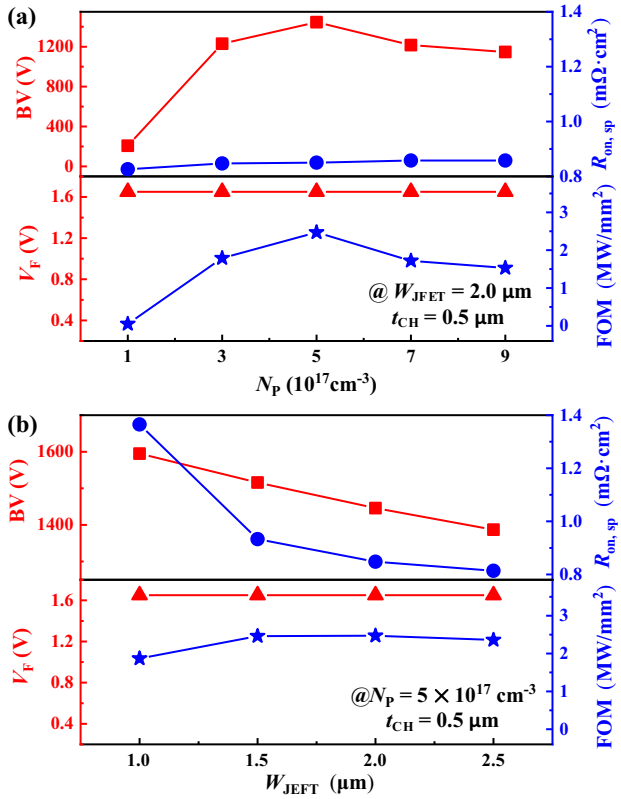


Fig. 9. Influences of W_{JFET} and N_P on BV and $R_{on,sp}$.

4. Conclusion

A vertical GaN FET with an integrated self-adapted CD is proposed to realize reverse conduction with a lower V_F. At

forward conduction of the CD-FET, the CD is turned off without affecting the on-state characteristic. At reverse conduction, the CD turns on prior to the body diode, achieving a low V_F. Meanwhile, the PBL and P-shield layer modulate the E-field distribution to realize a high BV. The introduced P-shield also results in a much lower Q_{GD}. Therefore, V_F, Q_{GD} and E_{switch} of the CD-FET are decreased by 49%, 55% and 80%, respectively, compared with the values for a conventional MOSFET. In addition, the CD-FET is beneficial for reducing parasitic inductance and the total chip area compared with the conventional method of using an externally connected SBD.

Acknowledgments

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