Experiment and simulation on degradation and burnout mechanisms of SiC MOSFET under heavy ion irradiation

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Experiments and simulation studies on 283 MeV I ion induced single event effects of silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) were carried out. When the cumulative irradiation fluence of the SiC MOSFET reached 5×10^6 ion·cm^{-2}, the drain–gate channel current increased under 200 V drain voltage, the drain–gate channel current and the drain–source channel current increased under 350 V drain voltage. The device occurred single event burnout under 800 V drain voltage, resulting in a complete loss of breakdown voltage. Combined with emission microscope, scanning electron microscope and focused ion beam analysis, the device with increased drain–gate channel current and drain–source channel current was found to have drain–gate channel current leakage point and local source metal melt, and the device with single event burnout was found to have local melting of its gate, source, epitaxial layer and substrate. Combining with Monte Carlo simulation and TCAD electrothermal simulation, it was found that the initial area of single event burnout might occur at the source–gate corner or the substrate–epitaxial interface, electric field and current density both affected the lattice temperature peak. The excessive lattice temperature during the irradiation process appeared at the local source contact, which led to the drain–source channel damage. And the excessive electric field appeared in the gate oxide layer, resulting in drain–gate channel damage.

Keywords: heavy ion, silicon carbide metal–oxide–semiconductor field-effect transistors (SiC MOSFET), drain–gate channel, drain–source channel, single event burnout, TCAD simulation

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1. Introduction

Silicon carbide (SiC) materials have obvious advantages over silicon in terms of breakdown voltage, thermal conductivity, and power density. Therefore, SiC power devices have huge application prospects. Especially in the electric energy conversion device of electric vehicles, the use of SiC power devices can significantly reduce the volume and power consumption compared to that of the silicon-based power devices. SiC material has a large bandgap, theoretically, it should have better radiation resistance.[1,2] It is found in the research that the degradation process of SiC diodes and metal–oxide–semiconductor field-effect transistors (MOSFETs) can be roughly divided into three stages of charge collection, leakage current increase, and devastating burnout with the increase of the bias voltage and linear energy transfer (LET).[3] In the charge collection stage, except for the displacement damage that may be caused by the high cumulative particle fluence, the performance of the SiC power device is not affected.[4–6] When the bias voltage and LET reach the single event leakage current (SELC) threshold, the leakage current of the SiC power device will increase to varying degrees during the irradiation process, resulting in the degradation of the electrical characteristics of the SiC power device after irradiation, especially the breakdown characteristics.[7–10] When single event burnout (SEB) occurs, the breakdown characteristics of SiC diodes and MOSFETs are completely lost, and they no longer have switching functions in power conversion systems.

When the bias voltage is high enough, heavy ions, protons, and neutrons may all cause SEB. When SEB occurred in the SiC MOSFET, there may also be a single-event gate rupture (SEGR) effect.[11–19] Both SiC diodes and MOSFETs will occur SELC under heavy ion irradiation. The localized avalanche breakdown due to ion-induced electric field spikes is considered to be the cause of SEB in Si diodes, and SEB in Si MOSFETs is thought to be caused by the opening of parasitic bipolar junction transistors.[20] Some existing simulation work believes that SEB and SELC in SiC MOSFET and SiC diode are due to excessive power that cannot be dissipated in time, which further leading to thermal effects.[21–24] The SEB locations of SiC power devices can be obviously observed, and it is difficult to directly observe the SELC location.[12,13,25] Single event effects seriously restrict the application of SiC

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power devices in the space field, and the burn-out and degradation of SiC power devices and their effect mechanisms need to be further studied.

In this paper, 283 MeV I ions are used to carry out heavy ion irradiation experiments of the SiC MOSFETs under different bias voltages. In the experiments, the drain current and transient pulse current of the SiC MOSFET are monitored in real time. The static electrical characteristics of the device are tested and analyzed. After the irradiation experiment, the leakage point of the burnt and degraded devices is located using emission microscope (EMMI), and scanning electron microscope (SEM) and focused ion beam (FIB) to visually observe and analyze the microscopic damage characteristics. The temporal and spatial distribution of heavy-ion induced energy loss in SiC MOSFET is calculated using Monte Carlo simulation. Further combined with TCAD tool, the electrothermal effect induced in the SiC MOSFET and its evolution when heavy ions are incident on the device under different bias voltages are simulated.

2. Experimental details

The heavy-ion experiment was carried out on the heavy-ion accelerator device of the Chinese Institute of Atomic Energy. The device selected for the experiment is the third-generation SiC MOSFET C3M0120090D produced by Cree company, and its rated current and on-resistance are 23 A and 120 mΩ. Before the experiment, we removed the front package of the device and conducted electrical parameter tests to ensure a good electrical performance of the device. The heavy ion selected in the experiment is the 283 MeV I ion, and the LET value is 70.2 MeV·cm^2·mg^{-1}. It should be noted that the LET value mentioned in the article refers to the surface LET value of the 283 MeV I ion, and its LET value varies with the depth of incidence with the transport of heavy ions in the SiC MOSFET. The range of I ions with energy of 283 MeV in SiC does not exceed 20 μm.

Based on the existing research on the degradation of SiC MOSFET under heavy ion irradiation, we carried out heavy ion irradiation experiments under three bias voltages of 200 V, 350 V, and 800 V. The SiC MOSFET cell structure and the test circuit diagram used in the heavy ion experiment are shown in Fig. 1. Figure 1(a) is the cell structure of the SiC MOSFET obtained by FIB-SEM analysis. The white metal Pt on the top of Fig. 1(a) is sprayed before FIB analysis and is not a material component of the SiC MOSFET. The SiC MOSFET used in the experiment is a planar vertical channel device. The SiC MOSFET consists of Al metal, SiO_2 oxide layer, Si gate, SiO_2 oxide layer and SiC material from top to bottom. The doping concentration of each region in the SiC material is indistinguishable in the FIB-SEM, and the total thickness of the epitaxial layer and substrate is 190 μm. Figure 1(b) is a cell model diagram of the SiC MOSFET established according to Fig. 1(a), and it shows the basic structure of SiC MOSFET and the thickness of each region on the top of SiC material. In the epitaxial layer of the SiC MOSFET, the N+ region is connected to the source, and the channel region is located near the interface between the P-based region and SiO_2. In the heavy ion experiment, the drain of SiC MOSFET was applied with a forward bias voltage, the source and gate were grounded, and the bias voltage V_{bias} mentioned below all represented the voltage of the drain. As shown in Fig. 1(c), R_0 in the circuit is a protection resistor with a resistance of 200 kΩ to ensure that the circuit current is lower than the limit current of the high-voltage power supply. The resistances of resistors R_2 and R_3 are 100 MΩ and 200 kΩ, respectively, and the sampling resistor R_3 is used to monitor transient current. A resistor R_1 with a resistance value of 1 Ω is connected in series with the irradiation SiC MOSFET to capture the pulse current when SEB or SELC occurs. The capture of the pulse current in the experiment was done with an oscilloscope, and the trigger was set on R_3. The drain current of SiC MOSFETs is monitored and stored in real time by computer controlled digital multimeter. The partial voltage of the protective resistor R_0 is considered to ensure the accuracy of the bias voltage of the irradiation SiC MOSFET. The partial voltage of 200 kΩ accounts for about 2% of the DC power supply V_{DC}. In the experiment, the pulse voltage changes on the R_3 and R_1 are recorded and stored, which can reflect the transient current changes of the irradiation SiC MOSFET.[16]

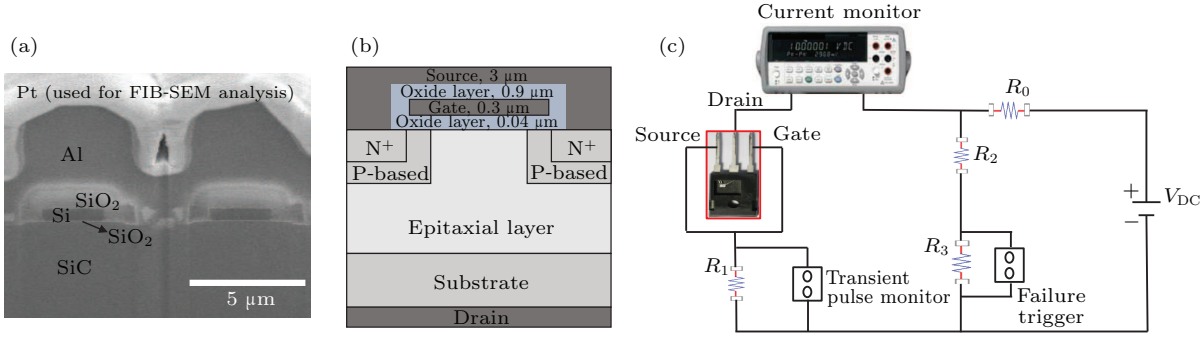


Fig. 1. Heavy ion experiment: (a) SiC MOSFET cell structure; (b) model diagram of SiC MOSFET; (c) schematic diagram of the test circuit.

The heavy-ion flux in the experiment ranges from 1000 ion·cm^{-2}·s^{-1} to 60000 ion·cm^{-2}·s^{-1}. If SEB occurs in the SiC MOSFET during the experiment, stop the experiment. If the drain current of the device increases, stop the experiment when the cumulative fluence reaches 5×10^6 ion·cm^{-2}. Figure 2 shows the gate degradation, SELC and SEB of SiC MOSFETs under different bias voltages. The blue, green, and red dashed lines are the limiting currents of the test circuit when the device burns out under different bias voltages. As shown in Fig. 2(a), when the bias voltage is 200 V, the drain current will have certain noise fluctuations, but the drain current of the SiC MOSFET does not change when the cumulative fluence reached 5×10^6 ion·cm^{-2}. At the beginning of irradiation, the bias voltage of the device is 350 V, if SEB occurs, the drain current of the device will directly from a drain current of less than 1×10^{-8} A reach to the limit current 1.75×10^{-3} A, as shown by the blue dotted line in Fig. 2(a). Since the 350 V bias voltage does not reach the SEB threshold voltage of the SiC MOSFET at this LET value but exceeds the SELC threshold voltage, the heavy ion-induced damage causes the drain current to continuously increase. The bias voltage also decreases continuously due to the voltage dividing effect of the protection resistor, which leads to a decrease in the increase rate of the drain current with the increase of the cumulative fluence, as shown by the blue line in Fig. 2(a). When the cumulative fluence reaches 5×10^6 ion·cm^{-2}, the drain current of the device is about 1.84×10^{-4} A, and the drain bias voltage is about 300.2 V.

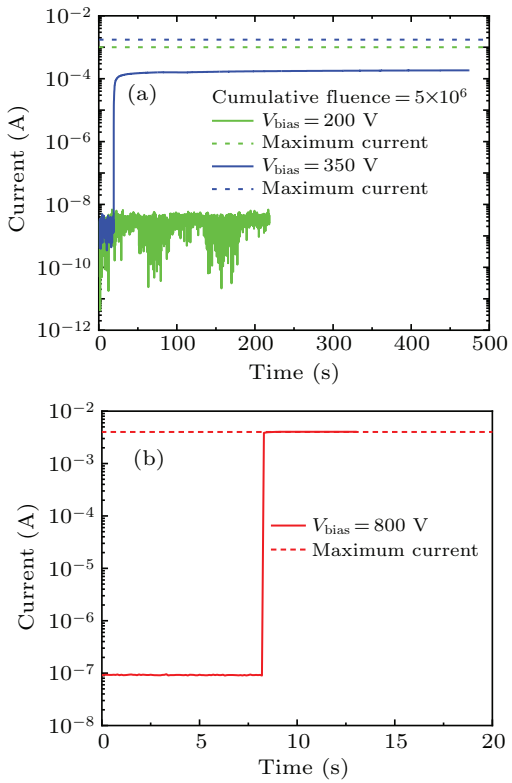


Fig. 2. Drain current change of the SiC MOSFET under different irradiation bias voltage (a) 200 V and 350 V; (b) 800 V.

As shown in Fig. 2(b), under the 800 V bias voltage, the current of the device increases instantaneously in a very short time after the ion beam is emitted, and the drain current reaches the limit current of the test circuit. At the same time, the voltage is completely transferred to the protection resistor, and the 200 kΩ protection resistor cannot protect the device. Use the oscilloscope to trigger and save the changes of the transient pulse current. The trigger voltage of the oscilloscope is adjusted with the change of the bias voltage, so as to ensure that the pulse current is captured and to avoid false triggering due to noise. Figure 3 shows the transient pulse current calculated from the voltage waveform captured across R_1 when SEB occurred in device under a bias voltage of 800 V. The resistance of the SiC MOSFET before irradiation is about 10 MΩ, and the resistance of the device after burnout is only 720 Ω. When the device burns out, the resistance of the drain electrode and gate–source electrodes of SiC MOSFET instantly drops from about 10 MΩ to a few hundred Ω, which causes the transient current of the device to rise instantaneously. However, due to the existence of the protection resistor, the transfer of the high voltage on the original device to the protection resistor is also a fast process. The combined action of the two processes results in a damped oscillation-like phenomenon in the transient pulse currents in the circuits we detected. As shown in Fig. 3, the pulse current is wave-shaped, and the maximum pulse current can reach about 20 A, and the pulse current width for the SiC MOSFET to burn out is on the order of microseconds. No device pulse current is captured at bias voltages of 200 V and 350 V.

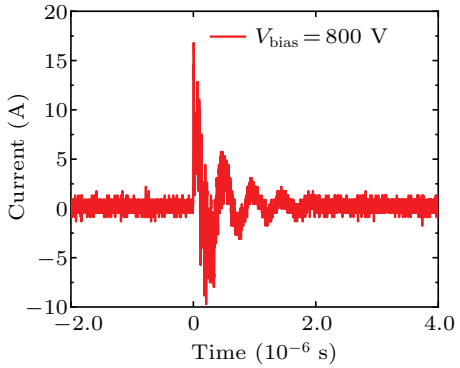


Fig. 3. Transient pulse current during SEB occurred in the SiC MOSFET.

3. Experiment results and discussion

3.1. Electrical characteristics test of irradiated SiC MOSFET

The devices have different degradations in the experiment, and the damage of the electrical performance after irradiation is also different. Figure 4 is the transfer characteristic curves of the device before and after the experiment under different bias voltages. As shown in Fig. 4(a), the bias voltage

and the accumulated ion fluence of irradiation of SiC MOSFET correspond to Fig. 2. When the gate voltage is 15 V, the gate current of the device with a bias voltage of 200 V in the experiment increases by at least 4 orders of magnitude. The gate current and the drain current are equal at the gate voltage of approximately 11 V when the experiment bias voltage of the device is 350 V, and the gate electrode and drain electrode are closed to the short circuit at this time as shown in Fig. 4(b). When the bias voltage is 800 V in Fig. 4(c), the gate current and the leakage current are significantly increased compared to the pre-irradiation when the gate voltage is less than the threshold voltage. After the channel is turned on, the gate current increases with the increase of the gate voltage, it is still at least one order of magnitude lower than that of the drain current.

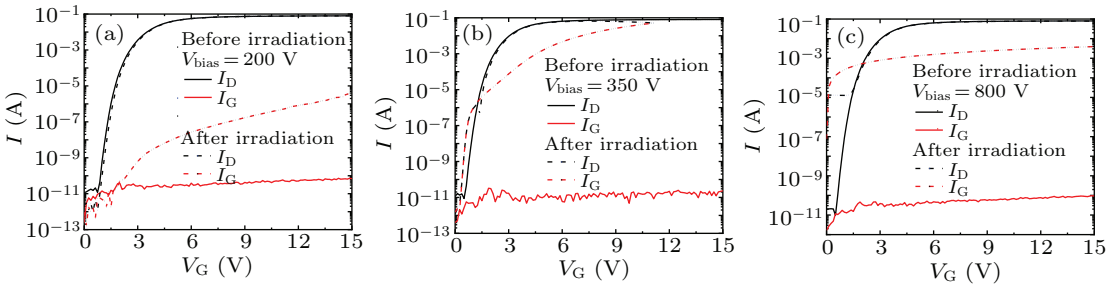


Fig. 4. The transfer characteristic curve of the SiC MOSFET under different bias voltage: (a) $V_{bias} = 200$ V. (b) $V_{bias} = 350$ V. (c) $V_{bias} = 800$ V.

The breakdown characteristic curves of the device under different irradiation bias voltages before and after irradiation are shown in Fig. 5. In Fig. 5(a), unlike the transfer characteristic, the gate current increases significantly with the increase of the gate voltage. When the gate voltage is 0 V, even if the drain voltage increases to 200 V, the degradation of the gate current is less than an order of magnitude. Combining Figs. 4(a) and 5(a), it can be found that the gate degradation of the device under the irradiation bias voltage of 200 V mainly results in current leakage in the gate–source channel, and the drain–gate channel is hardly affected. The electric field formed in the epitaxial layer by the irradiation at 200 V bias voltage is not enough to damage the drain–source channel. The gate oxide has a relatively high electric field strength at 200 V bias voltage, which may be the reason for the gate degradation. But because the gate and source are shorted to both voltages of 0 V, this also leads to no current change in the real-time current monitoring of the device with 200 V bias voltage, as shown in Fig. 2(a). When the irradiation bias voltage is 350 V, as shown in Fig. 5(b), the gate current degradation of the device gradually shows a consistent trend with the drain current degradation, but the damage does not lead to the complete loss of the device's breakdown characteristics. The damage of the gate oxide layer and the drain–source channel leads to the almost equal gate and drain currents before the channel is turned on as shown in Fig. 4(b), but after the channel is turned on, the drain–source channel becomes a low resistance channel and the drain current increases. But with the increase of gate voltage, the current of gate–source channel and gate–drain channel also increases sharply. This results in a near-short circuit of gate, drain and source when the gate voltage is 11 V in the transfer characteristic test, and finally the transfer test stops automatically when the gate voltage is 11 V.

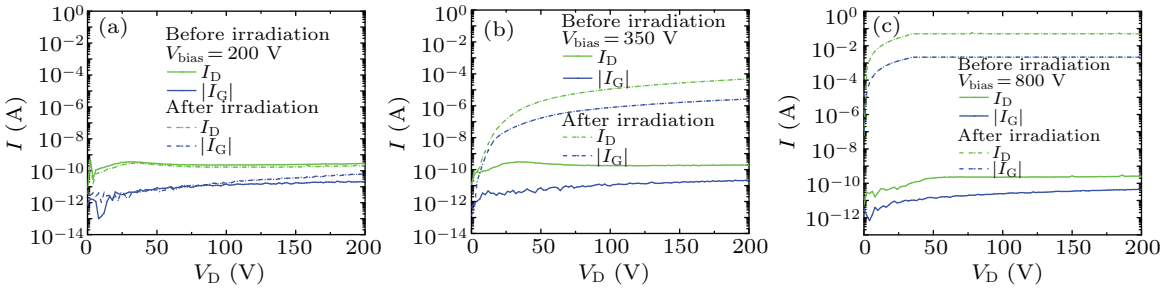


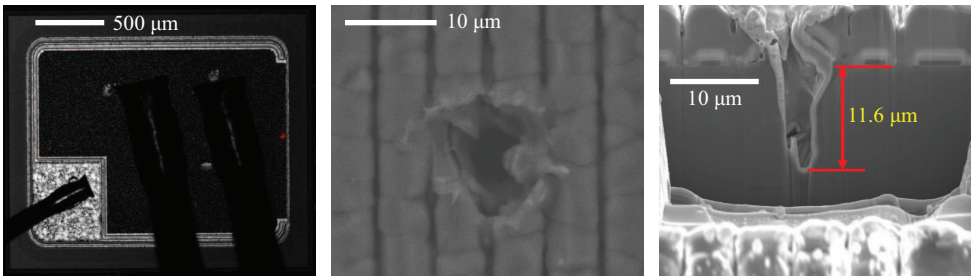
Fig. 5. The breakdown characteristic curve of the SiC MOSFET under different bias voltage: (a) $V_{bias} = 200$ V; (b) $V_{bias} = 350$ V; (c) $V_{bias} = 800$ V.

The SEB occurs in the device under the irradiation bias voltage of 800 V. As shown in Fig. 5(c), the drain current has reached the limit current at a very low drain voltage. According to the device datasheet, the drain voltage when the device drain current is equal to 0.1 mA is the breakdown voltage. The breakdown voltages of all devices before irradiation are in the range of 1100 V–1200 V. When the protection resistor R_0 is 200 kΩ, the device still maintains the breakdown voltage of

1007.5 V and 292.5 V under the bias voltage of 200 V and 350 V when the cumulative fluence reaches 5×10^6 ion·cm^{-2}, and the breakdown characteristics are degraded by 14% and 74%, respectively. The breakdown voltage of the device is lower than 1 V after the SEB occurred at a bias voltage of 800 V.

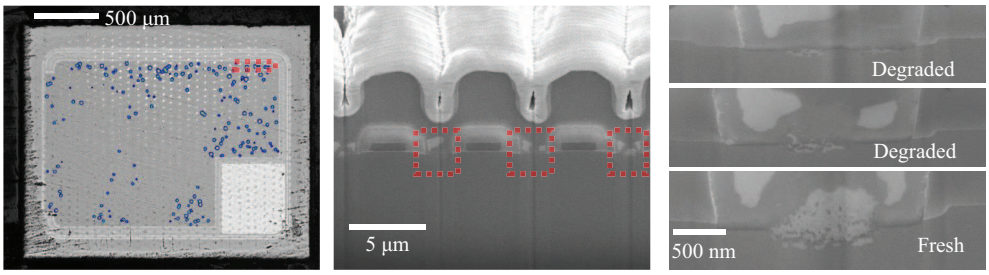
3.2. Location and microscopic analysis of device damage caused by heavy ions

Using EMMI to locate the SEB or SELC position of the SiC MOSFET, and then using SEM and FIB for microscopic analysis is an effective failure mechanism analysis method. In the EMMI test from the top of SiC MOSFET, only an obvious leakage point can be observed after the SEB occurred, as shown in Fig. 6(a). In the SEM and FIB analysis shown in Figs. 6(b) and 6(c), it is found that the SEB causes an obvious cavity on the surface of SiC MOSFET, and two closed SiC MOSFET cells are damaged. Usually, the thickness of the epitaxial layer of the SiC MOSFET with 1200 V rated voltage is considered to be about 10 μm.[17,22] As a commercial device, the epitaxial layer thickness of 900 V SiC MOSFET should not exceed 10 μm. It can be seen in Fig. 6(c) that the depth of the melting area of the device is slightly greater than 10 μm. The SEB of SiC MOSFET does not only affect the SiC material, the burnout region also contains the source metal, gate oxide layer, and the polysilicon gate electrode. However, the melting point of SiC is about 2900 K, which is higher than that of other materials. Combined with the burnout depth in SiC, we speculate that SEB started from SiC materials.



(a) EMMI (b) SEM (c) FIB-SEM

Fig. 6. Damage localization and analysis of SEB device: (a) EMMI; (b) SEM; (c) FIB-SEM. The experimental bias conditions of SEB device are LET = 70.2 MeV·cm^2·mg^{-1} and $V_{\rm bias}$ = 800 V.



(a) EMMI (b) SEM (c) FIB-SEM

Fig. 7. Damage localization and analysis of SELC device: (a) EMMI; (b) SEM; (c) FIB-SEM. The experimental bias conditions of the SELC device are LET = 70.2 MeV·cm^2·mg^{-1} and $V_{\rm bias}$ = 350 V.

Due to the presence of the source metal on the top of the SiC MOSFET, the location of SELC at 350 V bias voltage cannot be observed. Therefore, based on the light transmittance of the SiC material, we remove the bottom drain metal of the SiC MOSFET and then perform the EMMI test, as shown in Fig. 7(a). The drain voltage can no longer be applied, the gate voltage is applied for the test in the EMMI test. There is no leakage point in the bonding wire area in the middle of the chip and the gate pad area in the right corner. The bonding wire is too thick and heavy ions cannot penetrate, and the area covered by the bonding wire is not damaged. Under 350 V bias voltage, the cumulative fluence of the SiC MOSFET is 5×10^6 ion·cm^{-2}. After calculating to remove the bonding area and the gate pad area, the active area is about 0.013 cm^2, and the effective number of incident ions is 6.5×10^4. According to the results of the EMMI test, the damage of the gate–source channel does not occur with every incident of effective ions, and there may be some leakage positions caused by the drain–source channel. Likewise, we perform backside EMMI testing of the device with gate degradation at 200 V bias voltage, and find no leakage points. In the transfer characteristic test of Fig. 4(a), the gate current is only 3.9 μA when the gate voltage is 15 V, and we speculate that the gate leakage may be too small to be recognized in the EMMI test.

In the SEM and FIB analysis shown in Figs. 7(b) and 7(c), it is found that the device has local metal melting phenomenon at the source contact. The current degradation of the SiC diodes is believed to come from the lattice eutectic

where the metal electrode contacts the SiC or the local lattice melting of SiC.[18] In the case of short-circuit stress, obvious cracks appear in the gate oxide layer.[26] However, no cracks are found in the gate oxide layer of the SiC MOSFET with increased leakage current and gate damage. At the same time, only the pulse current during SEB will have a large current of fewer than 5 μs, which is significantly less than that of the large current of more than 10 μs under short-circuit stress. The degradation of the SiC MOSFET is different from that of short-circuit stress damage. Except for the obvious local metal contact melting in the source contact, heavy ion-induced damage of the gate oxide layer cannot be observed.

4. Simulation of single event effects caused by heavy ions

4.1. Heavy ion transport simulation

Monte Carlo simulations of heavy ion transport are carried out using GEANT4 software.[27,28] The Coulomb interaction between the incident ions and the device material is considered in the simulation, QGSP_BERT physics list and the high-precision electromagnetic model Option_4 are selected, which are the same as the physical process used in the GEANT4 simulations in Ref. [29]. The transport and energy deposition process of electrons with initial energy higher than 1 keV are considered in the simulation, and the energy deposition of electrons with initial energy less than 1 keV is calculated near the generation location. Using this model, the radial distribution of energy deposition at different incident depths can be calculated more accurately, so as to obtain accurate single event effect model parameters.

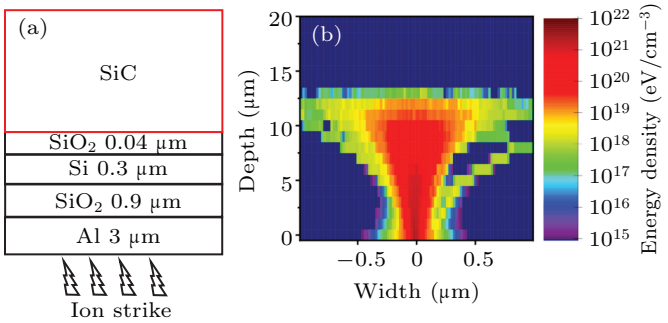


Fig. 8. The transport of 283 MeV I ion in the SiC MOSFET: (a) Monte Carlo simulation model diagram; (b) energy deposition density.

According to the structure of the SiC MOSFET, we construct the simulation model as shown in Fig. 8(a). Heavy ions pass through the source metal Al, SiO_2, Si, and SiO_2 oxide layer in turn, and finally enter SiC. The energy deposition density of I ion with an energy of 283 MeV in SiC is shown in Fig. 8(b). We calculate the total energy deposition of primary ions and secondary particles. The statistical step size of ion energy deposition in the incident direction is 1 μm, and the energy deposition density distribution is calculated and sorted for use in subsequent TCAD simulations. The maximum and minimum values of the Gaussian characteristic value for I ion energy deposition are 0.342 μm and 0.042 μm, and the time parameter for energy deposition is 1.8 ps.

4.2. TCAD simulation of SiC MOSFET

According to the results of the FIB analysis, we establish a TCAD model of the SiC MOSFET. In the TCAD simulation, we take into account the optimization of the mesh and the reduction of the calculation time, the distance of the Al metal from the top of the SiO_2 is 0.8 μm, and the gray part in the Fig. 9(a) is Al metal. The electrothermal characteristics of the SiC MOSFET are considered in the simulation. The related heat capacity, thermal resistance, and thermal conductivity parameters have been revised[21,30,31]

$$k(T) = \frac{611}{T-115}, \tag{1}$$

$$\chi(T) = a + bT + cT^2, \tag{2}$$

$$C_L = a + bT + cT^2 + dT^3, \tag{3}$$

where T is the lattice temperature of SiC. The relevant parameters used in the TCAD electrothermal simulation are shown in Table 1. The width of the device cell, the structure and material of the oxide layer and the gate electrode are obtained by FIB-SEM analysis, the thickness of the device epitaxial layer, and the doping and structure of each internal region are based on the model parameters of the 900 V SiC MOSFET in the Ref. [32] and the TCAD database.[33]

Table 1. Parameters for TCAD simulation.

Parameter	Value
N+ drain doping/depth	1×10^{19} cm^{-3}, 0.38 μm
P-based doping/depth	1×10^{18} cm^{3}, 0.81 μm
Epitaxial layer doping/depth	3×10^{15} cm^{-3}, 10 μm
Substrate doping/depth	6×10^{18} cm^{-3}, 180 μm
Thermal resistivity	$a=-0.18822$ cm·K/W, $b=1.6367\times10^{-3}$ cm/W, $c=-1.6941\times10^{-20}$ cm/(W·K)
Heat capacity	$a=1.5778$ J/(K·cm^3), $b=3.5332\times10^{-3}$ J/(K^2·cm^3), $c=-1.5447\times10^{-6}$ J/(K^3·cm^3), $d=2.6052\times10^{-10}$ J/(K^4·cm^3).

If the incident conditions of heavy ions are distinguished according to the different materials on the incident path, there are four different incident conditions when heavy ions are incident perpendicularly. Pos 1 means that heavy ions pass through the metal layer, polysilicon electrode, oxide layer, epitaxial layer, and finally enter the substrate. Pos 2 means that heavy ions enter the channel region after passing through the oxide layer, and then enter the epitaxial layer and the substrate in turn. Pos 3 means that heavy ions enter the SiC material and sequentially pass through the source region, p-type region, epitaxial layer, and finally enter the substrate. Pos 4 is where heavy ions pass through the metal layer directly into the

p-type region, and then into the epitaxial layer and the substrate in turn. As shown in Fig. 9(b), the simulation result of breakdown voltage based on the constructed TCAD model is 1180 V, which is consistent with the experimental test results.

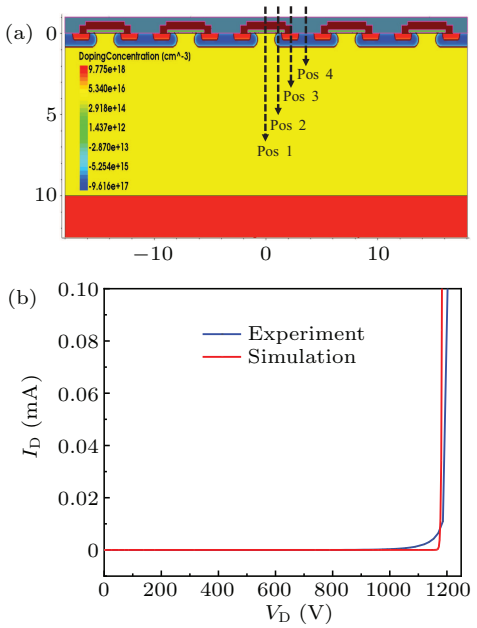


Fig. 9. TCAD simulation of the SiC MOSFET: (a) model structure diagram; (b) breakdown characteristics.

The single event effect model is constructed based on the Monte Carlo simulation results. The charge density induced by heavy ions exhibits a Gaussian distribution in the direction perpendicular to the ion track, and the ionization energy of SiC is about 7.8 eV. In the TCAD simulation, the temporal variations of the charge generation rate $T(t)$ and the charge generation rate $G(l,w,t)$ caused by the heavy ion are constructed respectively by[33]

$$T(t) = \frac{2\cdot\exp\left(-\left(\frac{t-t_0}{\sqrt{2}\cdot s_{\rm hi}}\right)^2\right)}{\sqrt{2}\cdot s_{\rm hi}\sqrt{\pi}\left(1+\mathrm{erf}\left(\frac{t_0}{\sqrt{2}\cdot s_{\rm hi}}\right)\right)}, \tag{4}$$

$$G(l,w,t) = G_{\rm LET}(l)R(w,t)T(t), \tag{5}$$

where t is the moment of the heavy ion penetration, and $s_{\rm hi}$ is the characteristic value of the Gaussian function. $R(w)$ describes the spatial variations of the generation rate. $G_{\rm LET}(l)$ is the linear energy transfer generation density and its unit is pairs/cm^3.

It is generally believed that the melting point of SiC is 2900 K–3100 K, and the critical temperature $T_{\rm c}$ of the SiC material in the simulation is set to 2900 K. The simulation stops when the lattice temperature of the SiC material reaches 2900 K. If the lattice temperature does not reach the critical burnout temperature, the simulation stops when the time reaches 1 μs. When I ions with an energy of 283 MeV are incident from four positions under 800 V bias voltage, the time and space distribution of the SiC MOSFET lattice temperature are shown in Figs. 10(a) and 10(b). Depending on the incident position, the substrate–epitaxial junction and the gate–source corner may be the initial burn-out position of the SiC MOSFET. The time at which the burnout occurs varies with the incident position. Except for pos 3, the burnt point of the incident position has the same abscissa as the incident position. When incident from pos 3, it means that heavy ions completely pass through the area where the current flows when the device is turned on. At the same time, the incident position is closed to the gate–source corner, which leads to drastic changes and concentration of current and electric field near the corners. However, due to the incomplete current path at the others three incident positions, there will be a large electric field at the gate–source corner in time, but the current is not large enough. The burnout finally occurs in the substrate–epitaxial junction where the electric field and current are locally excessive.

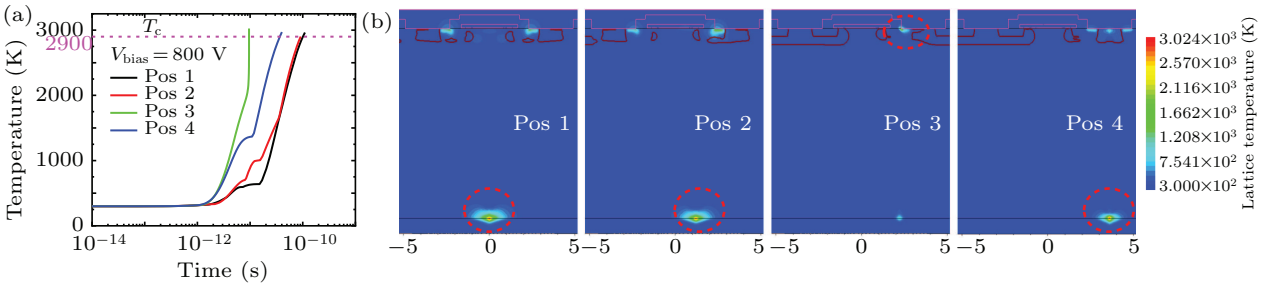


Fig. 10. The lattice temperature distribution of SiC devices when heavy ions are incident from different positions under 800 V bias voltage. (a) Time distribution. (b) Spatial distribution.

When heavy ions are incident from pos 4 under 800 V bias voltage, the lattice temperature, current density, electric field intensity, and power density of SiC MOSFET along with the incident depth are shown in Fig. 11. Combined with the FIB analysis results of the SiC MOSFET burnout point in Fig. 6, the burnout depth exceeds the thickness of the epitaxial layer, but only the critical lattice temperature exists near the substrate–epitaxial interface, so there are fewer burnt and melted parts in the substrate. The peak of current density and electric field appears on the interface at the same time, causing the device to dissipate too much power at the interface in a very short time and causing extreme lattice temperature. The

source contact position also has a larger electric field, but the current density is lower than that of the substrate–epitaxial interface, and the critical lattice temperature appears first at the substrate–epitaxial junction.

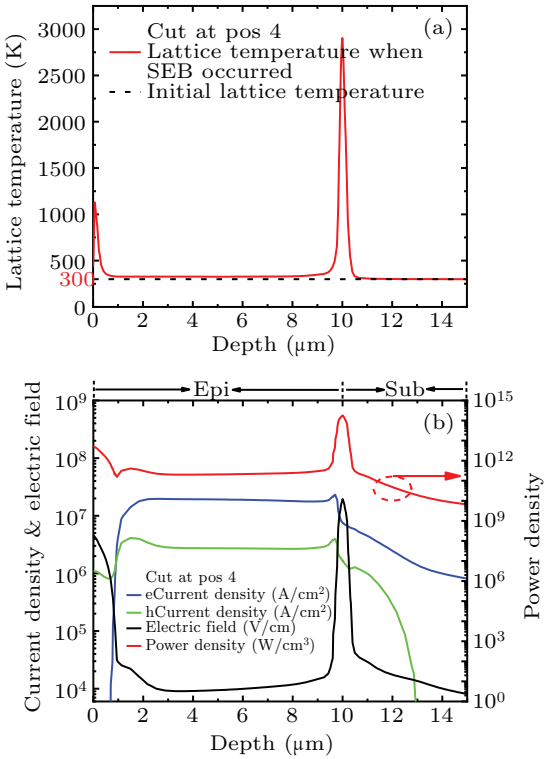


Fig. 11. The distribution of electrothermal parameters of the SiC MOSFET with depth: (a) lattice temperature; (b) current density, electric field intensity, and power density.

Figure 12 shows the temporal and spatial evolution of the electrothermal parameters of the SiC MOSFET for different incident positions under 350 V bias voltage. The variation of the peak electric field in the gate oxide layer is shown in Fig. 12(a). Reference [28] proposes that the threshold electric field E_c of gate oxide layer degradation is about 14 MV/cm, the cyan dotted line in Fig. 12(a) represents E_c, the field that causes the gate oxide layer degradation named the effective electric field. The electric field fluctuation of the gate oxide layer caused by the incidence of heavy ions from position 4 is significantly smaller than that of the others three positions, and the duration of the effective electric field when the heavy ions are incident from position 4 is about 2.81×10^{11} s. When the heavy ions are incident from the others three positions, there are certain differences in the duration of the effective electric field, but they are all more than twice the duration of the effective electric field corresponding to position 4. Combined with the EMMI results in Fig. 7(a), the entire active region of the device belongs to the SELC sensitive region. The size and brightness of the leakage spot in Fig. 7(a) represent the gate leakage current degree at this location, this is related to the incident position of heavy ions from the TCAD simulation results. Different incident positions lead to different changes in the electric field fluctuation of the gate oxide layer. The SiC MOSFET irradiated at 350 V bias voltage shows drain current increase in the real-time monitoring. Due to the difference in the incident positions, only two distinct lattice temperature peaks appear for the four typical incident positions with the movement of the charges. But in fact, three lattice temperature peaks appear in the device after the incidence of heavy ions. As shown in Fig. 12(c), taking pos 1 as an example, the first lattice temperature peak may appear at the SiC–gate oxide layer interface or SiC–source metal interface, depending on the location of the heavy ion incident. The second lattice temperature peak appears at the corners of SiO_2 due to the electric field concentration, and the third temperature peak appears at the junction between the substrate and the epitaxial layer due to the movement of charges and the difference in doping concentration. Although the temperature at the junction of the substrate and the epitaxial layer is relatively high, SiC itself has strong high temperature resistance. Combined with the EMMI test results of the irradiated device under 350 V bias voltage, the higher lattice temperature will cause the metal to melt at the contact between SiC and source electrode, and the electric field distribution inside the device under the drain bias voltage will be affected by the contact damage, resulting in increase of drain current and degradation of breakdown characteristics. The degradation of the gate oxide layer under the local high temperature and strong electric field also leads to the increase of gate current and drain current in the transfer and breakdown characteristics test. In the experiment, the area of the heavy ion source is larger than that of the chip area, which makes the degradation of the SiC interface and the gate oxide layer random, resulting in different stepped degradation of the drain current in real-time monitoring.

When the bias voltage is 200 V, since the gate and source are short-circuited and the current noise fluctuates greatly, the gate degradation is not found in real-time current monitoring. Fig. 13(a) shows the change of the peak electric field in the gate oxide layer with time. When the bias voltage is reduced from 350 V to 200 V, the peak electric field in the gate oxide formation decreases significantly under the same heavy-ion incident position, and the damage degree of the gate oxide layer may be weakened due to the decrease of the peak electric field. However, considering the effective electric field that causes the degradation of the device, except for position 4, when the heavy ions are incident from other positions, the duration of the effective electric field that causes the degradation of the gate oxide layer does not decrease. Due to the peak lattice temperature of SiC is less than half of its melting point, 200 V bias voltage is difficult to cause leakage current between the source and the drain, as shown in Fig. 13(b). The breakdown characteristic curve in Fig. 5(a) also shows that un-

der the 200 V drain bias voltage, the gate current increases by orders of magnitude. Although the gate current is only about 5 μA when the gate voltage is 15 V, the breakdown voltage of the SiC MOSFET has been reduced by about 14% under the cumulative heavy-ion fluence of 5×10^6 ion·cm^{-2}. It may also cause unacceptable effects on the SiC MOSFET once excessively high heavy ion fluences are accumulated at low bias voltages. And on the other hand, it is not conducive to the accurate estimation of the reliability of SiC MOSFET in the space environment.

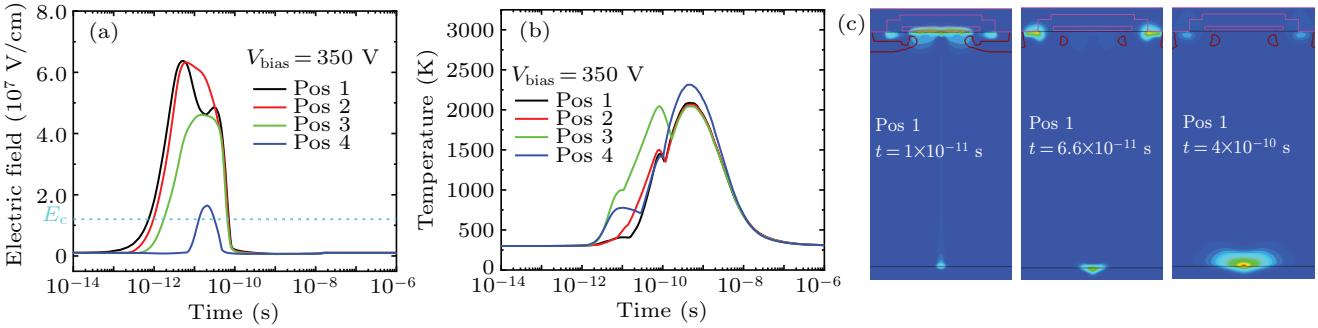


Fig. 12. The evolution of the electrothermal parameters of the SiC MOSFET when heavy ions are incident from different positions under 350 V bias voltage. (a) The peak electric field of the gate oxide layer. (b) Time distribution of lattice temperature. (c) Spatial distribution of lattice temperature.

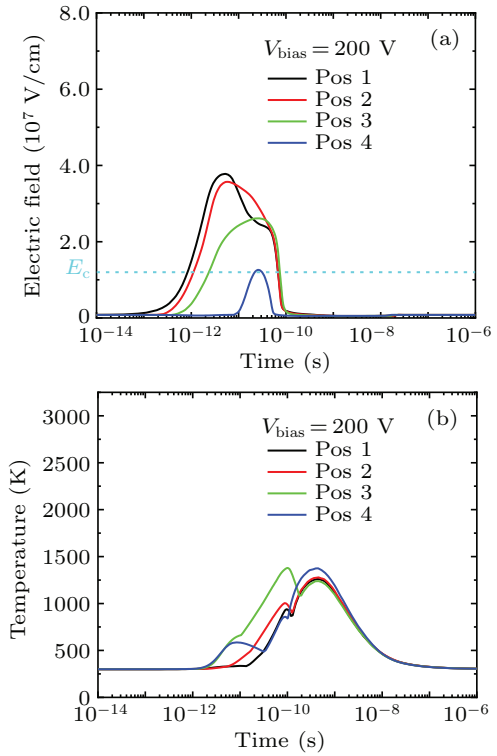


Fig. 13. The evolution of the electrothermal parameters of SiC MOSFET with time when heavy ions are incident from different positions under 200 V bias voltage. (a) The peak electric field of the gate oxide layer. (b) The lattice temperature.

5. Conclusion

The gate degradation, SELC and SEB of the SiC MOSFETs under 283 MeV I ion irradiation have been studied. When SEB appears in the SiC MOSFET under 800 V bias voltage, there will be accompanied by a transient pulse current on the order of amperes, and the pulse width is on the order of several microseconds. The SEB device still has a channel opening ability under a small drain voltage, but the breakdown characteristics are completely lost. The EMMI test can be used to locate the obvious SEB point in the SiC MOSFET. Under the 350 V bias voltage, the drain current of the device increases stepwise during the irradiation process, and there is no pulse current similar to SEB. The breakdown characteristic of the SELC device with 350 V bias voltage is degraded by about 74% under the heavy-ion fluence of 5×10^6 ion·cm^{-2}. In the EMMI test from the bottom of the chip, it is found that the device with SELC has gate–source leakage channels, but the number is significantly less than that of the effective ion fluence. In the SEM and FIB tests, it is found that part contact of the source metal and SiC melted. No degradation of the drain current is found under 200 V bias voltage, but the increase of gate current is found in the electrical characteristic test, and when the cumulative fluence is 5×10^6 ion·cm^{-2}, the drain–gate channel degradation causes about 14% degradation of the breakdown voltage.

The temporal and spatial distribution of energy deposition of 283 MeV I ions in SiC MOSFET using the Monte Carlo method are simulated and calculated. Using TCAD to simulate the degradation and burnout of the SiC MOSFET, both the source–gate corner and the substrate–epitaxial junction may be the initial burnout region, depending on where the heavy ions are incident. The simultaneous occurrence of high current density and large electric field in a local area causes the heat power to be unable and dissipated in time, and further causes excessively high lattice temperature. Under 350 V bias voltage, a higher lattice temperature appears at the interface of source metal and SiC. The lattice temperature does not reach the melting point of SiC but is sufficient to make the contact interface lattice eutectic. Further induce drain current increases at drain bias voltage. When the bias voltage is 200 V, the lattice temperature in SiC and the lattice temperature at the interface are further reduced, but there is still excessive electric field distribution in the gate oxide layer, which is enough to

cause gate degradation.

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