High performance carrier stored trench bipolar transistor with dual shielding structure

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We propose a novel high performance carrier stored trench bipolar transistor (CSTBT) with dual shielding structure (DSS-CSTBT). The proposed DSS-CSTBT features a double trench structure with different trench profiles in the surface, in which a shallow gate trench is shielded by a deep emitter trench and a thick oxide layer under it. Compared with the conventional CSTBT (con-CSTBT), the proposed DSS-CSTBT not only alleviates the negative impact of the shallow gate trench and highly doped CS layer on the breakdown voltage (BV), but also well reduces the gate-collector capacitance C_{GC}, gate charge Q_G, and turn-off loss E_{OFF} of the device. Furthermore, lower turn-on loss E_{ON} and gate drive loss E_{DR} are also obtained. Simulation results show that with the same CS layer doping concentration $N_{CS} = 1.5 \times 10^{16}$ cm^{-3}, the BV increases from 1312 V of the con-CSTBT to 1423 V of the proposed DSS-CSTBT with oxide layer thickness under gate (T_{og2}) of 1 μm. Moreover, compared with the con-CSTBT, the C_{GC} at V_{CE} of 25 V and miller plateau charge (Q_{GC}) for the proposed DSS-CSTBT with T_{og2} of 1 μm are reduced by 79.4% and 74.3%, respectively. With the V_{GE} increases from 0 V to 15 V, the total Q_G for the proposed DSS-CSTBT with T_{og2} of 1 μm is reduced by 49.5%. As a result, at the same on-state voltage drop (V_{CEON}) of 1.55 V, the E_{ON} and E_{OFF} are reduced from 20.3 mJ/cm^2 and 19.3 mJ/cm^2 for the con-CSTBT to 8.2 mJ/cm^2 and 9.7 mJ/cm^2 for the proposed DSS-CSTBT with T_{og2} of 1 μm, respectively. The proposed DSS-CSTBT not only significantly improves the trade-off relationship between the V_{CEON} and E_{OFF} but also greatly reduces the E_{ON}.

Keywords: carrier stored trench bipolar transistor (CSTBT), dual shielding structure, gate-collector capacitance, power loss

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1. Introduction

Insulated gate bipolar transistors (IGBTs) with trench gate and field stop (FS) layer (trench-FS IGBT) are one kind of mainstream IGBTs on markets. They are widely used in industrial control, electric vehicles and power supplies, etc.[1–3] To further improve the performance of devices, a carrier stored trench bipolar transistor (CSTBT) with an N-type carrier storage (N-CS) layer inserted between the P_{body} region and N-type drift region was proposed. During the forward conduction state, the highly doped N-CS layer forms a hole barrier between the N-CS layer and N-drift region, which improves the carrier concentration distribution and enhances the conductance modulation effect in the N-drift region.[4–6] Therefore, the trade-off relationship between the on-state voltage drop V_{CEON} and turn-off loss E_{OFF} is significantly improved.[7] However, the highly doped N-CS layer has negative impact on the breakdown voltage (BV). Meanwhile, the deep gate trench used in the CSTBT increases the gate-collector capacitance C_{GC}, which slows down the switching speed and increases the switch loss E_{OFF} as well as turn-on loss E_{ON}.[8–12] Therefore, to further improve the device performance, many improved CSTBT structures, such as p-type buried layer (PBL) structure, alternated trench IGBT with PBL structure, recessed emitter trench (RET) structure and split gate (SG) structure, have been proposed.[13–19] Although device performance is significantly improved for these structures, the contradiction between V_{CEON} and E_{OFF} for the CSTBT is still prominent, which limits the further reduction of the device power loss and improvement of the power density.

In this paper, a novel CSTBT with dual shielding structure (DSS-CSTBT) is proposed. Through simulation, the performance of the proposed DSS-CSTBT with different oxide layer thickness under gate (T_{og2}) is compared with the conventional CSTBT (con-CSTBT) in detail. In addition, the influence of the structure parameters on the device's static and dynamic performance is also compared and analyzed.

2. Device structure and mechanism

Figures 1(a) and 1(b) show the schematic cross-section view of the proposed DSS-CSTBT and con-CSTBT, respectively. Compared with the con-CSTBT, the proposed DSS-CSTBT features a double trench structure with different trench

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profiles in the surface, in which a shallow gate trench is shielded by a deep emitter trench and a thick oxide layer under it. The shallow gate trench of the proposed DSS-CSTBT is narrow and has a thick shielding oxide layer under it. Therefore, not only reduced C_{GC} and miller plateau charge Q_{GC} but also a smaller total gate charge Q_G are obtained, which improves the switching speed and reduces the E_{ON} and E_{OFF} of the device. Meanwhile, the deep and wide emitter trench acts as a vertical field plate and provides an electric field shielding effect on the highly doped N-CS layer and shallow gate trench. Then, an improved BV is obtained for the proposed DSS-CSTBT. In addition, the DSS decreases the area of the P_{body} region in the surface, which attenuates the extraction of holes from it. Therefore, it further improves the injection enhancement (IE) effect in the drift region, which alleviates the detrimental effect of the shallow trench gate on the forward conduction characteristics. As a result, the proposed DSS-CSTBT comprehensively improves the device performance and obtains a better trade-off relationship between the V_{CEON} and E_{OFF}.

Figures 2(a)–2(h) show a brief fabrication process flow for the proposed DSS-CSTBT. Compared with the con-CSTBT, two trench etching steps are used to form the double trenches of the proposed dual shielding structure. Utilizing the loading effect of the etching process, the first trench etching step is used to form the wide and deep emitter trench as well as narrow and shallow gate trench simultaneously. Then, a thick oxide layer is formed simultaneously in both the emitter trench and the gate trench by oxidizing and depositing. Especially, the gate trench is fully filled by the oxide layer due to its narrow width. After that, an additional trench etching step is used to form the thick oxide layer under the gate by etching the upper part of the oxide layer in the gate trench only. After the trench etching is completed, a gate oxide layer is re-formed on the sidewall of the gate trench by oxidation. The remaining process steps are fully compatible with the process flow of the con-CSTBT. Main device parameters used in the simulation are listed in Table 1.

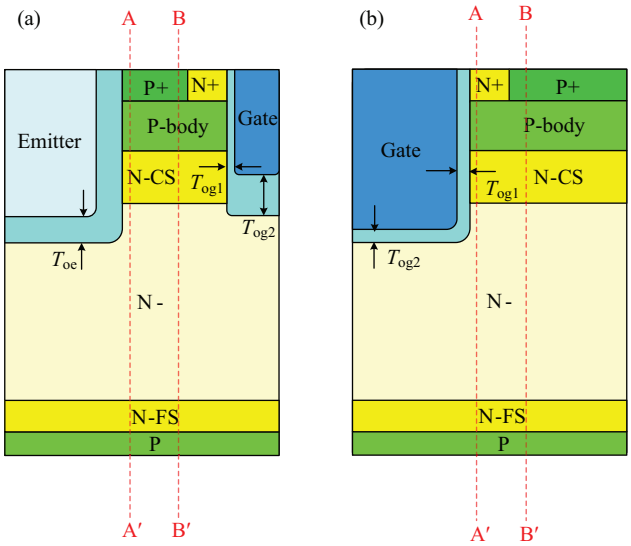


Fig. 1. Schematic cross-sectional views of (a) proposed DSS-CSTBT and (b) con-CSTBT.

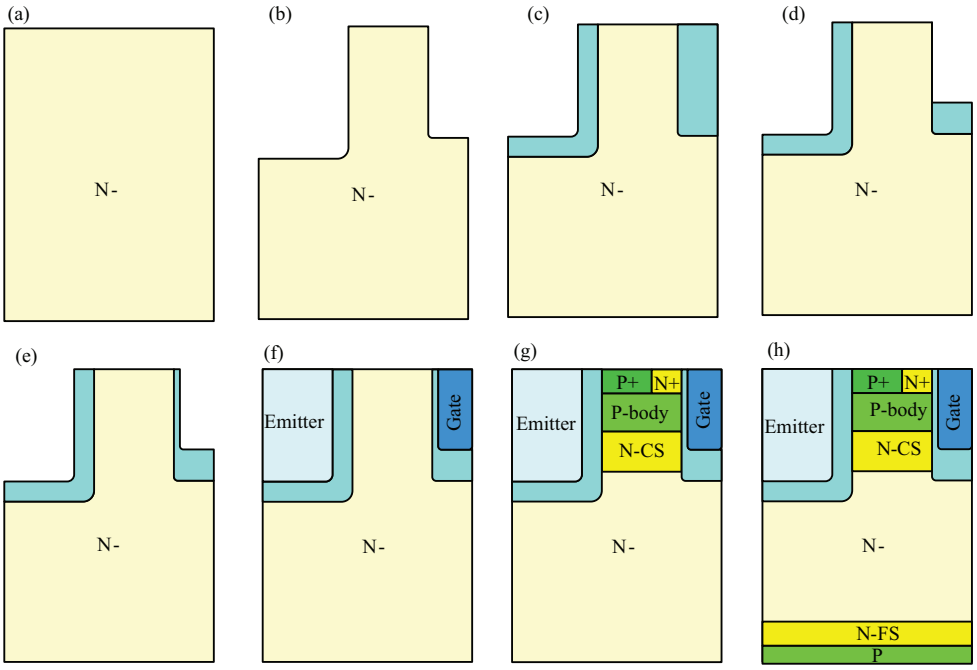


Fig. 2. Proposed brief fabrication process flow of the DSS-CSTBT: (a) select the N-type FZ substrate, (b) etch emitter and gate trenches simultaneously, (c) form thick oxide layer, (d) etch the upper part of the oxide layer in the gate trench, (e) form gate oxide layer on the sidewall of the gate trench, (f) fill trench with poly-silicon, (g) form the N-CS layer, P_{body}, N+ region, P+ region, and metal in surface, (h) form the backside structures.

Table 1. Main device parameters used in simulation.

Parameters	DSS-CSTBT	Con-CSTBT
Half-cell width (μm)	2	2
Gate trench width (μm)	0.4	0.7
Emitter trench width (μm)	0.7	/
N^+ emitter width (μm)	0.3	0.3
P-body width (μm)	0.9	1.3
Sidewall oxide layer thickness of gate, T_{og1} (μm)	0.1	0.1
Gate trench depth, T_{GT} (μm)	4	5
Oxide layer thickness under gate, T_{og2} (μm)	0.1–1	0.1
Emitter trench depth (μm)	5	/
Emitter oxide thickness, T_{oe} (μm)	0.4	/
P-body junction depth (μm)	1.5	1.5
CS layer junction depth (μm)	2	2
FS layer junction depth (μm)	4	4
P-body doping (cm^{-3})	1.5×10^{17}	1.5×10^{17}
CS layer doping (cm^{-3})	$1.5–3.5\times10^{16}$	1.5×10^{16}
N-drift doping (cm^{-3})	7×10^{13}	7×10^{13}
FS layer doping (cm^{-3})	2×10^{16}	2×10^{16}
P^+ collector doping (cm^{-3})	2×10^{17}	2×10^{17}

3. Results and discussion

Figure 3(a) shows the impact of the N_{CS} on the BV for the con-CSTBT and proposed DSS-CSTBTs with different emitter oxide layer thickness T_{oe}. In the simulation, the T_{og2} is kept same at 1 μm for the proposed DSS-CSTBTs. It can be seen that the BV of the proposed DSS-CSTBTs is larger than that of the con-CSTBT in a relatively large range of the N_{CS} owing to the shielding effect provided by the thicker T_{oe} and T_{og2}. As the T_{oe} of the proposed DSS-CSTBT increases, the shielding effect provided by the emitter trench is more obvious. Figure 3(b) shows the impact of the N_{CS} on the BV for the con-CSTBT and proposed DSS-CSTBTs with different T_{og2}. In the simulation, the gate trench depth T_{GT} and the T_{oe} are kept same at 4 μm and 0.4 μm for the proposed DSS-CSTBTs. It can be seen that in a relatively large range of the N_{CS}, the proposed DSS-CSTBTs all have a higher BV when compared with the con-CSTBT. The BVs for the proposed DSS-CSTBTs and con-CSTBT all decrease as the N_{CS} increases. With the same N_{CS} of 1.5×10^{16} cm^{-3}, the BV for the con-CSTBT is only 1312 V. However, the BV increases to 1427 V, 1435 V, and 1423 V for the proposed DSS-CSTBTs with the T_{og2} of 0.1 μm, 0.5 μm, and 1 μm, respectively. In the following discussion, the proposed DSS-CSTBTs with the T_{og2} of 0.1 μm, 0.5 μm, and 1 μm are referred to as the DSS-CSTBT1, DSS-CSTBT2, and DSS-CSTBT3, respectively. To obtain the similar BV of 1337 V, the N_{CS} can increase from 1.5×10^{16} cm^{-3} for the con-CSTBT to 3.5×10^{16} cm^{-3} for the proposed DSS-CSTBT3. Therefore, a higher N_{CS} can be adopted to maintain similar BV for the proposed DSS-CSTBT.

Figure 4 shows the vertical electric field distributions along the AA′ line at breakdown for the con-CSTBT and proposed DSS-CSTBTs, respectively. The N_{CS} used for all the devices is 1.5×10^{16} cm^{-3}. It can be seen that the proposed DSS-CSTBTs have smaller electric field peaks when compared with the con-CSTBT. This is due to the better shielding effect provided by the deep emitter trench with a thick oxide layer, which reduces the electric field crowding at the trench corner. For the proposed DSS-CSTBT with different T_{og2}, the vertical electric field distributions along the AA′ line keep almost no change.

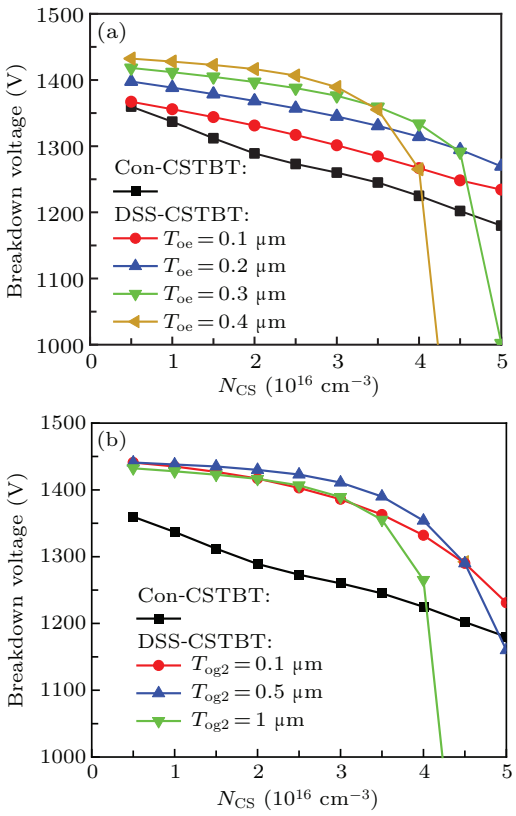


Fig. 3. Impact of the N_{CS} on the BV for the con-CSTBT and proposed DSS-CSTBTs with (a) T_{oe} and (b) T_{og2}.

Figure 5 shows effect of the N_{CS} on the V_{CEON} for the proposed DSS-CSTBTs and con-CSTBT. It can be seen that with the increase of the N_{CS}, the V_{CEON} decreases for all the devices. The V_{CEON} of all the three DSS-CSTBTs are lower than that of

the con-CSTBT when the N_{CS} is greater than 1×10^{16} cm^{-3}. As the N_{CS} increases, the proposed DSS-CSTBTs have more obvious advantages.

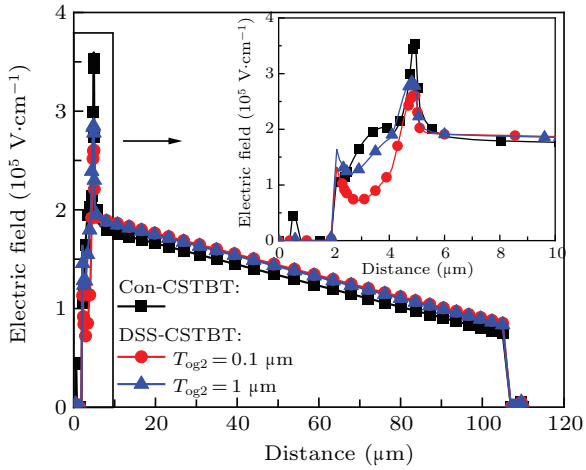


Fig. 4. Vertical electric field distributions at breakdown for the proposed DSS-CSTBTs and con-CSTBT along the AA′ line.

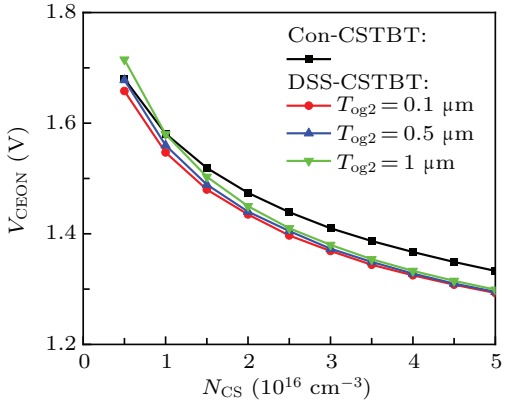


Fig. 5. Effect of the N_{CS} on the V_{CEON} for the proposed DSS-CSTBTs and con-CSTBT.

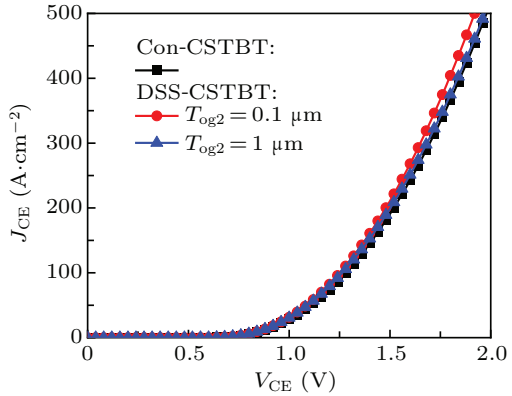


Fig. 6. Simulated *I*–*V* characteristics for the proposed DSS-CSTBTs and con-CSTBT at the same J_{CE} of 200 A/cm^2.

Figure 6 shows comparison of the *I*–*V* characteristics for these devices with the N_{CS} of 1.5×10^{16} cm^{-3}. At the same collector current density J_{CE} = 200 A/cm^2, the V_{CEON} values for the con-CSTBT, the proposed DSS-CSTBT1, and DSS-CSTBT3 are 1.52 V, 1.48 V, and 1.50 V, respectively. It can be seen that the V_{CEON} for the proposed DSS-CSTBTs is slightly smaller than that of the con-CSTBT. It can also be seen that with the increase of the T_{og2}, the V_{CEON} for the proposed DSS-CSTBT slightly increases. The reason is that with the same T_{GT}, the increase of the T_{og2} reduces the gate electrode depth, which reduces the electron accumulation around the gate area when the device is in forward conduction state. Figure 7 shows the on-state electron concentration distribution along the BB′ line for these devices. Since the hole has similar distribution as that of the electron owing to the conduction modulation in the drift region, only the electron concentration is drawn in the figure. It can be seen that at J_{CE} = 200 A/cm^2, the proposed DSS-CSTBTs have a higher carrier distribution at the emitter side of the drift region, which results in a lower V_{CEON}.

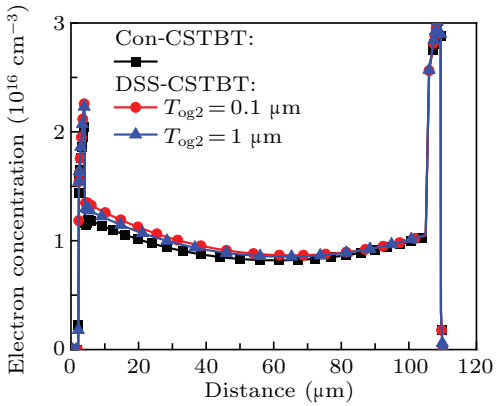


Fig. 7. On-state electron concentration distribution along BB′ line for the proposed DSS-CSTBTs and con-CSTBT at the same J_{CE} of 200 A/cm^2.

Figure 8 shows simulated characteristics of the C_{GC} for the con-CSTBT and proposed DSS-CSTBTs with different T_{og2}, respectively. It can be seen that contributed by the shallow and narrow gate electrode, the C_{GC} values of the proposed DSS-CSTBTs are much smaller than that of the con-CSTBT owing to the reduced coupling area between the gate and collector. At V_{CE} = 25 V, the C_{GC} of the proposed DSS-CSTBT3 is 79.4% lower than that of the con-CSTBT. Meanwhile, a lower C_{GC} is obtained for the proposed DSS-CSTBT with a thicker T_{og2}. This is due to the reduction of the gate electrode depth and enhanced shielding from the thicker oxide layer. Figure 9 shows simulated characteristics of the Q_G and Q_{GC} for these devices. It can be seen that during the process of V_{GE} rising from 0 V to 15 V, the total Q_G for the con-CSTBT is 1744 nC/cm^2. However, for the proposed DSS-CSTBT1 and DSS-CSTBT3, it is only 1244 nC/cm^2 and 880 nC/cm^2, respectively. When compared with the con-CSTBT, the total Q_G is decreased by 28.7% and 49.5%, respectively. In addition, the Q_{GC} is reduced from 721 nC/cm^2 for the con-CSTBT to 415 nC/cm^2 and 185 nC/cm^2 for the proposed DSS-CSTBT1 and DSS-CSTBT3, respectively. Compared with the con-CSTBT, the Q_{GC} is reduced by 42.4% and 74.3%, respectively. Because of the reduction of gate capacitance, especially

the reduction of C_{GC}, the proposed DSS-CSTBT greatly reduces the Q_G and Q_{GC}. Therefore, the proposed device can greatly improve the switching speed.

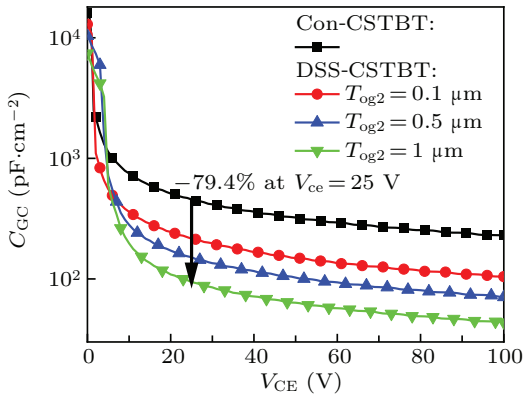


Fig. 8. Simulated characteristics of the C_{GC} for different devices.

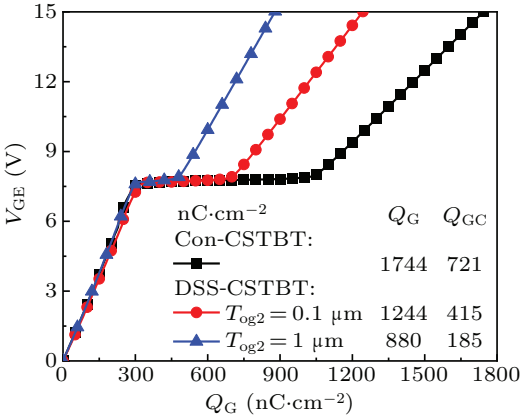


Fig. 9. Simulated characteristics of the Q_G and Q_{GC} for different devices during the process of V_{GE} rising from 0 V to 15 V.

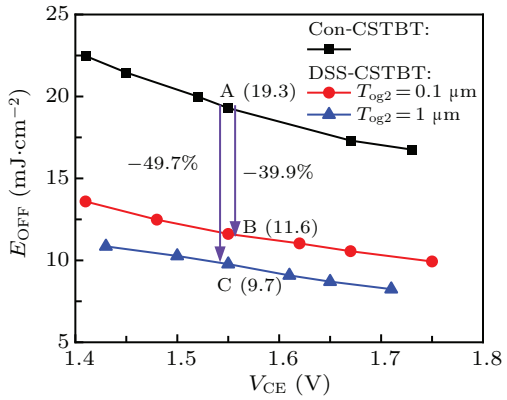


Fig. 10. Trade off relationship between V_{CEON} and E_{OFF} for different devices.

Figure 10 shows simulated trade-off relationship between the V_{CEON} and E_{OFF} for different devices. The results are obtained by using a clamped inductive load circuit and changing the collector doping concentration P_c. At the same V_{CEON} of 1.55 V, the E_{OFF} values for the con-CSTBT, the proposed DSS-CSTBT1, and DSS-CSTBT3 are 19.3 mJ/cm^2, 11.6 mJ/cm^2, and 9.7 mJ/cm^2, respectively. Compared with the con-CSTBT, the E_{OFF} values for the proposed DSS-CSTBT1 and DSS-CSTBT3 are reduced by 39.9% and 49.7%, respectively. Therefore, the proposed DSS-CSTBT demonstrates a better V_{CEON}–E_{OFF} trade-off relationship. It also can be found that a better V_{CEON}–E_{OFF} trade-off relationship can be obtained for the proposed DSS-CSTBT with a thicker T_{og2}. The reason is that although the V_{CEON} is slightly increased when the T_{og2} increases, the Q_G and C_{GC} are significantly reduced. Therefore, the proposed DSS-CSTBT with a thicker T_{og2} has a faster switching speed and smaller E_{OFF}.

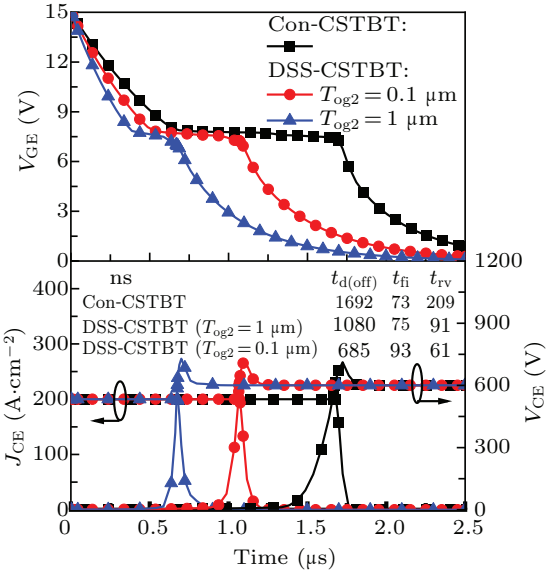


Fig. 11. Comparison of the gate turn-off voltage waveforms as well as collector turn-off current and voltage waveforms for the points A, B, and C shown in Fig. 10.

Figure 11 shows comparison of the turn-off characteristics of different devices for the points A, B, and C shown in Fig. 10. In order to keep the same V_{CEON} of 1.55 V, the P_c values for the con-CSTBT, proposed DSS-CSTBT1, and DSS-CSTBT3 are 1.9×10^{17} cm^{-3}, 1.7×10^{17} cm^{-3}, and 1.8×10^{17} cm^{-3}, respectively. It can be seen that owing to the reductions of Q_{GC} and Q_G, the gate of the proposed DSS-CSTBT discharges faster than that of the con-CSTBT, which is aligned with the result shown in Fig. 9. It can also be found that the turn-off delay time $t_{d(off)}$ for the con-CSTBT is 1692 ns, while the $t_{d(off)}$ values for the proposed DSS-CSTBT1 and DSS-CSTBT3 are 1080 ns and 685 ns only. Meanwhile, the current fall times t_{fi} for the con-CSTBT, the proposed DSS-CSTBT1, and DSS-CSTBT3 are 73 ns, 75 ns, and 93 ns, respectively. The voltage rise time t_{rv} is reduced from 209 ns of the con-CSTBT to 91 ns and 61 ns of the proposed DSS-CSTBT1 and DSS-CSTBT3, respectively. The result shows that the proposed DSS-CSTBT has a fast switching speed during the turn-off process, which contributes a smaller E_{OFF}. Figure 12 shows comparison of the dissipated power density P_{OFF} for the points A, B and C shown in Fig. 10 during turn-off process. The E_{OFF} is contributed by two phases, namely voltage rise phase ($E_{V,OFF}$) and current drop phase ($E_{I,OFF}$). It can be seen that the $E_{V,OFF}$ is reduced from 14.2 mJ/cm^2 for the con-CSTBT to 6.6 mJ/cm^2

and 4.6 mJ/cm^2 for the proposed DSS-CSTBT1 and DSS-CSTBT3, respectively. The $E_{\mathrm{I,OFF}}$ values for the con-CSTBT, proposed DSS-CSTBT1, and DSS-CSTBT3 are 5.1 mJ/cm^2, 5 mJ/cm^2, and 5.1 mJ/cm^2, respectively. Therefore, it can be seen clearly that compared with the con-CSTBT, the smaller $E_{\mathrm{V,OFF}}$ obtained for the proposed DSS-CSTBTs contributes to a smaller E_{OFF}. The smaller $E_{\mathrm{V,OFF}}$ is derived from the reduction of the Q_{GC}, which improves the voltage rise rate during turn-off process.

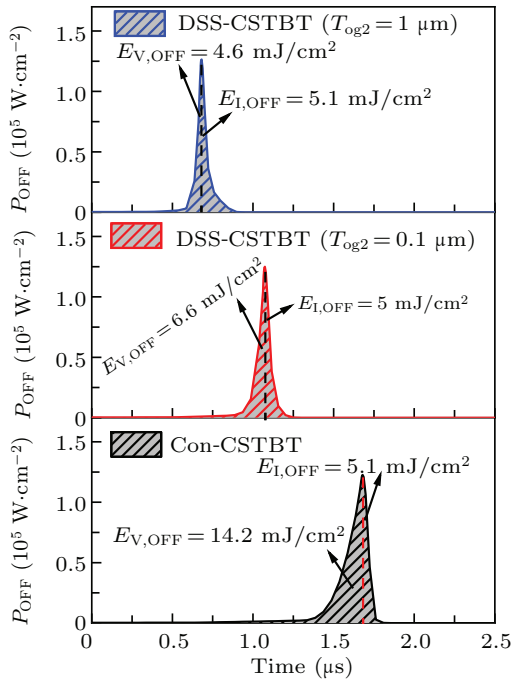


Fig. 12. Dissipated power density for the points A, B and C shown in Fig. 10 during the turn-off process.

Figure 13 shows the E_{ON}, E_{OFF} and gate drive loss E_{DR} of these devices at the same V_{CEON} of 1.55 V. Considering the impact of the freewheeling diode on the turn-on characteristics of the IGBTs, a well-designed fast recovery PiN diode is used in the simulation. As shown in the figure, the E_{ON} and E_{OFF} are 20.3 mJ/cm^2 and 19.3 mJ/cm^2 for the con-CSTBT. Noticeably, the E_{ON} and E_{OFF} for the proposed DSS-CSTBT1 are 11.7 mJ/cm^2 and 11.6 mJ/cm^2, and those for the proposed DSS-CSTBT3 are only 8.2 mJ/cm^2 and 9.7 mJ/cm^2, respectively. Furthermore, the E_{DR} is also reduced from 17.7 μJ/cm^2 for the con-CSTBT to 12.7 μJ/cm^2 and 9.2 μJ/cm^2 for the proposed DSS-CSTBT1 and DSS-CSTBT3, respectively. As a result, the proposed DSS-CSTBT not only reduces the E_{ON} and E_{OFF} during the switching process, but also obtains a low E_{DR}, which reduces the drive capability requirement for the gate driver. Furthermore, with the increasing T_{og2}, the E_{ON}, E_{OFF}, and E_{DR} are all reduced significantly, which obviously decreases the loss of device operation.

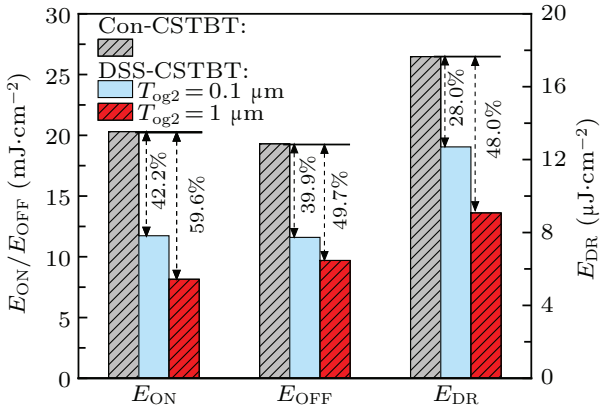


Fig. 13. The E_{ON}, E_{OFF}, and E_{DR} of different devices under the same $V_{\mathrm{CEON}}=1.55$ V.

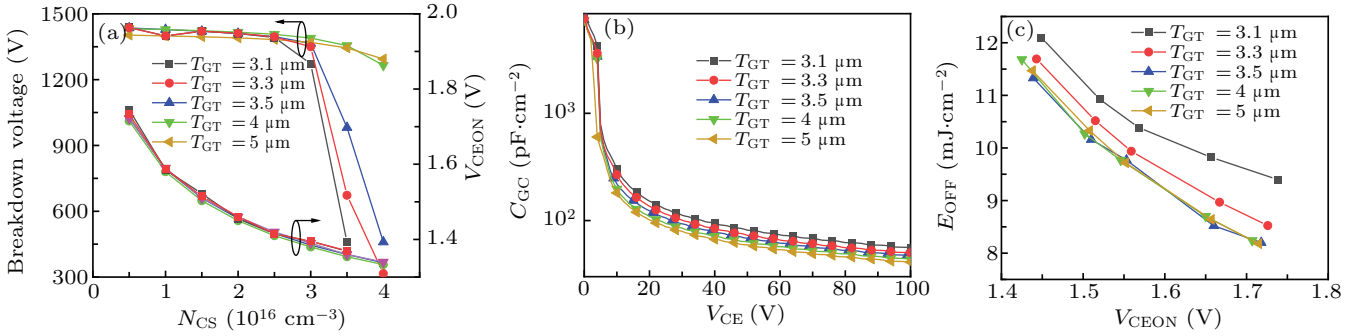


Fig. 14. Influence of gate trench depth on (a) BV and V_{CEON}, (b) C_{GC} and (c) the trade-off relationship between E_{OFF} and V_{CEON} for the proposed DSS-CSTBT.

Figure 14 shows influence of the T_{GT} on electrical characteristics of the proposed DSS-CSTBT. In the simulation, the gate electrode depth is kept same at 3 μm and the different T_{GT} means the change of the T_{og2}. It can be seen from Fig. 14(a) that the BV decline rate is faster with the decrease of the T_{GT} after the N_{CS} larger than a certain value. The proposed DSS-CSTBT with thicker T_{og2} can remain a relatively stable BV in a relatively large range of N_{CS}. This is due to the enhanced shielding effect provided by DSS, which reduces the electric field crowding at the trench corner. As for the forward conduction characteristics, the V_{CEON} for the proposed DSS-CSTBT is slightly increased with the increase of the T_{GT}. It can be found from Fig. 14(b) that the C_{GC} for the proposed DSS-CSTBT is decreased with the increase of T_{GT}, which is due to a

better shielding effect provided by the thick T_{og2}. Figure 14(c) shows the trade-off relationship between the V_{CEON} and E_{OFF} for the proposed DSS-CSTBT. It can be seen that the V_{CEON}–E_{OFF} trade-off relationship is significantly improved when T_{GT} increases from 3.1 μm to 3.5 μm. With the T_{GT} further increases to 5 μm, the improvement of the V_{CEON}–E_{OFF} trade-off relationship gradually achieves saturation since the C_{GC} is lower enough, and the displacement capacitance derived from the excess carriers in the drift region during the turn-off process becomes important.

4. Conclusion

In summary, we have proposed and analyzed a novel high performance DSS-CSTBT. Simulation results show that owing to the shielding effect provided by the DSS, the proposed DSS-CSTBT not only demonstrates a higher BV than the con-CSTBT at the same N_{CS} but also well reduces the C_{GC} and Q_G of the devices. Compared with the con-CSTBT, the C_{GC} at V_{CE} of 25 V and Q_{GC} for the proposed DSS-CSTBT are reduced by 79.4% and 74.3%, respectively. With the V_{GE} increasing from 0 V to 15 V, the total Q_G for the proposed DSS-CSTBT is reduced by 49.5%. As a result, at the same V_{CEON} of 1.55 V, the E_{ON} and E_{OFF} are reduced from 20.3 mJ/cm^2 and 19.3 mJ/cm^2 for the con-CSTBT to 8.2 mJ/cm^2 and 9.7 mJ/cm^2 for the proposed DSS-CSTBT, respectively. Moreover, the E_{DR} is also reduced from 17.7 μJ/cm^2 for the con-CSTBT to 12.7 μJ/cm^2 and 9.2 μJ/cm^2 for the proposed DSS-CSTBT1 and DSS-CSTBT3, respectively. Thus, the proposed DSS-CSTBT not only significantly improves the trade-off relationship between the V_{CEON} and E_{OFF} but also greatly reduces the E_{ON} and E_{DR}.

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