An insulated-gate bipolar transistor model based on the finite-volume charge method

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A finite-volume charge method has been proposed to simulate PIN diodes and insulated-gate bipolar transistor (IGBT) devices using SPICE simulators by extending the lumped-charge method. The new method assumes local quasi-neutrality in the undepleted N^- base region and uses the total collector current, the nodal hole density and voltage as the basic quantities. In SPICE implementation, it makes clear and accurate definitions of three kinds of nodes — the carrier density nodes, the voltage nodes and the current generator nodes — in the undepleted N^- base region. It uses central finite difference to approximate electron and hole current generators and sets up the current continuity equation in a control volume for every carrier density node in the undepleted N^- base region. It is easy to increase the number of nodes to describe the fast spatially varying carrier density in transient processes. We use this method to simulate IGBT devices in SPICE simulators and get a good agreement with technology computer-aided design simulations.

Keywords: finite-volume charge method, IGBT device, lumped charge method, SPICE simulation, TCAD simulation

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1. Introduction

Many models of PIN diodes and insulated-gate bipolar transistor (IGBT) devices have been proposed in the last several years to simulate power converter switching processes in circuits. Accurate and reliable device models can speed power circuit design and verification. So far, much effort has been made to develop and improve SPICE models of PIN diodes and IGBT devices from many aspects.[1–3] Hefner has developed a charge-control IGBT model based on the steady-state charge carrier distribution in the N^- base region of a PIN diode.[4,5] Kraus *et al.* developed another charge-control model based on a polynomial approximation of the partial time derivative of the charge carrier distribution.[6] The advantage of charge-control models is that only a few physical quantities are used to describe the behavior of power devices. The disadvantage is their lower accuracy due to the adoption of many simplifying approximations and the inability to adapt to different switching processes.[7]

Multiple-node methods such as the finite difference (FD) method,[8,9] the finite element (FEM) method[10] and the lumped charge (LC) method,[11,12] discretize the N^- base region into several small parts in real space and solve the proper equations accurately. The Fourier series (FS) method is also a multiple-node method.[13,14] It expands the excess carrier density into several discrete components in wave vector space. These methods have a better tradeoff between accuracy and cost, and can be solved in circuit form either by MATLAB Simulink or SPICE simulators. Usually these multiple-node methods also adopt many approximations such as local quasi-neutrality and the one-dimensional (1D) approximation to describe the carrier dynamics in the undepleted N^- base region. It is important to adopt more practical device conditions and more accurate approximations in device model development.

Lu *et al.* included a two-dimensional (2D) correction to the boundary carrier density of the undepleted N^- base region in the emitter–base junction side in IGBT devices using the FS method.[15] They obtained a better agreement between the simulation and experiments. Kang *et al.* implemented the FS method in a SPICE simulator to simulate a punch-through IGBT device with a N^+ buffer.[16] They made a diffusion approximation for the hole current in the N^+ buffer. As the n-type doping is only about 10^{16} cm^{-3} in the N^+ buffer, the electric field cannot be ignored and the drift current component can be comparable to the diffusion current component. We find this is the case through technology computer-aided design (TCAD) simulation. It is better if a model of an IGBT device has the same transport description in both the N^- base region and the N^+ buffer. Due to the adoption of a limited number of wave vectors in the expansion, the FS method cannot describe the abrupt change of physical quantities very well. This method can be implemented in either MATLAB Simulink or SPICE simulators. In a Simulink simulation, complicated program charts need to be drawn.[14] In a SPICE simulation, it is necessary to make the summations over many wave vectors and to transform the carrier density from wave vector space to real space, resulting in very complicated equations. In these respects, the real space methods, such as FD and LC methods, have more advantages. On the other hand, FD and LC methods

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also share another problem. For example, in FD and LC methods, the spatial partial derivatives are approximated by the FD formula. During fast switching processes, the width of the depletion layer of the emitter–base pn junction changes, thus a moving grid is needed to discretize the base region. A direct adoption of the moving nodes to build the FD formula will cause an artificial loss of the carrier number during fast switching processes. Recently we proposed using the compensation electron and hole current components to conserve the carrier number in the FD method.[9] The compensation current components are proportional to the moving speed of the boundary of the undepleted N^- base region and the average carrier density in this region. It is expected that such a correction is necessary in the LC method too. The FEM method does not use the FD replacement, but its equations are only valid under the condition of fixed boundaries of the undepleted N^- base region,[10] so in this method it is also necessary to correct the effect of the moving boundaries. The FS method does not have this problem.[13,14] In this method, the boundary positions of the undepleted N^- base region are determined by the boundary carrier densities through high-gain feedback controllers in SPICE simulations.[3]

The FD method is based on the ambipolar transport equation with a constant high injection carrier lifetime.[8,9] In contrast, the LC method is based on the drift–diffusion model.[11,12] It can use a density-dependent carrier lifetime, which is more accurate at a low injection level.[17] A further investigation of characteristics of the LC method is very useful. In the following we will analyze the main points and limitations of this method. We propose a new extension for this method, which we call the finite-volume charge (FVC) method.

2. Theoretical models

2.1. The FVC method versus the LC method

Figure 1(a) shows a punch-through IGBT structure. It has a thick N^- base region with a donor doping level between 10^{13} cm^{-3} and 10^{14} cm^{-3} and a thin N^+ buffer layer with a donor doping level of about 10^{16} cm^{-3}. Without the N^+ buffer layer, the structure is called a non-punch-through type. As shown in Fig. 1(b), an IGBT device is functionally equivalent to connecting the drain of an n-channel metal–oxide–semiconductor field-effect transistor (NMOSFET) to the base of a PNP bipolar transistor through a resistance-varying resistor R_n. It is noted that the names of the IGBT collector and emitter terminals are opposite to those terminals of the PNP device. There are two pn junctions: the base–collector junction (denoted as J_1) and the base–emitter junction (denoted as J_2). In the on-state of the IGBT device, J_1 is forward biased and J_2 is reverse biased. Injecting a lot of electrons and holes into the N^- base changes R_n. Region I is the drain region of the NMOSFET and works as a junction field effect transistor (JFET). Electron and hole current components in this region are mostly 2D. In the base region (II) they are mostly along the x-direction apart from near the boundary between regions I and II. Currently most IGBT models make the 1D approximation in the x-direction. The drain terminal of the NMOSFET is assumed to be on the line of $x = W$. The electron current through the channel region of the NMOSFET and region I is approximated using an empirical formula. Junction J_2 is assumed to extend to the whole range of L along the y-direction. The electron and hole density are assumed to be zero at the depletion layer boundary $x = W$ of the reverse-biased J_2 in Hefner's IGBT model.[5]

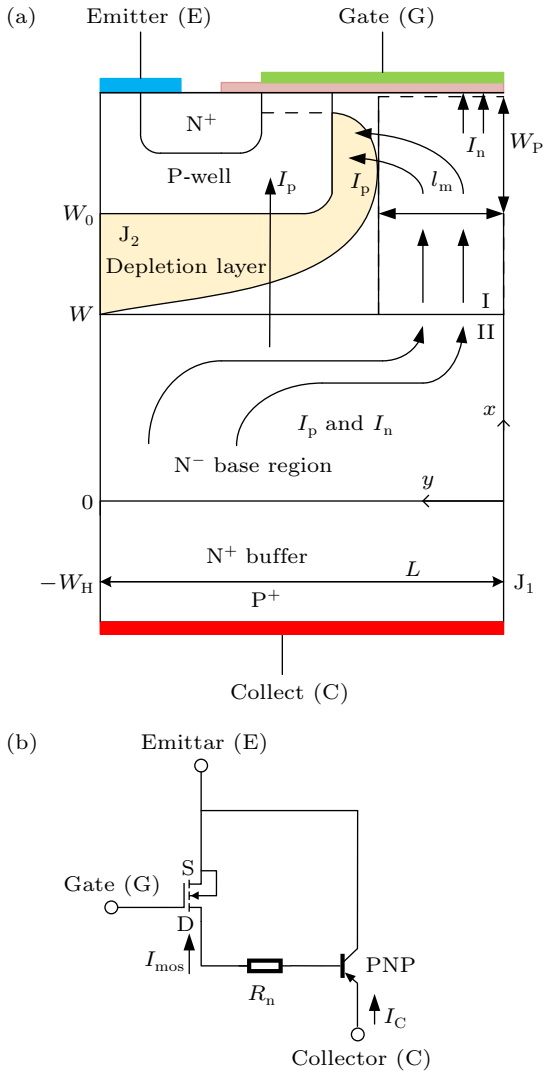


Fig. 1. (a) Schematic electron and hole current flows in a punch-through IGBT structure. (b) The equivalent circuit.

Taking a non-punch-through IGBT device as an example, in the 1D approximation in the x-direction the electron and hole current in the locally quasi-neutral N^- base can be written as

$$I_n = qA\mu_n \left[(p + N_B) E + V_T \frac{dp}{dx} \right], \tag{1a}$$

$$I_{\rm p} = qA\mu_{\rm p}\left(pE - V_{\rm T}\frac{{\rm d}p}{{\rm d}x}\right). \tag{1b}$$

Here $p(x,t)$ is the hole density, which is approximately equal to the excess hole density, E is the electric field, $V_{\rm T}$ is the thermal voltage, A is the cross-sectional area of the N^- base and $N_{\rm B}$ is the donor doping level in the base region. In order to use Eq. (1), Ma *et al.* employed three discrete lumped-charge nodes in the undepleted N^- base region.[11] In Fig. 2(a), nodes 2, 3, and 4 are equally spaced with a neighboring distance of $d/2$ in the undepleted N^- base region of a non-punch-through IGBT structure. The geometry is rotated by 90° with respect to that shown in Fig. 1(a). The symbol d has the same meaning as W in Fig. 1(a). There is also one more node across the depletion layer of the pn junction in each side: node 1 across J_1 on the left side and node 5 across J_2 on the right side. The hole carrier densities at the three nodes in the base region are p_2, p_3, and p_4, respectively. The corresponding lumped charges at these three nodes are defined as $q_{p_2} = qAdp_2$, $q_{p_3} = qAdp_3$, and $q_{p_4} = qAdp_4$. The electron and hole current components between nodes 2 and 3 are approximated as

$$\begin{aligned} I_{n_{23}} &\approx qA\mu_{\rm n}\left[(p_3 + N_{\rm B})\frac{v_{23}}{d/2} - V_{\rm T}\frac{p_2 - p_3}{d/2}\right] \\ &\approx \frac{(q_{p_3} + Q_{\rm M})v_{23}}{T_{n_{23}}V_{\rm T}} - \frac{(q_{p_2} - q_{p_3})}{T_{n_{23}}}, \end{aligned} \tag{2a}$$

$$\begin{aligned} I_{p_{23}} &\approx qA\mu_{\rm p}\left(p_3\frac{v_{23}}{d/2} + V_{\rm T}\frac{p_2 - p_3}{d/2}\right) \\ &\approx \frac{q_{p_3}v_{23}}{T_{p_{23}}V_{\rm T}} + \frac{(q_{p_2} - q_{p_3})}{T_{p_{23}}}. \end{aligned} \tag{2b}$$

These electron and hole currents are called current generators in SPICE circuits. In Eq. (2), $Q_{\rm M}$, $T_{n_{23}}$ and $T_{p_{23}}$ are defined as $Q_{\rm M} = qAdN_{\rm B}$, $T_{n_{23}} = (d^2/2)/(\mu_{\rm n}V_{\rm T})$, and $T_{p_{23}} = (d^2/2)/(\mu_{\rm p}V_{\rm T})$, respectively. In the LC method, $T_{n_{23}}$ and $T_{p_{23}}$ are respectively called the electron and hole transit times between nodes 2 and 3. The voltages at nodes 2 and 3 are v_2 and v_3 with the definition $v_{23} = v_2 - v_3$. Between node 3 and node 4, we can write similar equations for electron and hole current generators. The current continuity equation for charge conservation is given by

$$I_{\rm cont,3} = I_{p_{23}} - I_{p_{34}} = \frac{{\rm d}q_{p_3}}{{\rm d}t} + \frac{q_{p_3} - Q_{\rm m}}{\tau_{\rm B}}, \tag{3}$$

where $\tau_{\rm B}$ is the high-injection carrier lifetime in the base and $Q_{\rm m}$ is the total equilibrium minority hole density in the N^- base region defined as $Q_{\rm m} = qAdn_{\rm i}^2/N_{\rm B}$. We use $W_{\rm dep1}$ and $W_{\rm dep2}$ to denote the depletion layer widths of J_1 and J_2, respectively. The currents from Eq. (2) are assumed to be constant between adjacent nodes and not to be position dependent. No current continuity equation is set up for either of the carrier densities p_2 and p_4.

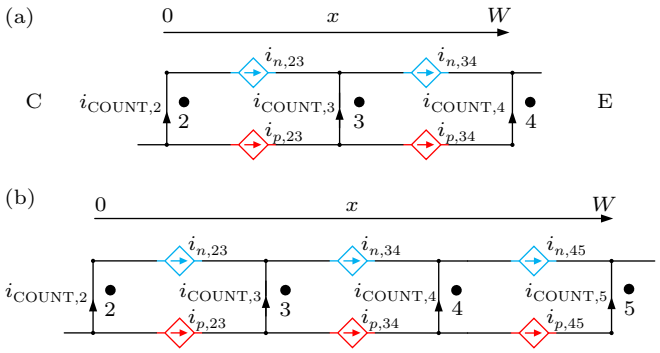


Fig. 2. (a) The scheme of conventional[12] and (b) the improved lumped charge methods.[18] Only nodes in the N^- base are shown.

Iannuzzo *et al.* have implemented the LC method in the form of a SPICE circuit.[12] The circuit shown in Fig. 2(a) has a hole current branch and an electron current branch. For each space discretization node there is one hole circuit node and one electron circuit node at two sides of the current generator $I_{{\rm cont},k}$ in the SPICE circuit. For voltage nodes, vertical $I_{{\rm cont},k}$ current generators are replaced by vertical shorts to keep the vertically connected nodes at the same voltage. When the pn junction J_1 between nodes 1 and 2 is forward biased, the current generator $I_{\rm cont,1}$ is given by[18]

$$I_{\rm cont,2} = AJ_{\rm sne}\left(\exp\left(\frac{V_{j12}}{V_{\rm T}}\right) - 1\right) + \frac{{\rm d}Q_{d_2}}{{\rm d}t}. \tag{4}$$

The first term describes the minority electron recombination in the left P^+ region in the collector. The second term describes carrier storage in the N^- region related to the diffusion capacitance. It is expressed by[18]

$$Q_{d_2} = \frac{Aqn_{\rm i}^2}{N_{\rm B}}\sqrt{D_{\rm p}\tau_{\rm p}}\exp\left(\frac{V_{j12}}{V_{\rm T}}\right). \tag{5}$$

This is a textbook equation for minority carrier injection in a long diode at a low injection level. Here Q_{d_2} actually describes the hole injection into the N^- region and the local charge neutrality means ${\rm d}Q_{d_2}/{\rm d}t$ also gives the change of stored electrons in the N^- region. For node 4, equations similar to Eqs. (4) and (5) can be written down with another term of carrier storage Q_{d_4}. Charges Q_{d_2}, q_{p_3}, and Q_{d_4} describe stored charges in the N^- region and have a double counting problem. The minority carrier diffusion length in Eq. (5) may be replaced by a fitting parameter. The total stored charge is not accurately described in this approximation.

Duan *et al.* tried to improve Eq. (3) by adding another space discretization node (Fig. 2(b)) in the undepleted N^- base region.[18] In this case, nodes 2, 3, 4, and 5 are equally spaced nodes with a distance of $d/3$. Here $d = W$ is the width of the undepleted N^- base region. There is also one more node across the pn junction depletion layer in each side: node 1 across J_1 on the left side and node 6 across J_2 on the right side. The hole densities at nodes 2 to 5 are p_2, p_3, p_4, and

p_5, respectively. The current generators $I_{n_{23}}/I_{p_{23}}$ and $I_{n_{34}}/I_{p_{34}}$ are assumed at nodes 3 and 4, respectively. Duan *et al.* used three current continuity equations for regions 2 to 3, 3 to 4, and 4 to 5. The number of current continuity equations is still smaller than the total number of lumped charge nodes in the undepleted N^- base region. Although they achieved very good agreement between experimental data and simulation results,[18] their improved LC method also introduced many different kinds of quantities and thus the method is complicated.

Our careful analysis of the LC method finds that it can be improved by the following points:

(i) Except for current generators from pn junctions at two boundaries, it is better to define and compute the electron and hole current generators only at the middle of two neighboring nodes. Figure 3(a) shows our discretization in the N^- base of a non-punch-through IGBT device. Space discretization nodes are labelled as n_1, n_2, n_3, n_4 and start from n_1 in the N^- base region. Nodes n_2 and n_3 are equivalent and their number can be easily increased if needed. In the following we assume the total number of nodes in the undepleted N^- base is N. Node n_1 on the top starts from the collector side, the last node n_N at the bottom is at the emitter side. For each index k, both the nodal voltage v_k and the nodal carrier density p_k are define at node n_k. We define $2N$ variables as the basic quantities of an IGBT device. They are the nodal voltage difference $v_{k+1}-v_k$, the nodal carrier density p_k and the total collector current I_C. A detailed analysis shows that with a given V_{GE} these basic quantities fully determine the state of the IGBT device. Functions of these basic quantities can be used to express other quantities such as the electron or hole current components in the N^- region and the voltage drops across two pn junctions in an IGBT device; these are also called generators in our SPICE circuits. The current generator nodes are only at $n_{I_1}, n_{I_2}, \ldots, n_{I_{N+1}}$. For example, for node n_{I_3} between nodes n_2 and n_3 we have

$$I_{n_{23}} \approx qA\mu_n \left[\frac{(p_2+p_3+2N_B)}{2}\frac{v_2-v_3}{\Delta x} - V_T\frac{p_2-p_3}{\Delta x}\right], \quad (6a)$$

$$I_{p_{23}} \approx qA\mu_p \left[\frac{(p_2+p_3)}{2}\frac{v_2-v_3}{\Delta x} + V_T\frac{p_2-p_3}{\Delta x}\right]. \quad (6b)$$

Here Δx is the distance between n_2 and n_3. The electric field E and $\mathrm{d}p/\mathrm{d}x$ are both computed as the central finite difference. The electron and hole current generators I_{n_1} and I_{p_1} at the position $n_{1-\delta}$, I_{n_N}, and I_{p_N} at the position $n_{N+\delta}$ are computed from the device physics. The symbol $n_{1-\delta}$ denotes a position slightly above node n_1 and the symbol $n_{N+\delta}$ denotes a position slightly below node n_N. The recombination current I_{n_1} of minority electrons and the hole current I_{p_1} in the p-type collector are expressed as

$$I_{n_1} = qAh_p p_1(p_1+N_B), \quad (7a)$$

$$I_{p_1} = I_C - I_{n_1}. \quad (7b)$$

Here I_C is the total collector current. The equations for I_{n_N} and I_{p_N} are complicated and will be given later. All current generators will form a SPICE current circuit in the SPICE simulation.

(ii) In contrast to the LC method, the carrier density at two boundary sides p_1 and p_N should also fulfill the current continuity equations, so it is necessary to choose the control volumes properly to apply the current continuity equations. Figure 3(a) shows our choice of control volume. Its size at two boundaries is chosen as $\Delta x/2$ and at all central places is chosen as the dimension of Δx. The nodal carrier density and the control volume have a one-to-one correspondence. The following current continuity equations can be written for the boundary node n_1 (similarly for n_N) and n_2 (similarly for other nodes):

$$I_{p_1} - I_{p_{12}} = qA\frac{\Delta x}{2}\left[\frac{\mathrm{d}p_1}{\mathrm{d}t} + \frac{(p_1-p_m)}{\tau_B}\right], \quad (8a)$$

$$I_{p_{12}} - I_{p_{23}} = qA\Delta x\left[\frac{\mathrm{d}p_2}{\mathrm{d}t} + \frac{(p_2-p_m)}{\tau_B}\right]. \quad (8b)$$

Here $I_{pn_1n_2}$ and $I_{pn_2n_3}$ are computed at current generator nodes n_{I_1} and n_{I_2}, respectively. $p_m = n_i^2/N_B$ is the equilibrium minority hole density in the N^- base region. In the whole control volume, the total current is a constant, but the electron and hole current components I_n and I_p have no definition except at the current generator nodes. In Fig. 3, all current generators are drawn in diamond symbols. Between the current generators expressed by diamond symbols dashed lines are plotted to indicate that only the total current is meaningful there. Eq. (8) will be converted into a SPICE circuit.

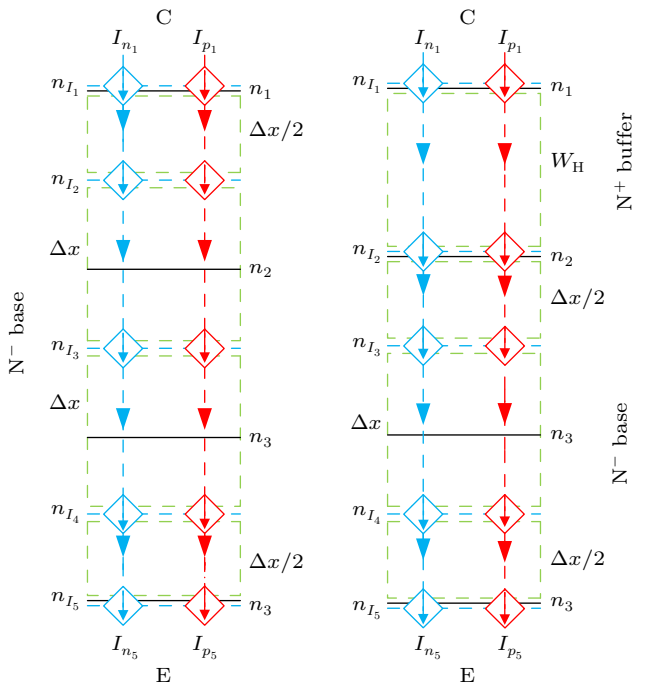


Fig. 3. The carrier density nodes, current generator nodes and control volumes in the FVC method: (a) a non-punch-through IGBT, (b) a punch-through IGBT.

(iii) The collector–base pn junction J_1 is assumed to have the forward conduction, so the change in its depletion layer thickness will be ignored. The emitter–base pn junction J_2 is reverse biased and the change in its the depletion layer width is controlled by a high-gain feedback controller[3]

$$W_{\rm dep2} = -K \times \min(p_N, 0). \tag{9}$$

Here K is an empirical constant. The feedback keeps p_N to a small negative value. The change of $W_{\rm dep2}$ results in a change in the width of the undepleted N^- base region. In the LC model, the reverse bias across J_2 is given by Eq. (10a)[12]

$$V_{J_2} = \begin{cases} -(C_{J_2}|_{1V} \min(qp_N d, 0))^2, & (10a) \\ -K \times (\min(p_N, 0))^2, & (10b) \\ K \times \min(p_N, 0). & (10c) \end{cases}$$

Here $C_{J_2}|_{1V} = [q\varepsilon_{\rm Si} N_{\rm B}/2(V_{\rm bi} - V_{J_2})]^{1/2}$ is the barrier capacitance of J_2 by setting $V_{\rm bi} - V_{J_2} = 1$ V. $q_{p_N} \equiv qdp_N$ is the lumped charge at node N in the LC model. Equation (10a) is not a physical equation but an artificial feedback controller similar to Eq. (9). It can be written as the form of Eq. (10b) with K as an empirical constant. The feedback controllers in Eqs. (9) and (10c) have been used in the FD and FS simulation approaches of PIN diodes before.[9,14] Equations (9) and (10) are equivalent to each other. Other forms of feedback controller are also possible.

(iv) Figure 3(b) shows a punch-through IGBT device with a N^+ buffer with a doping level $N_{\rm H}$, a width $W_{\rm H}$ and a high injection carrier lifetime $\tau_{\rm H}$. At node n_2, at the interface between the N^+ buffer and the N^- base, the voltage v_2 is continuous, but the carrier density is not continuous. Therefore, node n_2 for the carrier density is split into two nodes: n_{2h} in the N^+ buffer side and n_{2l} in the N^- base side. Nodes n_{2h} and n_{2l} can also be expressed as $n_{2+\delta}$ and $n_{2-\delta}$.

The carrier densities at these two nodes connected by

$$p_{2l}(p_{2l} + N_{\rm B}) = p_{2h}(p_{2h} + N_{\rm H}). \tag{11}$$

Here p_{2l} and p_{2h} are the carrier densities at nodes n_{2l} and n_{2h}, respectively. $N_{\rm B}$ in Eq. (7) is replaced by $N_{\rm H}$ in the punch-through IGBT device.

At the middle of the N^+ buffer, we define the current generators as

$$I_{n_{12}} \approx qA\mu_{n_{\rm H}} \left[\frac{(p_1 + p_{2h} + 2N_{\rm H})}{2} \frac{v_{12}}{W_{\rm H}/2} - V_{\rm T} \frac{p_1 - p_{2h}}{W_{\rm H}/2} \right], \tag{12a}$$

$$I_{p_{12}} \approx qA\mu_{p_{\rm H}} \left[\frac{(p_1 + p_{2h})}{2} \frac{v_{12}}{W_{\rm H}/2} + V_{\rm T} \frac{p_1 - p_{2h}}{W_{\rm H}/2} \right]. \tag{12b}$$

We can transform both current generators from the middle of the N^+ buffer to node n_{2h}

$$I_{n_12} \approx qA\mu_{n_{\rm H}} \left[\frac{(p_1 + p_{2h} + 2N_{\rm H})}{2} \frac{v_{12}}{W_{\rm H}/2} - V_{\rm T} \frac{p_1 - p_{2h}}{W_{\rm H}/2} \right] + qA \frac{W_{\rm H}}{4} \left(\frac{{\rm d}p_1}{{\rm d}t} + \frac{{\rm d}p_{2h}}{{\rm d}t} \right), \tag{13a}$$

$$I_{p_{12}} \approx qA\mu_{p_{\rm H}} \left[\frac{(p_1 + p_{2h})}{2} \frac{v_{12}}{W_{\rm H}/2} + V_{\rm T} \frac{p_1 - p_{2h}}{W_{\rm H}/2} \right] - qA \frac{W_{\rm H}}{4} \left(\frac{{\rm d}p_1}{{\rm d}t} + \frac{{\rm d}p_{2h}}{{\rm d}t} \right). \tag{13b}$$

In deriving these equations, the carrier number in the N^+ buffer is assumed to be $AW_{\rm H}(p_1 + p_{2h})/2$. Current generators in Eqs. (6) and (13) are assumed to be between nodes n_1 and n_2, so the total current equals the sum of electron and hole current generators in Eqs. (12) or (13) from nodes n_1 to n_2. This point is useful for establishing the SPICE simulation circuit. With Eq. (13), the charge current continuity equation can be written as

$$I_{p_1} - I_{p_{12}} = qAW_{\rm H} \left[\frac{{\rm d}p_1}{{\rm d}t} + \frac{(p_1 - p_{\rm mH})}{\tau_{\rm H}} \right], \tag{14a}$$

$$I_{p_{12}} - I_{p_{23}} = qA \frac{\Delta x}{2} \left[\frac{{\rm d}p_{2l}}{{\rm d}t} + \frac{(p_{2l} - p_{\rm m})}{\tau_{\rm B}} \right], \tag{14b}$$

$$I_{p_{23}} - I_{p_{34}} = qA\Delta x \left[\frac{{\rm d}p_3}{{\rm d}t} + \frac{(p_3 - p_{\rm m})}{\tau_{\rm B}} \right]. \tag{14c}$$

Here $I_{p_{23}}$ and $I_{n_{23}}$ are defined at the middle of node n_{2l} and n_3. $p_{\rm mH} = n_{\rm i}^2/N_{\rm H}$ is the equilibrium minority hole density in the N^+ buffer. $\tau_{\rm H} = \tau_{\rm B} = \tau_{\rm p} + \tau_{\rm n} = 13$ μs is chosen as the high-injection lifetime in both the N^- base and the N^+ buffer. The definitions of other current generators follow Eq. (6) and Fig. 3(a). Other choices of control volume for n_1 and n_2 are also possible. For example, if choosing Eq. (12) as the current generator in the N^+ buffer one can take the top half of the N^+ buffer as the control volume for n_1 and the bottom half of the N^+ buffer plus a small part of the N^- base region with a dimension of $\Delta x/2$ below node n_{2l} as the control volume for n_2. The resultant current continuity equation for node n_2 will be slightly complicated, but our tests show the results are almost the same.

(v) Finally, we also include the compensation electron and hole current corrections at node N due to the change of $W_{\rm dep2}$ in transient processes. Such corrections are important for fast switching PIN diodes.

With the above improvements, the new scheme can be thought as an extension of the LC method or better as the FVC method. Carrier conservation is fulfilled much better by the present choice of the positions of current generators and the control volumes. In addition, only the total collector current, the nodal carrier density and voltage are chosen as basic quantities in the new scheme. In the following we will compare the TCAD simulations of an IGBT device with SPICE simulations based on the new method.

2.2. SPICE circuit implementation of the FVC method

Figure 4 shows our SPICE current circuit implementation of the FVC method in a punch-through IGBT. E_j and E_{ds} are two voltage generators across the depletion layers of the collector–base and emitter–base pn junctions, respectively. E_j is connected between node C and n_1 giving $E_j = v_1 - v_C$, E_{ds} is connected between $n_N = d$ and node $E = s$ giving $E_{ds} = v_d - v_E$. Here d and s are the drain and source terminals of the NMOSFET in the IGBT device. The symbol d is the width of the undepleted N^- base region only in the LC method. The electron and hole current through E_j are I_{n_1} and I_{p_1}. E_j is given by the following equation:

$$E_j = 2V_T \ln\left(\frac{p_1}{n_i} + 1\right). \tag{15}$$

The nodes equivalent to n_3 can be increased. As discussed above, the total current I_C is constant between two neighboring voltage nodes. It is expressed as the sum of the local electron and hole current generators. Each voltage node is also connected to the ground through a large resistor, for example, 100 MΩ. This makes every voltage node have a DC pass to the ground. The definition of the voltage-controlled source V_{dep} is the same as in the LC method.[18]

The electron current at node $d = n_N$ is

$$\begin{aligned} I_{nd} &= \frac{\varepsilon_{Si}(A - A_{gd})}{x_{dep0} + W_{dep2}} \frac{dV_{ds}}{dt} + I_{mos}(V_{gs}, V_{ds}) \\ &\quad + A_{gd} C_{gd} \frac{dV_{dg}}{dt} + qA\overline{p} \frac{dW_{dep2}}{dt}, \end{aligned} \tag{16a}$$

$$I_{pd} = I_C - I_{nd}. \tag{16b}$$

Here x_{dep} is the zero-bias depletion layer width of the emitter–base pn junction J_2. $I_{mos}(V_{gs}, V_{ds})$ is the DC channel current in the NMOSFET. Figure 1(a) shows schematically the electron and hole current flows in a 2D TCAD IGBT structure. In this figure, we have $W - W_0 = x_{dep0} + W_{dep2}$. A is the cross-sectional area of an IGBT cell in the y–z plane and A_{gd} is the area of the gate overlapping with the drain. In Fig. 4 the current flow is approximated as a 1D one. The third term of I_{nd} in Eq. (16) is a displacement current in the drain and the capacitance C_{gd} is not a constant but depends on V_{dg}. In the real implementation, this term is described by the voltage-controlled voltage source V_{dep} connected in series with a constant gate oxide-related capacitance C_{oxd} in the LC method. The fourth term of I_{nd} is added by us.[9] It is due to the adoption of the moving uniform nodes indexed from n_3 to n_N to describe the effect of the moving boundary of the depletion layer at $x = W$. The symbol $\overline{p}$ denotes the average carrier density in the undepleted N^- base region. This term may be small for the slow change of dW_{dep2}/dt in IGBT devices due to the large gate-related capacitance, but cannot be ignored in fast-switching PIN diodes.

Near the line $x = W$ in Fig. 1(a), the current flow has a 2D property. A small part of the hole current flows from the bottom vertically through the depletion layer of the emitter–base pn junction J_2 in the left side. We will ignore this small hole current component to derive the 2D correction and assume that the hole current flows from the bottom region II to the top direction and makes a right turn near $x = W$ into region I, where it turns left to the P-well. In Fig. 1(a), the physical property on the line of $x = W$ is not uniform. However, in Fig. 4 this line is approximated as the drain terminal d. When V_{CE} is small, the depletion layer of the emitter–base pn junction J_2 is only distributed in the left side, and when V_{CE} is high enough and the current is low, the depletion layer starts to extend to the full region under the gate. The 2D nature is clearly visible in the emitter side. In an IGBT model, V_{ds} is defined by the bias across the emitter–base pn junction J_2. It is not equal to the usual drain–source voltage difference of the NMOSEFT. As the other part of V_{ds} drops in region I shown in Fig. 1(a), which works as a JFET, the value of V_{ds} is easily extracted from the potential distribution in the depletion layer of the emitter–base pn junction J_2 near $x = W$ at the left boundary from TCAD simulation. Thus, we can extract I_{mos} versus V_{ds} from the DC voltage sweep of the TCAD simulation. The following behavior model for the NMOSFET channel current is used for $V_{gs} = V_{GE} > V_{th}$:

$$I_{mos} = \begin{cases} 0 \text{ for } V_{ds} < V_{ds0}, \\ \frac{K_p\left[(V_{gs} - V_{th})(V_{ds} - V_{ds0}) - 0.5K_f(V_{ds} - V_{ds0})^2\right]}{1 + \theta(V_{gs} - V_{th})} \\ \text{for } V_{ds0} \le V_{ds} \le V_{dsat} = (V_{gs} - V_{th})/K_f, \\ \frac{K_p/K_f(V_{gs} - V_{th})^2}{1 + \theta(V_{gs} - V_{th})}\left[1 + \lambda(V_{ds} - V_{ds0} - V_{dsat})\right] \\ \text{for } V_{ds} \ge V_{dsat} = (V_{gs} - V_{th})/K_f. \end{cases} \tag{17}$$

The IGBT device is really a multi-dimensional device. However, the existing SPICE IGBT models are still 1D ones with a proper inclusion of some 2D effects. We still follow this direction to set up our FVC SPICE IGBT model. Let us make the 1D approximation and assume the depletion layer of the emitter–base pn junction J_2 is uniformly distributed along the y-axis. I_{pd} is the total hole current at $x = W$ through E_{ds}.

$$E_{ds} = \frac{qN_{eff}}{2\varepsilon_{Si}} W_{dep2}\left(2x_{dep0} + W_{dep2}\right), \tag{18a}$$

$$N_{eff} \equiv N_B + \frac{|I_{pd}|}{qAv_{sat}}. \tag{18b}$$

Here we do not add the effect of I_{nd} in the definition of N_{eff}. When V_{ds} is small, only a very small fraction of hole current passes through the depletion layer to contribute to N_{eff} in the TCAD simulation. However, this correction is comparable to N_B and cannot be ignored. When V_{ds} is high, the electron current will pass though the depletion layer, but the NMOSFET works in saturation and the error of N_{eff} does not affect I_{mos} too much. It is noted that E_{ds} is a voltage-controlled voltage source

if $W_{\rm dep2}$ is taken as a generalized voltage signal and $V_{\rm ds}$ is the voltage difference between nodes d and s. Finally, the current continuity equation, for example (14c), is converted into a SPICE circuit by scaling the hole density $\widetilde{p}_i = p_i/N_0$ with $N_0 = 1\times10^{16}$ cm$^{-3}\cdot$V^{-1}, and making the time-to-resistance transformation $R_{\rm B} = \tau_{\rm B}/C_0$ with $C_0 = 1\times10^{-6}$ F:

$$\left[\frac{C_0(I_{p_{23}} - I_{p_{34}})}{qA\Delta x N_0} + \frac{\widetilde{p}_{\rm m}}{R_{\rm B}}\right] = C_0\frac{{\rm d}\widetilde{p}_3}{{\rm d}t} + \frac{\widetilde{p}_3}{R_{\rm B}}. \tag{19}$$

The term in the left of Eq. (22) is just another generalized current generator. Similar conversions can be done for other current continuity equations. For an IGBT device above the threshold, our simulation shows that the high-injection approximation used in Eqs. (14) and (22) is good enough. However, the literature results and our simulation show that for a PIN diode switching between a forward-biased state and a reverse-biased state, the use of a density-dependent lifetime covers both the low- and high-injection regions, and gives a more accurate current.[17]

The width of the undepleted N$^-$ base is given by the following equation in the FVC method:

$$W = W_0 - x_{\rm dep0} - W_{\rm dep2} = (N-1)\,\Delta x. \tag{20}$$

Note that this width is expressed by d in the LC method and by W in the FVC method.

In the 1D Hefner IGBT model,[4,5] the electron or hole density at $x = W$ is zero. In the 2D TCAD IGBT structure shown in Fig. 1(a), the average carrier density over the y-axis at $x = W$ is not zero; this results in a higher collector current at the same terminal bias. Several papers have investigated 2D effects. Lu *et al.* found that the average hole density $p_{l_{\rm m}}$ over the $l_{\rm m}$ edge on the right-hand side of Fig. 1(a) is approximately proportional to the total hole current I_{pW} at $x = W$. They further assumed the same relation held at $x = W$ between the average hole carrier density p_N over the L-dimension and the hole current $I_{\rm pd}$. In Fig. 1(a), L is the dimension of an IGBT cell on the y-axis. We also define P_w as the average hole density over the L-dimension at $x = W$ and $a_{\rm i}$ as $a_{\rm i} = l_{\rm m}/L$. We will test this assumption using the data from the TCAD simulation and adopt it in our SPICE simulation. The two relations are given as follows:

$$p_{W_0} = a_{\rm i}p_{l_{\rm m}} = cI_{pW_0}, \tag{21a}$$

$$p_N = cI_{\rm pd} \approx cI_{pW_0}. \tag{21b}$$

Here c is a parameter. The approximation $I_{\rm pd} \approx I_{pW}$ is also adopted in Eq. (21b). With Eq. (21), equation (9) is changed into[15]

$$W_{\rm dep2} = -K\times\min\left(p_N - cI_{\rm pd}, 0\right). \tag{22}$$

This can also be converted into a SPICE circuit by taking $W_{\rm dep2}$ as a generalized voltage.

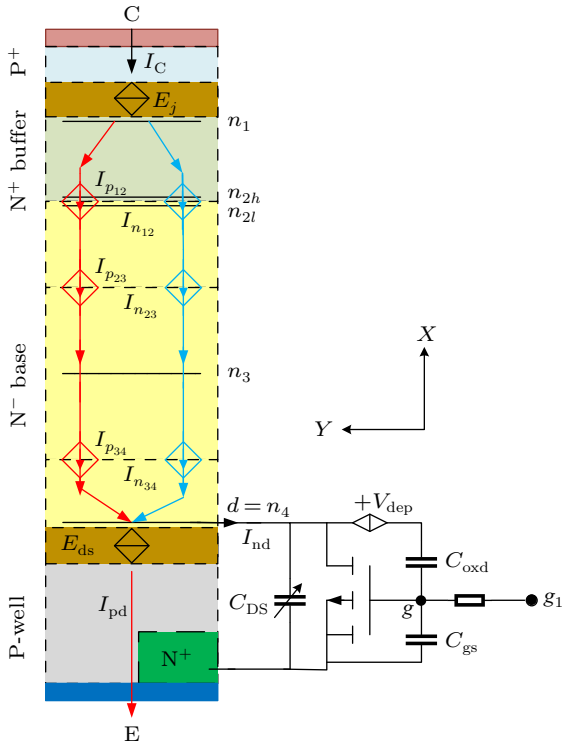


Fig. 4. Schematic picture of the SPICE current circuit implementation of a punch-through IGBT in the FVC method.

A theoretical formula for parameter c is given as[15]

$$c = \frac{l_{\rm m}}{2\ln(10)qD_{\rm p}}G\left(\frac{l_{\rm m}}{W_{\rm p}}\right)\frac{1}{A}. \tag{23}$$

Here $D_{\rm p}$ is the hole diffusion coefficient. The function $G(x)$ is defined in Lu's paper.[15] The area A is given as $A = LL_Z$. Although the parameter $l_{\rm m}$ is bias-dependent it was taken as a constant in Lu's paper.[15]

3. Results and discussion

In this paper, Sentaurus TCAD software and the LTSPICE simulator are used to do simulations. Two node numbers of $N = 11$ and $N = 4$ are compared. All parameters used in this paper are presented in Table 1.

Based on Fig. 1(a), we extract $V_{\rm ds}$ from the TCAD simulated potential, electron and hole distributions across the emitter–base pn junction J$_2$ in a cut line at $y = 9$ μm. In our TCAD IGBT cell structure, near the left boundary at $y = 10.25$ μm, junction J$_2$ is almost uniform and can be approximated as 1D in the x-direction. Then we can form $I_{\rm mos}$–$V_{\rm ds}$ curves. From these curves, we can extract the MOSFET parameters. However, the emitter–base pn junction J$_2$ is not an abrupt junction, so a direct use of the textbook pn junction equations will cause errors of parameters. When a MOSFET works in saturation, it is well known that the total anode current $I_{\rm CE}$ is proportional to the electron current $I_{\rm mos}$. In this case, we have

$$I_{\rm CE} \propto \frac{(V_{\rm GE} - V_{\rm th})^2}{1 + \theta(V_{\rm GE} - V_{\rm th})}. \tag{24}$$

Table 1. Parameters of the TCAD IGBT and circuit.

Symbol	Quantity	Value
W_0	base width	209.9 (μm)
W_H	buffer width	9 (μm)
N_B	donor doping level in base	5.8×10^{13} (cm^{-3})
N_H	donor doping level in buffer	1×10^{16} (cm^{-3})
μ_n, μ_p	base carrier mobilities	1408, 484 ($cm^2{\cdot}V^{-1}{\cdot}s^{-1}$)
μ_{nH}, μ_{pH}	buffer carrier mobilities	1177, 430 ($cm^2{\cdot}V^{-1}{\cdot}s^{-1}$)
τ_B, τ_H	high-injection lifetimes	13, 13 (μs)
τ_n, τ_p	SRH lifetime parameters	10, 3 (μs)
V_T	thermal voltage	0.02585 (V)
L, L_Z	IGBT cell length and width	10.25, 1×10^5 (μm)
W_p, l_m	two size parameters below drain	3, 4.58 (μm)
C_{gs}	gate–source related capacitance	0.25 (nF)
t_{ox}	gate oxide thickness	0.1 (μm)
x_{dep0}	zero-bias depletion width in J_2	4 (μm)
V_{th}	threshold voltage	2.624 (V)
K_p	a parameter for the NMOSFET	2.834 ($A{\cdot}V^{-2}$)
K_f	a parameter for the NMOSFET	1.787
θ	mobility degradation factor	0.17713 (V^{-1})
λ	channel modulation factor	0.005 (V^{-1})
h_p	recombination parameter in J_1	6.35×10^{-13} ($cm^4{\cdot}s^{-1}$)
L_1	inductor in the SPICE circuit	10 (μH)
R_1, R_g	two resistors in the SPICE circuit	50, 1000 (Ω)

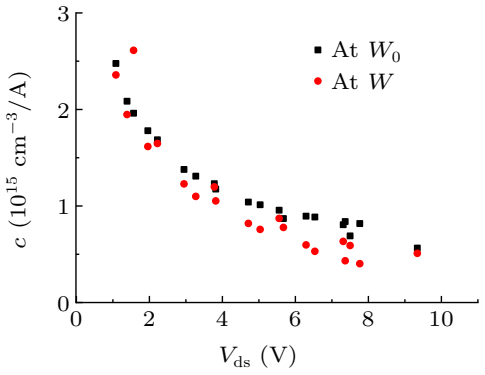


Fig. 5. The dependence of parameter c on V_{ds} extracted from TCAD simulation at $x = W_0$ and $x = W$. The spread of the data is partly due to a weak V_{GE} dependence.

Here the λ-dependence in I_{mos} is ignored. From TCAD simulated I_{CE}–V_{GE} curves at one V_{CE} value, V_{th} and θ can be extracted very accurately.

We then extract the parameter c defined in Eq. (21) from TCAD simulation. Figure 5 shows their values versus V_{ds} extracted at $x = W_0$ and $x = W$. The data are not on a single curve due to a weak V_{GE} dependence. The values of parameter c extracted at $x = W_0$ and $x = W$ almost overlap with each other. The value of c is 2.5×10^{15} $cm^{-3}{\cdot}A^{-1}$ at $V_{ds} = 1$ V, and decreases with increasing V_{ds}. In order to make SPICE simulation possible, two kinds of expressions for c have been tested in this paper: A constant value and a bias-dependent expression. They are denoted as choice c_1 and c_2, respectively. Choice c_1 was used by Lu *et al.*[15], with which $c = 2.89\times10^{15}$ $cm^{-3}{\cdot}A^{-1}$ can be computed from Eq. (23). Then this value is adjusted slightly to give the SPICE simulation a better agreement with our TCAD simulation data. Finally, we take $c = 2.23\times10^{15}$ $cm^{-3}{\cdot}A^{-1}$ in choice c_1. Choice c_2 is obtained by fitting the data of Fig. 5 to a proper analytical formula. The two choices of parameter c are summarized as follows:

$$c = \begin{cases} c_1:\ 2.23\times10^{15}\ \text{cm}^{-3}/\text{A for all } V_{ds}, \\ c_2:\ (V_{GE}+6.0)\exp(-0.2162V_{ds}) \\ \quad\times 1.664\times10^{14}\ \text{cm}^{-3}/\text{A}. \end{cases} \tag{25}$$

Figures 6(a) and 6(b) show the collector current I_C versus V_{CE} without and with the 2D correction, respectively. The results demonstrate the importance of the 2D correction. In Fig. 6(a), I_C values are very different for $N = 11$ and $N = 4$. With choice c_1 in Fig. 6(b), I_C values for $N = 11$ and $N = 4$ are close to each other. Adopting $N = 4$ gives higher I_C values in the linear region due to the error in computing the electric field $-\Delta v/\Delta x$ and the carrier density gradient $\Delta p/\Delta x$. In a transient process, the charge profile changes very fast in space so a larger node number will give a better accuracy. Figure 6(b) shows that for $V_{GE} \le 10$ V, the choice c_2 of parameter c gives better I_C current curves, and for $V_{GE} = 15$ V, the simple linear dependence on V_{GE} in choice c_2 is not enough. The choice c_1 for parameter c can easily achieve convergence in the SPICE simulation under different conditions. However, the data for choice c_2 for parameter c are obtained by converting the results of DC sweeps under a constant V_{CE} condition. A DC sweep under a constant V_{GE} condition does not converge for choice c_2 of parameter c. This indicates that there is still an incompatibility in incorporating the 2D correction in the simple 1D approximation. In the following we will take choice c_1 for parameter c to perform the transient SPICE simulation. Finally, we have done a TCAD mixed-circuit transient simulation. Figure 7 shows the circuit used for the TCAD mixed-circuit simulation and FVC-based SPICE simulation. Figure 8 compares the I_C, V_{GE} and V_{CE} waveforms simulated using the TCAD mixed-circuit simulation and the FVC-based SPICE simulation. The nominal drain–gate overlap area is $A_{gd} = l_m L_Z$. To get a better agreement between the TCAD mixed-circuit simulation and the FVC-based SPICE simulation, a smaller $A_{gd} = 0.6 l_m L_Z$ is used in the SPICE simulation. Checking the electron density under the gate at a switching time of 2.7 μs from TCAD simulation shows that only a part of area $l_m L_Z$ contributes to the capacitance C_{dg}. The agreement between TCAD simulation and the $N = 11$ SPICE simulation is very good. The $N = 4$ SPICE simulation is less accurate than the $N = 11$ one.

The above results demonstrate the effectiveness of our FVC method and the necessity for 2D corrections to the SPICE simulations of IGBT devices. The nonconvergence of the DC sweep of V_{CE} under constant V_{GE} with choice c_2 for parameter c shows that the implementations of 2D corrections at the present stage are not perfect and can be improved further. It

is desirable to give up the simple 1D approximation and develop an IGBT model based on multi-region carrier distributions. Sheng *et al.* and Feiler *et al.* have done pioneering work in this direction.[19,20] The N^- base region is further divided into left and right regions. However, in Sheng's work, the regional carrier density distributions do not consider the mutual charge transfer and are not used to derive the final collector current either.[19] In Feiler's model, charge transfer is allowed between different regions but carrier recombination is completely ignored.[20] We hope to develop a better IGBT model in the future to account for the 2D effects more accurately and then use it to do SPICE simulations.

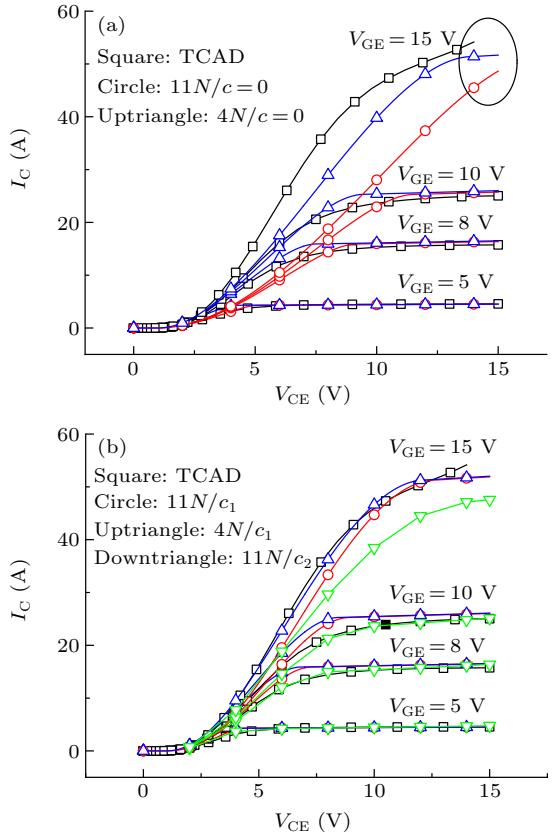


Fig. 6. The collector current I_C versus V_{CE} at different V_{GE}: (a) without 2D correction, (b) with 2D correction using two choices for parameter c.

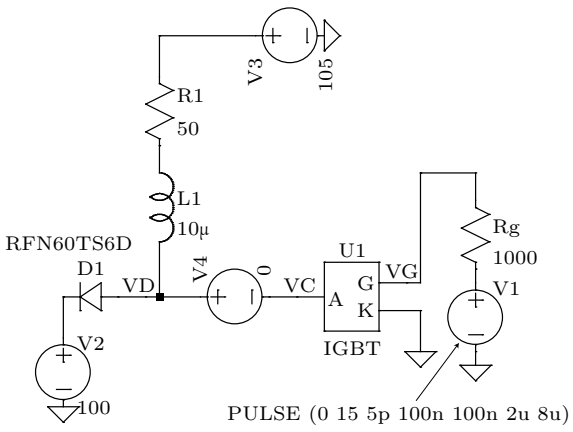


Fig. 7. The circuit used for TCAD mixed-circuit simulation and FVC-based SPICE simulation.

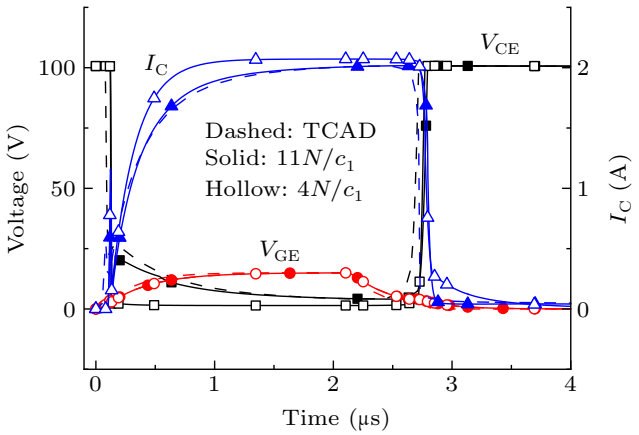


Fig. 8. Comparison of I_C, V_{GE}, and V_{CE} waveforms simulated using TCAD mixed-circuit simulation and FVC-based SPICE simulation.

4. Conclusion

In summary, a finite-volume charge method has been proposed to simulate PIN diodes and IGBT devices using SPICE simulators by extending the lumped-charge method. The new method assumes local quasi-neutrality in the undepleted N^- base region and uses the total collector current, the nodal hole carrier density and voltage only as the basic quantities. Besides the carrier density nodes and the voltage nodes, the SPICE circuit also defines all current generator nodes at clear positions. It uses central finite difference to approximate electron and hole current generators, and sets up the current continuity equation in a control volume for every carrier density node in the undepleted N^- base region. We use this method to simulate a punch-through IGBT device in the LTSPICE simulator. The results are in very good agreement with TCAD simulations. We have compared two kinds of 2D correction formulae for the hole boundary density in the emitter–base side and demonstrated the importance of 2D correction.

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