High performance SiC trench-type MOSFET with an integrated MOS-channel diode

Jie Wei(魏杰)[1], Qinfeng Jiang(姜钦峰)[1], Xiaorong Luo(罗小蓉)[1,†], Junyue Huang(黄俊岳)[1], Kemeng Yang(杨可萌)[1], Zhen Ma(马臻)[1], Jian Fang(方健)[1], and Fei Yang(杨霏)[2]

[1] *School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu* 610054, *China*
[2] *Global Energy Interconnection Research Institute, Beijing* 102209, *China*

(Received 15 February 2022; revised manuscript received 24 June 2022; accepted manuscript online 29 June 2022)

A novel SiC double-trench metal-oxide-semiconductor field effect transistor (MOSFET) with integrated MOS-channel diode is proposed and investigated by Sentaurus TCAD simulation. The new SiC MOSFET has a trench gate and a stepped-trench source, and features an integrated MOS-channel diode on the top sidewall of the source trench (MT MOS). In the reverse conduction state, the MOS-channel diode turns on firstly to prevent the internal parasitic body diode being activated, and thus reduces the turn-on voltage V_F and suppresses the bipolar degradation phenomena. The V_F of 1.70 V (@$I_{ds} = -100$ A/cm^2) for the SiC MT MOS is 38.2% lower than that of SiC double-trench MOSFET (DT MOS). Meanwhile, the reverse recovery charge Q_{rr} of the MT MOS is 58.7% lower than that of the DT MOS at $I_{load} = 700$ A/cm^2, and thus the reverse recovery loss is reduced. Furthermore, owing to the modulation effect induced by the double trenches, the MT MOS preserves the same superior forward conduction and blocking performance as those of DT MOS, with 22.9% and 18.2% improvement on breakdown voltage and $R_{ON,sp}$ compared to the trench gate MOSFET with planar integrated SBD (ST MOS).

Keywords: SiC MOSFET, bipolar degradation, MOS-channel diode, reverse recovery

PACS: 85.30.De, 85.30.Tv, 73.40.Qv, 51.50.+v **DOI:** 10.1088/1674-1056/ac7cd5

1. Introduction

In some applications, such as motor drives and synchronous rectifiers, power devices need an anti-paralleled freewheel diode (FWD) to rectification. One typical method is using an external anti-paralleled Schottky barrier diode (SBD) as the FWD. However, it not only consumes extra area in package, but also introduces parasitic inductance, which limits switching frequency and reduces the power density in power converter/inverter apparatus.[1] Integrating SBDs can address these problems,[2,3] which will degrade blocking characteristic and thermal stability nevertheless. The parasitic PN body diode in SiC MOS can realize reverse conduction function. However, the PN body diode has a high forward voltage drop and bipolar degradation effect, and thus degrades MOSFET's performance.[4,5] The trench gate MOS (T-MOS) is widely used due to its high channel density, while it suffers from critical issue of premature breakdown in the trench gate oxide bottom.[6,7] P-shield region under the trench gate is always used to address this issue.[8–12]

In this work, a novel SiC trench-type MOSFET with an integrated MOS-channel diode (MCD) is proposed (MT MOS) to realize the reverse conduction. The MCD acts as an FWD and suppresses the body diode turning on. Hence the MT MOS achieves superior reverse performances, and the double-trench also improves the forward and blocking characteristics.

2. Structure and mechanism

Figure 1(a) shows the structure of the proposed MT MOS. It has a trench gate and a stepped-trench source, and features an integrated MOS-channel diode (MCD, shown in the red dashed rectangular) on the sidewall of source trench. Note that D_S and t_{oxs} are the depth and sidewall oxide thickness of shallow source trench, L_{off} is the offset between the shallow source trench and P-region. Figure 1(b) shows a double trench MOSFET (DT MOS) with gate trench and source trench surrounded by P-region, just with parasitic PN body diodes as FWD. Figure 1(c) shows a trench gate MOSFET with a planar integrated Schottky diode (ST MOS) as an FWD.

Figures 2(a) and 2(b) show the zoomed schematic diagrams of the MCD and equivalent circuit of the MT MOS. The N^+-source, P-body, N-drift/N^+-drain, source metal and oxide layer together form the MCD. Its anode and cathode electrode are the source and drain electrode of the MOSFET, respectively. It is worth noting that both the MT MOS and the DT MOS own two parasitic PN body diodes (D_1 and D_2). In the reverse conduction mode, the anode and cathode of the MCD are applied to high and low potentials, respectively. Thus, a strong inversion layer is formed along the MOS channel of MCD. This means that the free-wheeling current path for the novel MT MOS is firstly formed through the MCD, instead of turning on the D_1 and D_2. Therefore, the MT MOS could con-

†Corresponding author. E-mail: xrluo@uestc.edu.cn
© 2023 Chinese Physical Society and IOP Publishing Ltd

duct the reverse current in unipolar mode, and thus achieve a low turn-on voltage (V_F), and effectively suppress the bipolar degradation phenomena. On the contrary, the DT MOS conducts the reverse current path in bipolar mode by turning on the D_1 and D_2. The SBD assumes the unipolar mode freewheeling current path for ST MOS. Meanwhile, the MCD is not activated in the forward conduction and blocking states, and thus the MT MOS maintains the forward output and blocking characteristics as good as those of the DT MOS. Table 1 shows the key parameters used in simulations of this work.

Table 1. Parameters for the three MOSFETs.

Parameters	MT MOS	DT MOS	ST MOS
N-drift epitaxy thickness (μm)	12	12	12
N-drift epitaxy doping (cm^{-3})	8×10^{15}	8×10^{15}	8×10^{15}
Depth/width of gate & source trench (μm)	1.5/1	1.5/1	1.5/1
Gate oxide thickness (nm)	50	50	50
Optimized P-body doping (cm^{-3})	1×10^{16}	1×10^{16}	2×10^{17}
Channel mobility[13,14] (cm^2/V·s)	25	25	25

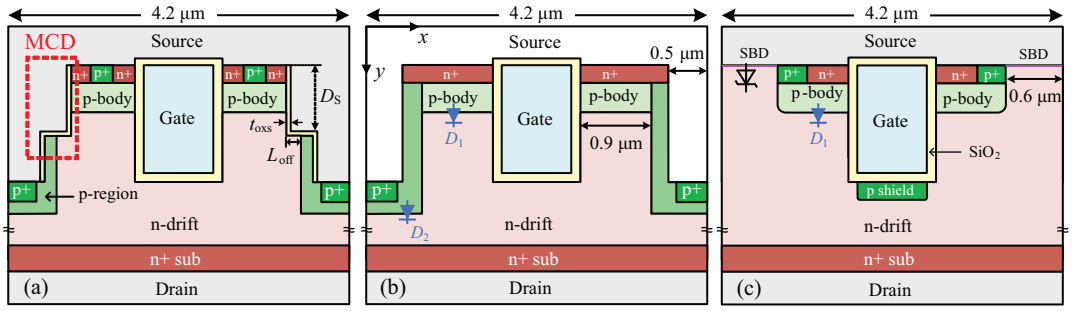


Fig. 1. Schematic views of (a) the MT MOS, (b) the DT MOS, and (c) the ST MOS.

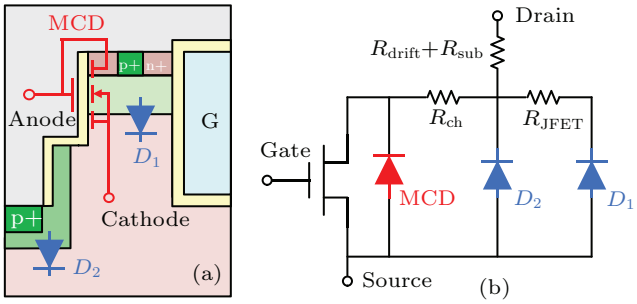


Fig. 2. (a) Schematic view of the MOS-channel diode and two body diodes. (b) Equivalent circuit for the proposed MT MOS.

3. Results and discussion

Figure 3(a) shows the reverse current characteristics in the third quadrant for the three devices. Figure 3(b) illustrates the hole density contours and current flowlines. For the MT MOS in the initial stage, MCD turns on firstly as $|V_{ds}|$ increases and the hole current is zero. It verifies that the MT MOS operates in unipolar conduction mode since the current flows along the inversion layer of MCD as shown in Fig. 3(b). The parasitic body diode turns on at $|V_{ds}| \approx 3.2$ V and the MT MOS transfers to bipolar conduction mode with a sudden increase in the hole/total current. Therefore, the turn-on of the parasitic body diode is suppressed in the red shaded region. For the ST MOS, its integrated SBD also turns on prior to the body diode to conduct in unipolar mode. For the DT MOS, it conducts in bipolar conduction mode and the current flows through the parasitic body diode (shown in Figs. 3(a) and 3(b)). As illustrated in Fig. 3(b), the hole densities in the drift region for MT MOS (e.g., 110 cm^{-3}) and ST MOS (e.g., 370 cm^{-3}) are much lower than that of DT MOS (e.g., 3.1×10^{13} cm^{-3}), which confirms the unipolar mode instead of bipolar mode like that of the DT MOS. Obviously, the $V_F@I_{ds} = -100$ A/cm^2 of the MT MOS and ST MOS reduces to 1.70 V from 2.75 V of the DT MOS. The voltage transferring to the bipolar mode for MT MOS is larger than that for DT MOS, because the MCD suppresses the bipolar conductance modulation effect.

Figures 4(a) and 4(b) compare the forward conduction and blocking characteristics of the three devices. The $R_{ON,sp}$ values for the MT MOS and DT MOS are 1.525 mΩ·cm^2 and 1.536 mΩ·cm^2, respectively. The breakdown voltages (BVs) for the MT MOS and DT MOS are 1487 V and 1493 V, respectively. Both devices exhibit almost the same figure-of-merit (FOM = $BV^2/R_{ON,sp}$) value about 1.45 GW/cm^2. Therefore, the MT MOS almost does not degrade the $R_{ON,sp}$ or BV compared with the DT MOS. By the way, the slightly weakened output current capability of the MT MOS is due to stronger JFET effect caused by shallow source trench. It is favorable for improving the short-circuit ruggedness of the device.[15] For the ST MOS, the $R_{ON,sp}$ is 1.865 mΩ·cm^2 and its BV is just about 1210 V, because its electric field (E-field) modulation effect is weakened without the double trench. To further investigate the breakdown characteristic, the E-field distributions in the blocking state with $V_{ds} = 1200$ V are shown in

Fig. 4(b). Related parameters have been optimized to keep the E-field peak in gate oxide (E_{ox-m}) lower than 4 MV/cm for the MT and DT MOSFETs.[16,17] It shows that the source trench and P-region prevent the gate oxide bottom from premature breakdown, and the stepped-trench source further improves the electric field distribution in the MT MOS. However, the E_{ox-m} in the ST MOS is larger than 4 MV/cm, owing to lack of source trench to modulate the E-field distribution.

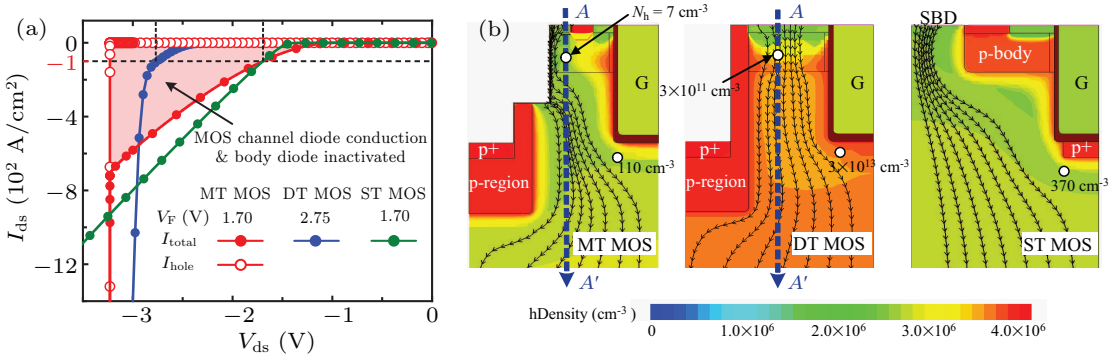


Fig. 3. (a) Reverse conduction I–V characteristics at $V_{gs} = -5$ V. (b) Hole density and total current flowlines distribution for three devices at $I_{ds} = -100$ A/cm^2.

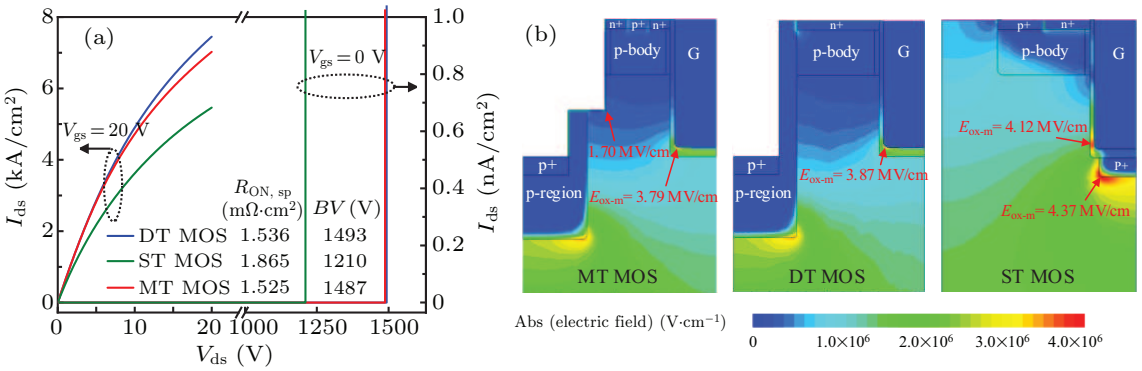


Fig. 4. (a) The I–V characteristics in forward conduction and blocking states. (b) Electric field contours at $V_{gs} = 0$ V and $V_{ds} = 1200$ V in half-cell for the three devices.

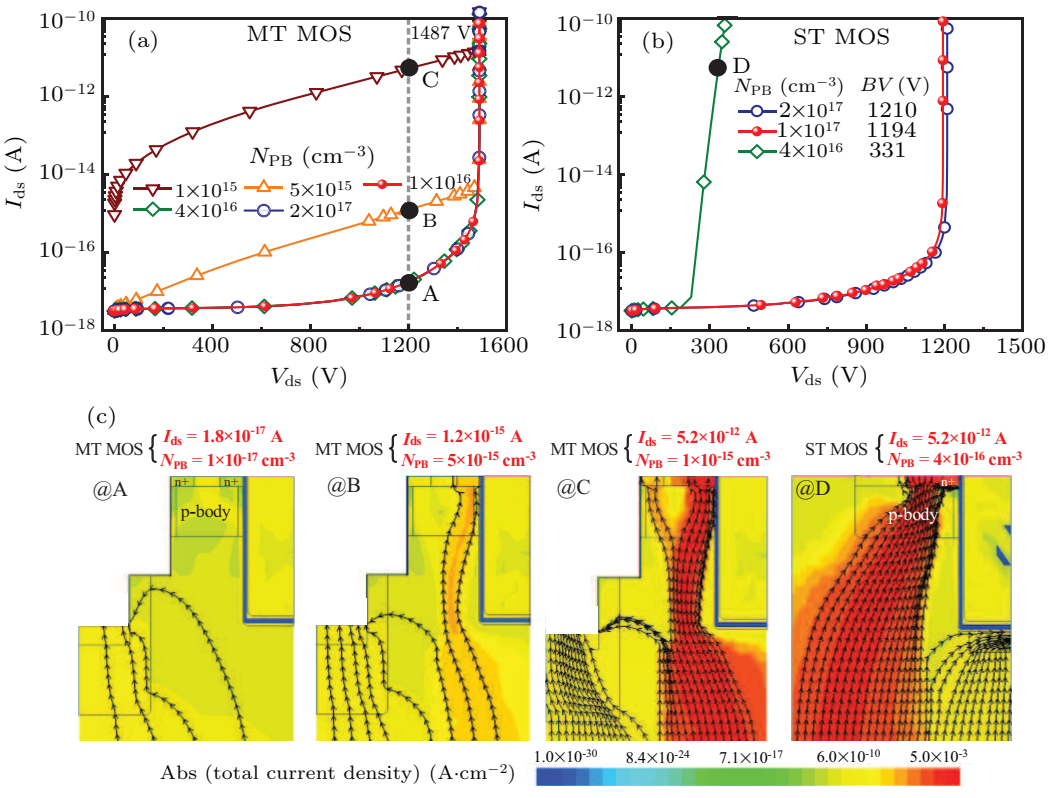


Fig. 5. (a) and (b) Forward blocking characteristics and (c) current flowlines distributions for the MT MOS and ST MOS with different N_{PB}.

Figures 5(a) and 5(b) compare the forward blocking I–V characteristics for the MT MOS and ST MOS with different P-body doping concentrations (N_{PB}). Figure 5(c) illustrates the leakage current flowlines distributions extracted from the A, B, C and D points labeled in Figs. 5(a) and 5(b). For MT MOS, the leakage current keeps a low value (about 10^{-17} A) when $N_{PB} \geq 1\times10^{16}$ cm^{-3}, while significantly increases (about 5×10^{-12} A) at $N_{PB} = 1\times10^{15}$ cm^{-3}. For the ST MOS, the blocking voltage significantly decreases when $N_{PB} = 4\times10^{16}$ cm^{-3}. For both the devices, high leakage current and BV degeneration are caused by the punch-through of the P-body in NPN (N+/P-body/N-drift), as shown in Fig. 5(c). Therefore, both the MT MOS and DT MOS in this work adopt $N_{PB} = 1\times10^{16}$ cm^{-3} to ensure low V_F and high BV, and the ST MOS adopts $N_{PB} = 2\times10^{17}$ cm^{-3}.

The reverse recovery characteristics are investigated by simulations with the inductive clamping double pulses test circuit shown in Fig. 6(a). The purple or pink dashed arrows denote current paths when the upper arm MOSFET (device under test, DUT) is working in freewheeling or shutdown mode. The blue arrow denotes the reverse recovery current of DUT. Figure 6(b) illustrates that the reverse recovery waveforms of the MT MOS and DT MOS are almost the same at $I_{load} = 100$ A/cm^2. However, at a high I_{load} (e.g., $I_{load} = 400$, 700 A/cm^2), the reverse recovery current peak and reverse recovery time of the MT MOS are far less than those of the DT MOS. To investigate the mechanism, Fig. 6(c) shows the hole concentration along AA' cut line (in Fig. 3(b)) in reverse freewheeling mode. At $I_{load} = 100$ A/cm^2, the hole concentration of the DT MOS is much lower than the N-drift region doping (N_{drift}), and thus its reverse recovery characteristic is the same as that of MT MOS. However, at $I_{load} = 400$ A/cm^2 and 700 A/cm^2, the injected hole concentrations in DT MOS are higher than the N_{drift}, while the hole concentrations in MT MOS are still much lower than the N_{drift}. This is because the body diode in DT MOS is completely turned on at the large I_{load} (e.g., $I_{load} \geq 400$ A/cm^2), and then a large number of holes are injected into the drift region to realize the conductance modulation effect. However, the MT MOS relies on MCD to achieve reverse conduction, which could suppress the conductance modulation effect induced by the body diode. Thus, only a few holes are injected into the drift region and then the MT-MOS shows much lower hole density even at the large I_{load}. Therefore, the MT MOS shows a much better reverse recovery characteristic than the DT MOS at a high current density, owing to much fewer excess carriers needed to be extracted. The reverse recovery characteristics of ST MOS are similar to those of the MT MOS, because both devices are in unipolar mode. Compared with the DT MOS, the decreased ratio of reverse recovery charge (Q_{rr}) for the MT MOS increases from 2.55% at $I_{load} = 100$ A/cm^2 to 58.7% at $I_{load} = 700$ A/cm^2 as shown in Fig. 6(d). It indicates that the MT MOS exhibits obvious advantages over the DT MOS at high I_{load}.

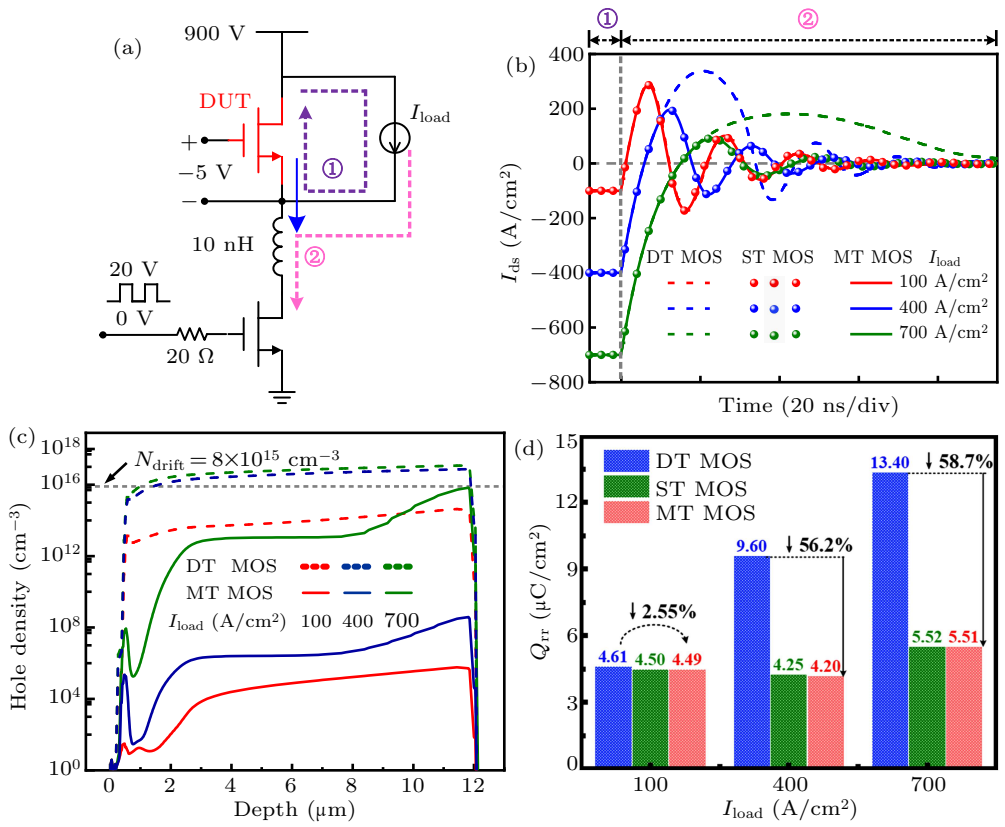


Fig. 6. (a) Inductive clamping double pulse test circuit for the reverse recovery characteristics. (b) Reverse recovery waveforms. (c) Hole concentration in reverse freewheeling mode. (d) Reverse recovery charge (Q_{rr}) under different I_{load}.

Figure 7(a) depicts the impacts of N_{PB} and t_{oxs} on V_F for the MT MOS. Obviously, the V_F decreases with the decreasing t_{oxs} or N_{PB}. That is because the electronic barrier heights are lower for smaller t_{oxs} or N_{PB} values, as the conduction band distribution along the MCD sidewall is shown in Fig. 7(b). Then, it is easier to form the inversion layer to conduct the reverse current and realize a lower V_F. The area below the red dashed line in Fig. 7(a) represents the optimal region, in which V_F value is lower than $V_F = 2.75$ V of DT MOS. For a too high N_{PB}, it is difficult to form the inversion layer and thus the PN body diode turns on to determine the V_F, wherein the V_F is above 2.75 V and is almost independent of t_{oxs}. However, if the N_{PB} is too low, the leakage current of the MT MOS in blocking mode will be too large, which is discussed in Fig. 4.

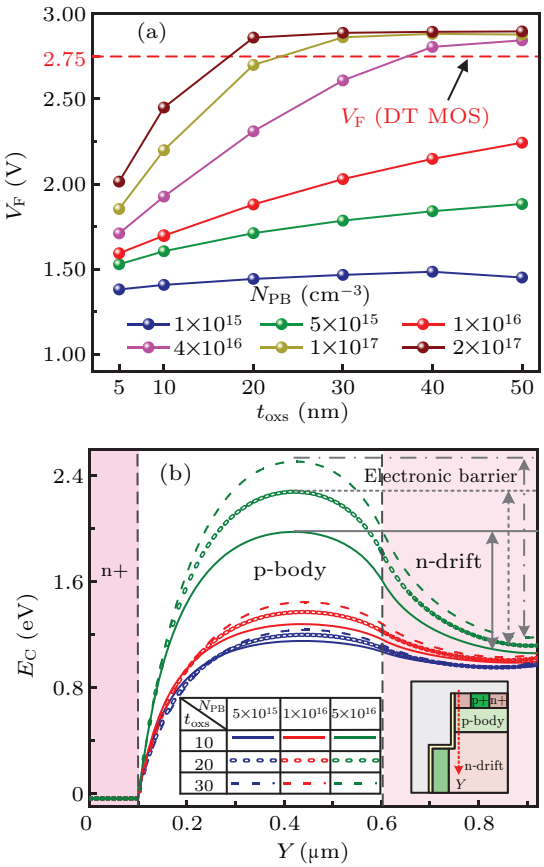


Fig. 7. (a) Influences of t_{oxs} and N_{PB} on V_F for MT MOS at $I_{ds} = -100$ A/cm^2. (b) Conduction band distributions along MCD sidewall with different N_{PB} and t_{oxs} at $V_{ds} = 0$.

Figure 8(a) shows the impacts of the D_S and L_{off} on V_F. The V_F of the MT MOS decreases with the increasing D_S owing to the lengthened electron accumulation layer path along the MCD sidewall. Also, the optimal value (> 0.15 μm) of L_{off} can reduce the spreading resistance and then a small V_F can be obtained. It is noticeable that when D_S is larger than 0.9 μm, the V_F changes just slightly with the varying L_{off}, as the shaded region shown in Fig. 8(a). The influences of the work function (W_m) of source metal on V_F and reverse conduction I–V characteristic are depicted in Fig. 8(b). As the work function increases, the V_F increases while the $|V_{ds}|$ required to transfer to the bipolar conduction mode decreases, because the mutual depletion effect induced by the source metal is enhanced. Considering the influences of these parameters, an optimized V_F of 1.70 V at $N_{PB} = 1 \times 10^{16}$ cm^{-3}, $t_{oxs} = 10$ nm, $D_S = 1$ μm and $L_{off} = 0.2$ μm is achieved. In this work, the work function value of the source contact metal is set to 4.25 eV,[8] and the mentioned work function values and their source metal can refer to Refs. [8,18–22].

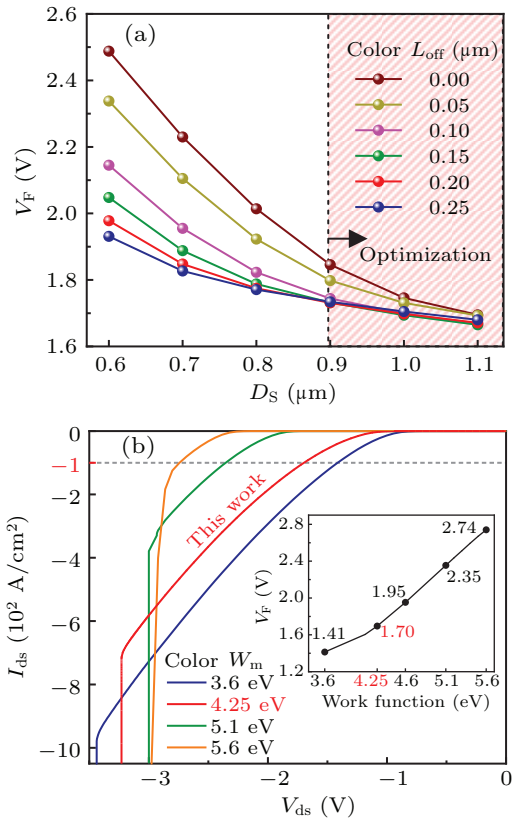


Fig. 8. Influences of the (a) D_S and L_{off}, and (b) work function (W_m) of source metal on V_F for the MT MOS at $I_{ds} = -100$ A/cm^2.

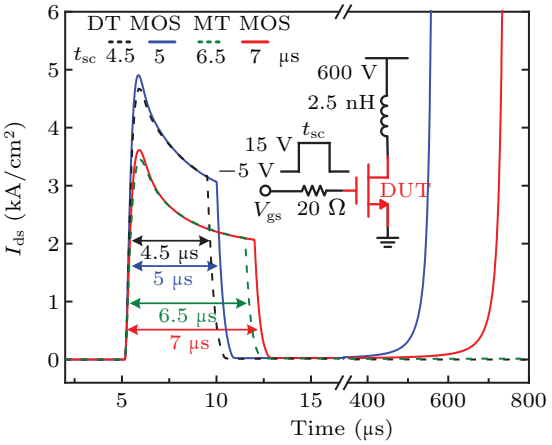


Fig. 9. Short-circuit characteristics for the MT MOS and DT MOS.

Figure 9 shows the short-circuit waveforms. The failures of the MT MOS and DT MOS are detected when the gate turns off and I_{ds} sharply rises, which is caused by the high heat generated in the short circuit process and unable to give away in

time. Owing to its lower saturation current, the short-circuit time of the MT MOS extends to 7 μs from 5 μs of the DT MOS. As shown in Table 2, the MT MOS achieves better comprehensive performances than other two devices.

Table 2. Performance comparison of the three devices.

Parameters	MT MOS	DT MOS	ST MOS
V_F (V) (@I_{load} = 100 A/cm^2)	1.70	2.75	1.70
Q_{rr} (μC/cm^2) (@I_{load} = 700 A/cm^2)	5.51	13.36	5.52
Bipolar degradation	No	Yes	No
Short-circuit time (μs)	7	5	–
BV (V)	1487	1493	1210
$R_{ON,sp}$ (mΩ·cm^2)	1.525	1.536	1.865

4. Conclusion

A novel SiC MOS with an integrated MOS-channel diode is proposed and studied by TCAD simulations. The MCD can realize a low V_F in unipolar reverse conduction mode and then suppress the bipolar degradation. The simulation results show that the MT MOS exhibits a significant improvement in both the forward and reverse characteristics. The V_F of MT MOS is 38.2% lower than that of DT MOS. The reverse recovery charge Q_{rr} of MT MOS is 58.7% lower than that of the DT MOS at I_{load} = 700 A/cm^2. Therefore, the reduced reverse recovery loss is obtained for MT MOS, especially in the case of large load currents. Meanwhile, the MT MOS preserves the same advantages as those of DT MOS in forward conduction and blocking characteristics, and increases the BV by 277 V compared with the ST MOS.

Acknowledgements

The authors appreciate the support by the Science & Technology Program (High voltage and high power SiC material, devices and the application demonstration in power electronic transformers) of the State Grid Corporation of China Co. Ltd.

Project supported by the National Key Research and Development Program of China (Grant No. 2016YFB0400502).

References

[1] Saito K, Miyoshi T, Kawase D, *et al.* 2018 *IEEE Trans. Electron Dev.* **65** 1063
[2] Han Z, Bai Y, Li C, *et al.* 2021 *IEEE Trans. Electron Dev.* **68** 192
[3] Li X, Tong X, Huang Alex Q, *et al.* 2018 *IEEE Trans. Electron Dev.* **65** 347
[4] Skowronski M and Ha S 2006 *J. Appl. Phys.* **99** 11101
[5] Agarwal A, Fatima H, Haney S, *et al.* 2007 *IEEE Electron. Dev. Lett.* **28** 578
[6] Agarwal A K, Casady J B, Rowland L B, *et al.* 1997 *IEEE Electron. Dev. Lett.* **18** 586
[7] Tan J, Cooper J A and Melloch M R 1998 *IEEE Electron. Dev. Lett.* **19** 487
[8] Nakamura T, Nakano Y, Aketa M, *et al.* 2011 *Proceeding of the International Electron Devices Meeting*, December 5–7, 2011, Washington, DC, USA, p. 26.5.1
[9] Zhou X, Pang H, Jia Y, *et al.* 2020 *IEEE Trans. Electron Dev.* **67** 582
[10] Wang Y, Tian K, Hao Y, *et al.* 2016 *IEEE Electron. Dev. Lett.* **37** 633
[11] Chen X M, Shi B B, Li X, *et al.* 2021 *Chin. Phys. B* **30** 048504
[12] Ran S L, Huang Z Y, Hu S D, *et al.* 2022 *Chin. Phys. B* **31** 018504
[13] Liu X Y, Hao J L, You N N, *et al.* 2020 *Chin. Phys. B* **29** 037301
[14] Chung G Y, Tin C C, Williams J R, *et al.* 2001 *IEEE Electron. Dev. Lett.* **22** 176
[15] Peterset D, Siemieniec R, Aichinger T, *et al.* 2017 *Proceeding of the 29th International Symposium on Power Semiconductor Devices and IC's*, May 28–June 1, 2017, Sapporo, Japan, p. 239
[16] Saha A and Cooper J A 2007 *IEEE Trans. Electron Dev.* **54** 2786
[17] Zhou X, Yue R, Zhang J, *et al.* 2017 *IEEE Trans. Electron Dev.* **64** 4568
[18] Lide D R 1969 *CRC Handbook of Chemistry and Physics* 86th edn. (Boca Raton, FL: CRC Press)
[19] S Tsukimoto, K Nitta, T Sakai, *et al.* 2004 *J. Electron. Mater.* **33** 460
[20] S Tsukimoto, T Sakai, T Onishi, *et al.* 2005 *J. Electron. Mater.* **34** 1310
[21] L G Fursin, J H Zhao and M Weiner. 2001 *Electron. Lett.* **37** 1092
[22] N A Papanicolaou, A Edwards, M V Rao, *et al.* 1998 *Appl. Phys. Lett.* **73** 2009