Enhancement of holding voltage by a modified low-voltage trigger silicon-controlled rectifier structure for electrostatic discharge protection

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A novel structure of low-voltage trigger silicon-controlled rectifiers (LVTSCRs) with low trigger voltage and high holding voltage is proposed for electrostatic discharge (ESD) protection. The proposed ESD protection device possesses an ESD implant and a floating structure. This improvement enhances the current discharge capability of the gate-grounded NMOS and weakens the current gain of the silicon-controlled rectifier current path. According to the simulation results, the proposed device retains a low trigger voltage characteristic of LVTSCRs and simultaneously increases the holding voltage to 5.53 V, providing an effective way to meet the ESD protection requirement of the 5 V CMOS process.

Keywords: electrostatic discharge, floating n-well, low-voltage trigger silicon-controlled rectifier

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1. Introduction

With the gradual shrinking of the electrostatic discharge (ESD) design window and chip area, the ESD in low-voltage integrated circuits faces many challenges arising from thin dielectrics, shallow junctions, etc. Accordingly, designs of ESD protection are critical for high-performance circuits.[1–4] The commonly used protective devices in ESD protection design include diode, metal-oxide-semiconductor field-effect transistor (MOSFET), bipolar junction transistor (BJT), and silicon-controlled rectifier (SCR). Among these devices, SCR possesses a relatively higher current driving capability, the highest area efficiency, and robustness.[5] However, a high trigger voltage of common SCR limits its applications in advanced CMOS technology.[6,7] On the other hand, the SCR with a low holding voltage usually faces a latch-up effect.[8,9] Therefore, SCR-based ESD protection devices have been studied over the past few decades.[10–14] To accommodate the ever-shrinking ESD design window, devices with low trigger voltage, high hold voltage, and improved dynamic resistance have become a research hotspot.

Low-voltage trigger silicon-controlled rectifier (LVTSCR) affects the avalanche breakdown by introducing the GGNMOS structure in the SCR, as shown in Fig. 1(a). The improved device structure can significantly reduce the trigger voltage of SCR. However, the low holding voltage caused by the strong snapback of the coupled n–p–n and p–n–p bipolar junction transistors (BJT) has not been optimized in traditional LVTSCRs.[15,16] The traditional approach is to increase the holding voltage by increasing the gate length. However, this improvement increases the area of the thin gate oxide, resulting in a drop in secondary breakdown current. The N^+ active region bridged on the P/N well junction of the LVTSCR is divided into blocks. This improved method will build an auxiliary current discharge path, which can increase the holding voltage.[17] However, this method will reduce the failure current value and affect the robustness of the device.

In this work, a novel structure named as the PN-LVTSCR is proposed by adding a floating n-well region and ESD implant to the LVTSCR structure. The simulation results show that the use of floating n-well and ESD implant in the LVTSCR maintains the low trigger voltage characteristics and simultaneously increases the holding voltage.

2. A novel low voltage trigger silicon-controlled rectifier

2.1. Device structure and description

The cross-sectional and equivalent circuit diagrams of the conventional LVTSCR and the proposed PN-LVTSCR are shown in Fig. 1. The width of the conventional LVTSCR and the proposed PN-LVTSCR is set to be an identical value of 100 μm. The other key dimension parameters are outlined in Table 1.

For the LVTSCR, the equivalent circuit diagrams are composed of a parasitic p–n–p transistor (pnp), lateral n–p–n transistor (npn), n-well resistance (R_{NW}), p-well resistance (R_{PW}), and a GGNMOS path. The structure of the LVTSCR is characterized by the GGNMOS structure embedded in the traditional SCR. The addition of the highly doped N^+ region of GGNMOS will reduce the avalanche breakdown voltage, thereby accelerating the triggering process of the LVTSCR.

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Table 1. Key device parameters of the conventional LVTSCR and the proposed PN-LVTSCR.

Dimensions (μm)	LVTSCR	PN-LVTSCR
L	1	1
D_1	1, 2, 3	1, 2, 3
D_2	none	0.5, 1
D_3	none	0, 1, 2
D_4	none	0, 0.5, 1
D_5	none	0.25
D_6	1	1
D_7	1	1

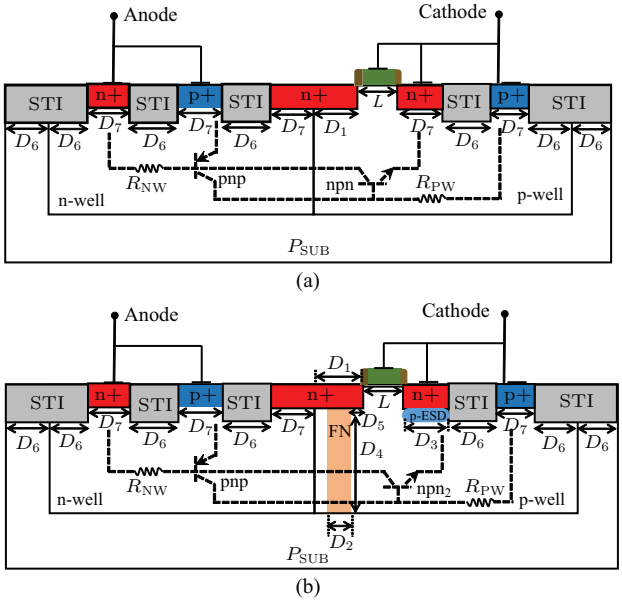


Fig. 1. Cross-sectional and equivalent circuit diagrams of (a) the LVTSCR and (b) the PN-LVTSCR.

As shown in Fig. 1(b), the novel device structure introduces an additional floating n-well (FN) under the drain of GGNMOS. Meanwhile, an ESD implant (P-ESD) is employed in the region close to the source. The main purpose of introducing floating n-well and ESD implant is to reduce the current flowing into the SCR current path and to weaken the beta value of the parasitic n–p–n transistor (npn$_2$).

2.2. Mechanistic analysis of the proposed device

To verify the ESD protection characteristics of the PN-LVTSCR, device simulations were conducted using Sentaurus TCAD.[18] All results simulated are based on the 0.18-μm CMOS process. The multi-current pulses with a rise time of 10 ns and a width of 100 ns to mimic human body model (HBM) events are applied to devices. The quasi-statistic characteristics are obtained by averaging the transient data in an interval of 60–90 ns.[19,20] The physics models such as mobility, avalanche breakdown, Shockley read hall, Auger recombination, effective intrinsic density, and Fermi energy are utilized in these simulations. Lattice temperature correlates with device failure in simulations, and the critical failure temperature of the device is defined in this paper as 1200 K, and the doping concentrations and depths for different regions are listed in Table 2.

Table 2. The doping concentrations and depths for different regions.

Type of mask	Doping concentration (cm^{-2})	Depth (μm)
Highly doped n$^+$	2×10^{20}	0.22
Highly doped p$^+$	2×10^{20}	0.22
p-well	2×10^{17}	2.5
n-well	2×10^{17}	2.5
FN	2×10^{17}	0, 1, 2.5
p-ESD	3×10^{19}	0.42

The distribution of total current density during the whole triggering process of the PN-LVTSCR is shown in Fig. 2. When the anode voltage is too low, there is almost no current flow inside the device. At this time, discharge current does not occur for the PN-LVTSCR, as shown in Fig. 2(a).

The GGNMOS will be the first one to turn on when the ESD surge reaches the GGNMOS avalanche breakdown threshold, as shown in Fig. 2(b). The current path at this time is used as the main discharge path (path 1). However, the floating n-well reduces the doping concentration of the drain region of the GGNMOS.[21,22] This affects the avalanche breakdown process, and increases the value of trigger voltage (V_t).

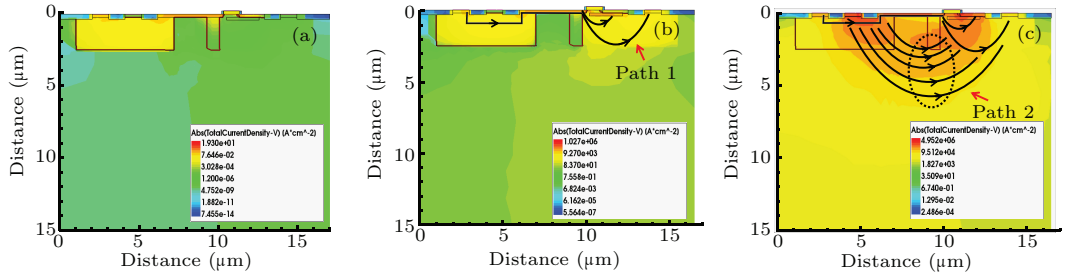


Fig. 2. The total current density distribution of the PN-LVTSCR with (a) no current discharge path, (b) GGNMOS turned on, and (c) parasitic SCR triggered.

Figure 2(c) shows that when the GGNMOS is turned on, the internal cross-coupling n–p–n transistor and the p–n–p bipolar transistor will induce current positive feedback. Namely, the current in the base area is continuously amplified, and a large current is generated. High voltage is no longer needed inside the device to maintain the avalanche breakdown state, causing the conductance modulation effect. As the space charge near the avalanche junction disappears, snapback occurs in the device. At this point, the SCR path is turned on, and the PN-LVTSCR starts to work. Notice that the introduc-

tion of a floating n-well and an ESD implant will increase the base width and base doping concentration of the npn_2. This improved method can significantly enhance the current discharge capability of path 1, decrease the beta value of the npn_2 transistor, and reduce the current flowing through the SCR current path (path 2). Accordingly, the current gain of the SCR is weakened and requires a higher holding voltage to maintain the conduction of the SCR.

Figure 3 shows the *I*–*V* curves of the traditional LVTSCR and the PN-LVTSCR, where the lengths of D_1, D_2, and D_3 are 3 μm, 0.5 μm, and 2 μm, respectively. The holding voltage (V_h) of the proposed PN-LVTSCR is increased from 4.37 V to 5.53 V compared with the traditional one, equivalent to a growth rate of 28.6%.

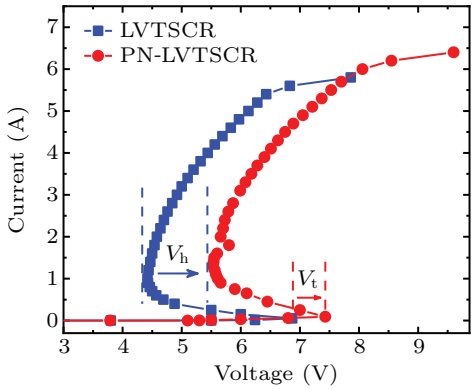


Fig. 3. The *I*–*V* curve of the traditional LVTSCR and the proposed PN-LVTSCR, where the sizes of D_1, D_2, and D_3 are 3 μm, 0.5 μm, and 2 μm, respectively.

On the other hand, a secondary breakdown occurs when the current is eventually increased to the point of thermal failure of the device. However, the introduction of ESD implant affects the operation of the parasitic N^+/P junction, and enhances the current flowing through path 1, thus improving the overall current discharge capability of the device. Such an influence by using ESD implant can also be utilized to understand the improved secondary breakdown (I_{t2}) current.

3. Results and optimizations

The ESD protection performance of the proposed PN-LVTSCR with varying parameters is shown in Fig. 4.

The influence of D_1 on ESD performance is discussed when the D_2 length is 0.5 μm and the D_3 length is 2 μm. Figure 4 shows the *I*–*V* curves of the LVTSCR and PN-LVTSCR with different D_1 lengths. As the length of D_1 increases, the trigger voltage of the PN-LVTSCR slightly increases compared to the LVTSCR. The main reason for this phenomenon is that the floating n-well reduces the doping concentration of the drain region of the GGNMOS, which affects the avalanche breakdown of the n^+/p-well. Although the trigger voltage has increased, the voltage range is still maintained at 7–8 V, which meets the design requirements of ESD protection for the low-voltage integrated circuit.

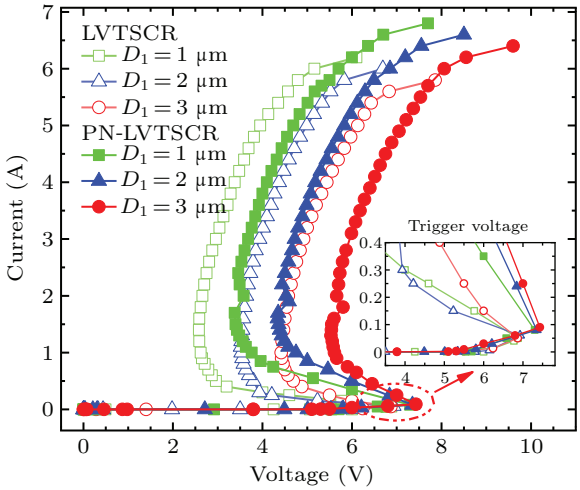


Fig. 4. The *I*–*V* curve of the traditional LVTSCR and the proposed PN-LVTSCR, for different D_1 values.

Similarly, the holding voltage of the same type of device continues to rise with increasing D_1. The rise of D_1 causes the base width of npn_2 to be elongated, which affects the current gain of the transistor. The result requires a larger holding voltage to maintain the internal SCR current path open.

The PN-LVTSCR with the same D_1 length has a higher holding voltage compared with the LVTSCR. It is mainly attributed to the combined effect of the floating n-well and the ESD implant. In such a PN-LVTSCR, the positive feedback effect in the SCR current path is weakened, and the current flowing through the SCR path becomes lower. To maintain the conduction of the SCR path, a larger holding voltage is required. When D_1 is 3 μm, and the depth of the floating n-well is the same as the n/p well, the holding voltage and trigger voltage reach 5.53 V and 7.56 V, respectively. Therefore, the PN-LVTSCR can be used as an ESD protection device for ICs operating at 5 V. It is worth mentioning that this implementation method weakens the positive feedback of the SCR and concurrently slowdowns the device's response speed.

The figure of merit (FOM) is usually used as an evaluation index to evaluate the ESD protection performance of the device.[23] The definition of FOM is as follows:

$$\mathrm{FOM} = (V_h \times I_{t2})/(V_t \times A),$$

where A is the total silicon area of the ESD protection device. The performance parameters of the traditional LVTSCR and the PN-LVTSCR with different structure sizes are listed in Table 3, including trigger voltage, holding voltage, secondary breakdown current, and total silicon area. Finally, the FOM of each device is obtained by calculation. From Table 3, it can be seen that the ESD protection design of this improved LVTSCR has the most efficient FOM.

Table 3. The electrostatic characteristics of the LVTSCR and the PN-LVTSCR.

Structures	D_1 (μm)	V_t (V)	V_h (V)	I_{t2} (A)	A (μm^2)	FOM (mA/μm^2)
LVTSCR	1	6.88	2.58	6.0	2300	0.98
	2	6.93	3.52	5.8	2400	1.23
	3	6.87	4.42	5.5	2500	1.42
PN-LVTSCR	1	7.53	3.38	6.6	2300	1.29
	2	7.50	4.22	6.3	2400	1.48
	3	7.56	5.53	6.1	2500	1.79

Figure 5 shows the effect of different depth of well (D_4) values on the ESD protection performance of the device, where the sizes of D_1, D_2, and D_3 are 3 μm, 1 μm, and 0 μm, respectively.

As the depth of the well increases, the trigger voltage rises from 6.9 V to 7.2 V, and the holding voltage continues to rise from 4.3 V to 5.1 V, with an increase of 19%. The addition of floating n-well weakens the doping concentration of the GGNMOS N^+ region. This will affect the avalanche breakdown process, causing the trigger voltage to rise. On the other hand, the length of the base region of the npn_2 transistor is extended, which weakens the positive feedback effect of the thyristor, thereby increasing the holding voltage.

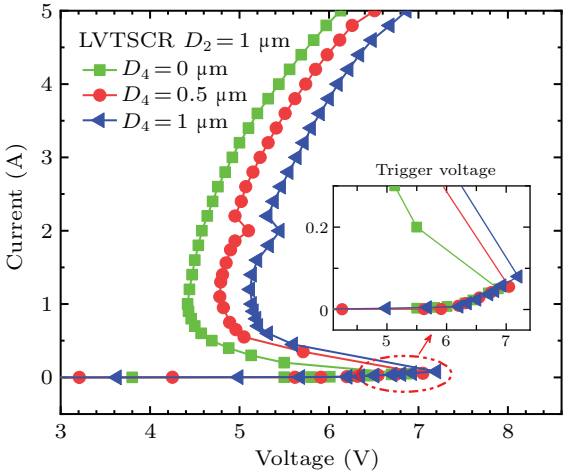


Fig. 5. The I–V curve of the traditional LVTSCR, when taking different D_4 values.

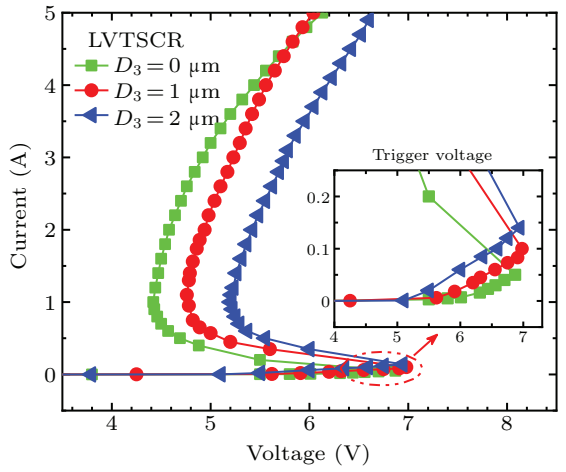


Fig. 6. The I–V curves of the traditional LVTSCR with different lengths of D_3.

The ESD implant plays a critical role in the PN-LVTSCR. The influence of the length of ESD implant on ESD performance is further explored. For the parameter setting, the length of D_1 is optimized at 3 μm, and no floating n-well is added. The I–V curves of the PN-LVTSCR with different ESD implant lengths are shown in Fig. 6.

With an increase in ESD implant length, the trigger voltage shows little change while the holding voltage is significantly enhanced. Due to the introduction of the ESD implant, the base doping concentration of the parasitic transistor of the GGNMOS is increased. This causes the avalanche breakdown of the PN-LVTSCR to occur earlier, but this improvement does not affect the trigger voltage. The main reason for this phenomenon is that the ESD implant reduces the amplification factor of the internal positive parasitic npn transistor, a larger voltage is required to establish the internal positive feedback. At the same time, the doping concentration of the base region of the n–p–n transistor in the SCR current path has also been enhanced, thereby increasing the holding voltage.

4. Conclusion and perspectives

In summary, we have proposed a novel LVTSCR device with a floating n-well and an ESD implant. It shows a better electrical characteristics compared with traditional LVTSCRs in terms of the holding voltage. With a parameter setting of D_1, D_2, and D_3 at 3 μm, 0.5 μm, and 2 μm respectively, the trigger voltage is maintained at 7.56 V, and the holding voltage exceeds 5.53 V, fulfilling the ESD protection requirements of 5 V low-voltage integrated circuits and holding the potential to implement an ESD protection operation within a tiny window of 2.03 V.

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