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Citation: Chin. Phys. B, 2022, 31 (**10**): 108802. DOI: 10.1088/1674-1056/ac6b27
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Development of ZnTe film with high copper doping efficiency for solar cells

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(Received 1 March 2022; revised manuscript received 21 April 2022; accepted manuscript online 28 April 2022)

Since a hole barrier was formed in back contact due to mismatch of work function, the back contact material for CdTe cell has been a significant research direction. The ZnTe:Cu is an ideal back contact material, which reduces the valence band discontinuity and can be used as the electron back reflection layer to inhibit interface recombination. The conductivity of ZnTe:Cu film is improved by applying RF-coupled DC sputtering and post-deposition heat treatment. The doping efficiency is computed as the ratio of free hole density and copper concentration, which can be correlated with performance for CdTe-based solar cell. The higher doping efficiency means that more copper atoms substitute for Zn sites in ZnTe lattices and less mobilized copper atoms remain which can enter into the CdTe absorber layer. Copper atoms are suspected as dominant element for CdTe-based cell degradation. After optimizing the ZnTe:Cu films, a systematic study is carried out to incorporate ZnTe:Cu film into CdTe solar cell. The EQE spectrum is kept relatively stable over the long wavelength range without decreasing. It is proved that the conduction band barrier of device with ZnTe:Cu/Au contact material has an effect on the EQE response, which works as free electron barrier and reduces the recombination rate of free carrier. According to the dark *J*–*V* data or the light *J*–*V* data in the linear region, the current indicates that the intercept gives the diode reverse saturation current. The results of ideality factor indicate that the dominant recombination occurs in the space charge region. In addition, the space charge density and depletion width of solar cell can be estimated by *C*–*V* profiling.

Keywords: solar cell, radio frequency sputtering, doping efficiency, post-deposition heat treatment

PACS: 88.40.jm, 81.15.Cd, 88.40.hj, 81.20.–n **DOI:** 10.1088/1674-1056/ac6b27

1. Introduction

Now, the technology of making cadmium telluride (CdTe) solar cells is one of the key technologies in the field of thin film solar cells.[1–3] CdTe back contact material for cadmium telluride (CdTe) cell has always been a significant research direction.[4] For a solar cell with traditional structure (Fig. 1(a)), a hole barrier is formed in back contact due to mismatch of work function.[5,6] Many researchers have proved that copper-doped zinc telluride (ZnTe:Cu) is an ideal back contact material (Fig. 1(b)).[7,8] The ZnTe:Cu is a hole transport material that is inserted between electrode layer and absorber, which can reduce the valence band discontinuity (0.05 eV–0.30 eV) caused by the contact barrier.[9] Owing to the slight mismatch of lattice between ZnTe:Cu and CdTe, the ZnTe:Cu film can be used as an electron back reflection layer (1.00 eV–1.08 eV) to inhibit interface recombination.[10] After the activation of post-deposition heat treatment (PDHT), high level carrier concentration can be easily achieved.[11]

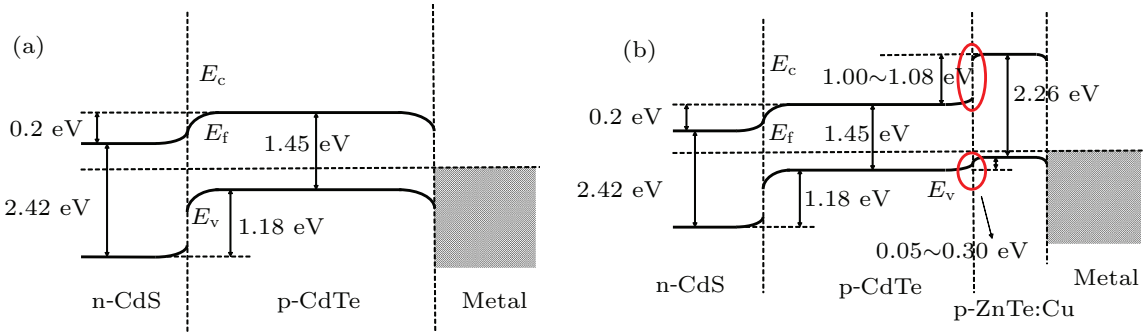


Fig. 1. Schematic diagram of energy band structure for CdTe solar cell (a) metallic contact, and (b) modified cell with ZnTe:Cu layer.

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Although there are few reports on RF coupled DC sputtering of ZnTe:Cu film, there may exist an effect on film properties as demonstrated on ZnO:Al and Cd_2SnO_4.[12,13] In this work, we investigate the influence of target bias and PDHT for ZnTe:Cu. Furthermore, a systematic study is conducted on the devices with different contact materials, which proves that ZnTe:Cu back contact layer may reduce hole barrier. Through effective activation process, the efficiency of solar cell is improved by the modified band alignment.

2. Experiment

2.1. Preparation of ZnTe:Cu and devices

ZnTe:Cu films were prepared on Corning 7059 glass substrates through RF-coupled DC sputtering followed by rapid thermal processing (RTP) at different temperatures.[14] Optimized ZnTe:Cu films were then used to complete CdTe solar cell devices. Both CdS:O and CdTe polycrystalline films were sputtered on the commercial TEC15 substrate by using standard process. Afterwards, the CdS:O/CdTe devices were activated by chloride treatment, which was conducted in mixed atmosphere with 5% oxygen and 95% nitrogen.[15] After the chloride treatment, different back contacts were used (Fig. 2).

For reference, the Au electrode (30-nm thick) or Cu/Au bilayer structure with an optimal Cu thickness (4 nm) was evaporated on an activated absorber surface by electron beam evaporation (Figs. 2(a) and 2(b)). As shown in Fig. 2(c), ZnTe:Cu/Au stacked structure was sputtered on an absorber layer. The ZnTe target with three inches in diameter was used, which has a purity of 99.99% with 5% atomic concentration of copper. The devices with different thickness ZnTe:Cu buffer layers (40 nm–200 nm) were annealed on the RTP furnace at 200 °C–320 °C for 20 s–120 s.

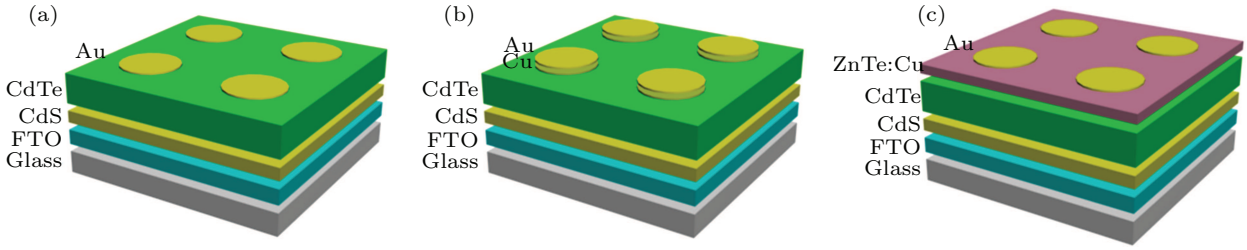


Fig. 2. Schematic diagram of devices with different contact layers: (a) Au, (b) Cu/Au, (c) ZnTe:Cu/Au (nonscaled).

2.2. Characterization methods

The morphology of film surface and device cross section were observed by using scanning electron microscope (SEM, Zeiss Sigma). The film electrical property was measured by Hall effect (Nanometric Hall 5500). The atomic ratio was investigated by energy dispersive spectrometer (EDS, Bruker). For the device, the current density–voltage (J–V) curve was measured on a source meter (Keithley 2400) and solar simulator (Newport Oriel 91159A, USA). External quantum efficiency (EQE) was investigated in PV measurement (QEX7 system, USA). The capacitance–voltage (C–V) was measured in a semiconductor characterization system (SCS, Keithley 4200).

3. Results and discussion

3.1. Improvement of doping efficiency

Deposition rate, optical and electrical properties of ZnTe:Cu film are affected by target bias voltage as demonstrated in previous work.[14] The influence of PDHT and target bias are investigated to understand benefits obtained from RF-coupled DC sputtering and heating process separately. The combined process of PDHT (300 °C) and target bias voltage (−122 V) is dramatically improved, which makes the resistivity decrease from 243.58 Ω·cm to 0.04 Ω·cm (Fig. 3(a)). The carrier mobility is enhanced to 0.214 $cm^2/(V{\cdot}s)$ (Fig. 3(b)). As shown in Fig. 3(c), the carrier concentration is improved from 5.0×10^{17} cm^{-3} to 9.2×10^{20} cm^{-3} at a −122 V bias voltage and RTP at 270 °C for 60 s. Nevertheless, the carrier concentration decreases with excessive annealing temperature increasing. The doping efficiency is computed as the ratio of free hole density to copper concentration, showing an upward trend from 0.03% to 60.9% (Fig. 3(d)).[16] The copper concentration in ZnTe:Cu film is derived from the relative ratio of Zn to Te to Cu from EDS data taken from the same film. The doping efficiency can be correlated with the performance for CdTe-based solar cell. The higher doping efficiency means that more copper atoms substitute for Zn sites in ZnTe lattices and there remain less mobilized copper atoms which can enter into the CdTe absorber layer. Copper is suspected as a dominant element for CdTe-based cell degradation.[17] Possible degradation mechanisms include the decline in window layer transmission (decreased J_{sc}) and change in the space charge region (decreased V_{oc}).[18]

As shown in Table 1, in National Renewable Energy Laboratory, Gessert *et al.* noted that carrier concentration of ZnTe:Cu (0.45 at.%) film is 1.9×10^{18} cm^{-3} at annealing temperature of 375 °C in flowing N_2 for 30 min.[19] And the as-deposited ZnTe:Cu (6 at.%) film reaches a maximum carrier

concentration of 3×10^{20} cm^{-3} at a substrate temperature of 300 °C.[20] In the University of Toledo, Bohn *et al*. noted that the ZnTe:Cu (8.86 at.%) film with a high carrier concentration of 1×10^{21} cm^{-3} is grown at 400 °C.[21] In our laboratory, the doping efficiency of ZnTe:Cu (5 at.%) film (200 nm thick) is improved to 60.9%.

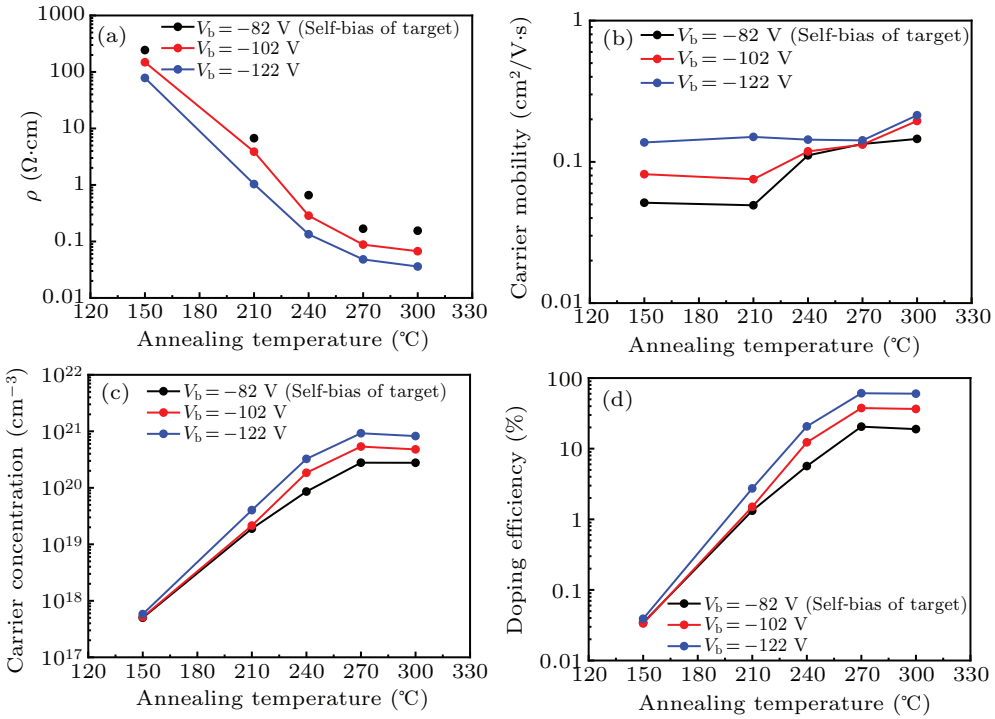


Fig. 3. ZnTe:Cu properties with different target bias of −82 V (black line), −102 V (red line), and −122 V (blue line): (a) resistivity, (b) carrier mobility, (c) carrier concentration, (d) doping efficiency.

Table 1. Summary of electrical performance of ZnTe:Cu films deposited by different groups.

Copper concentration in ZnTe:Cu (at.%)	Film thickness (μm)	Resistivity (Ω·cm)	Carrier concentration (cm^{-3})	Doping efficiency (%)	Groups
0.5	1.0	0.5–1.0	1.9×10^{18}	2.1	NREL, USA
6	1.0	–	3.0×10^{20}	25.3	NREL, USA
8.9	0.7	0.01	1.0×10^{21}	57.0	University of Toledo, USA
5	0.2	0.04	9.2×10^{20}	60.9	IEE, CAS

3.2. Fabrication of CdTe solar cells

To understand the changes of back contact materials, it is significant to review the fabrication of device with fundamental structure. All solar cells are deposited on NSG TEC15 glass which is coated by SnO_2:F (FTO) (Fig. 4(a)). The CdS:O film is sputtered through RF deposition process and used as a window layer on the TEC15 glass for solar cell (Fig. 4(b)). Then polycrystalline CdTe film is deposited on CdS:O film in the same sputtering system with a substrate temperature of 301 °C (Fig. 4(c)). With the achievement of chlorine activation process, the study of the CdTe grain boundary surface by SEM reveals that the $CdCl_2$ treatment results in the enlargement of the grain size (Fig. 4(d)). As for back contact, the interface issue of the mismatch of work function can be solved by inserting a buffer layer of ZnTe:Cu which is prepared by the RF coupled DC sputtering, and device performance is significantly enhanced after being annealed additionally. Figure 4(e) shows that the surface of CdTe film is homogenously covered with uniform ZnTe:Cu film. Figure 4(f) shows the surface morphology of ZnTe:Cu with optimal RTP. After the PDHT, the grain boundaries become blurred where the small grains are "swallowed" by large grains.

The superstrate structure is used for CdTe solar cells as shown in Fig. 5(a). Figures 5(b)–5(d) show the box plots obtained from 36 cell efficiencies for each condition. The active area of each cell is approximately 0.07 cm^2. Figure 5(b) shows the effect of ZnTe:Cu thickness with RTP at temperature 300 °C in 100 s. The cell with 80-nm-thick ZnTe:Cu layer reaches a best performance (10.55%, in average), which is mainly due to the enough copper atoms needed to enhance the p-type doping concentration of the absorber layer. Figure 5(c) shows the efficiency (E_{ff}) values *versus* the annealing temperature for devices with 80-nm-thick ZnTe:Cu layer and anneal-

ing time of 100 s. "No RTP" samples refer to the devices that are unannealed. When the annealing temperature is 280 °C, the maximum solar cell efficiency is obtained (11.63%, in average). Figure 5(d) displays the statistical results of the performance for devices with 80-nm-thick ZnTe:Cu film and the same annealing temperature (280 °C). The $E_{\rm ff}$ value first increases from 8.78% (20 s) to 12.89% (60 s) and then decreased (9.53%, 120 s).

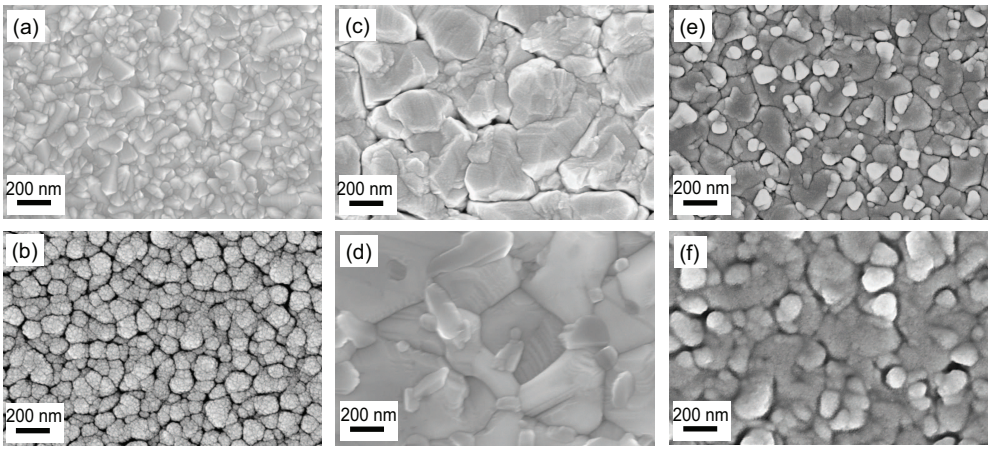


Fig. 4. SEM image of (a) FTO, (b) FTO/CdS:O, (c) FTO/CdS:O/CdTe (as-deposited), (d) FTO/CdS:O/CdTe (with Cl treatment), (e) FTO/CdS:O/CdTe/ZnTe:Cu (as-deposited), and (f) FTO/CdS:O/ CdTe/ZnTe:Cu (with optimized PDHT treatment).

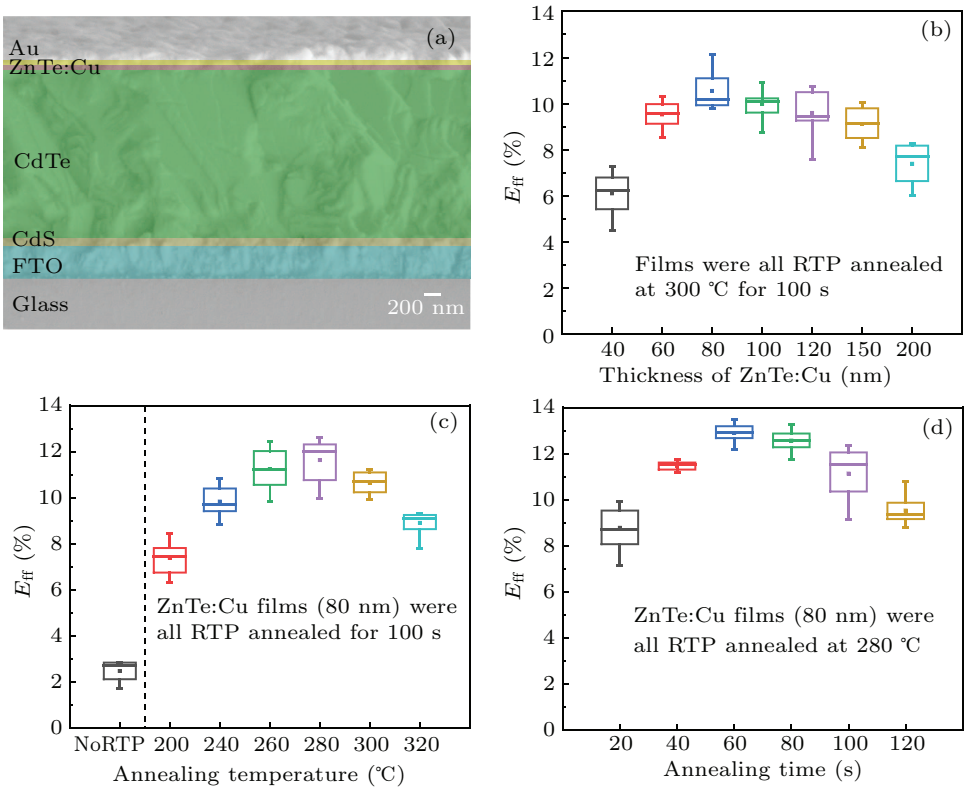


Fig. 5. (a) Cross section of device, (b) effect of ZnTe:Cu thickness on device efficiency, (c) effect of annealing temperature on device efficiency, and (d) effect of annealing time on device efficiency.

Figure 6(a) displays the typical J–V curves for devices with respective contact materials of Au, Cu/Au, ZnTe:Cu/Au with No RTP treatment, ZnTe:Cu/Au with optimal RTP treatment at 280 °C for 60 s, and ZnTe:Cu/Au with excessive RTP treatment at 320 °C for 100 s. We collect the highest efficiency of CdTe-based film solar cell under different preparation conditions. The corresponding photovoltaic measurements of devices are summarized in Table 2.

The typical CdTe soalr cell with Au contact material shows the behavior of "roll-over", which causes FF of 51.51% and $V_{\rm oc}$ of 606 mV. The efficiency value of this device is 7.27%, with $J_{\rm sc}$ = 23.21 mA/cm^2, $R_{\rm s}$ = 9.69 Ω·cm^2, and $R_{\rm sh}$ = 350 Ω·cm^2. The behavior of "roll-over" implies the existence of contact barrier, which results from the mismatch of work function between electrode layer and absorber layer.[22] With the incorporation of a copper film, FF and $V_{\rm oc}$ ex-

hibit a limited improvement of 65.36% and 736 mV, with $R_s = 5.40\ \Omega{\cdot}cm^2$ and $R_{sh} = 1675\ \Omega{\cdot}cm^2$. The J_{sc} value remains essentially unchanged (23.68 mA/cm^2), and thus the overall efficiency increases to 11.48%. As for ZnTe:Cu contact material, as-deposited solar cell with no RTP treatment shows bad current collection (18.41 mA/cm^2). The device efficiency is 2.87%, leading to low V_{oc} (508 mV), the high series resistance R_s (21.26 $\Omega{\cdot}cm^2$), the low shunt resistance R_{sh} (86 $\Omega{\cdot}cm^2$), and fill factor (30.65%). After the optimal RTP treatment, the performance of device is significantly enhanced. The R_s decreases from 21.26 $\Omega{\cdot}cm^2$ to 4.23 $\Omega{\cdot}cm^2$ because of the barrier reduction.[23] The leakage of electricity is prohibited and R_{sh} improves from 86 $\Omega{\cdot}cm^2$ to 1109 $\Omega{\cdot}cm^2$. At the same time, the *J*–*V* curves exhibit no "roll-over" behavior, with $E_{ff} = 13.48\%$, $J_{sc} = 26.76$ mA/cm^2, $V_{oc} = 756$ mV, and $FF = 66.60\%$. Once the devices are over treated with excessive annealing temperature or annealing time, all the photovoltaic parameters obviously decline. For example, the efficiency of cell declines from 13.48% to 9.55% (29.15% in decrement), with $V_{oc} = 730$ mV, $J_{sc} = 25.59$ mA/cm^2, and $FF = 51.10\%$. The degradation is assumed to be mainly because of copper diffusion to CdS:O film, which degrades the PN junction and leads to shunting.

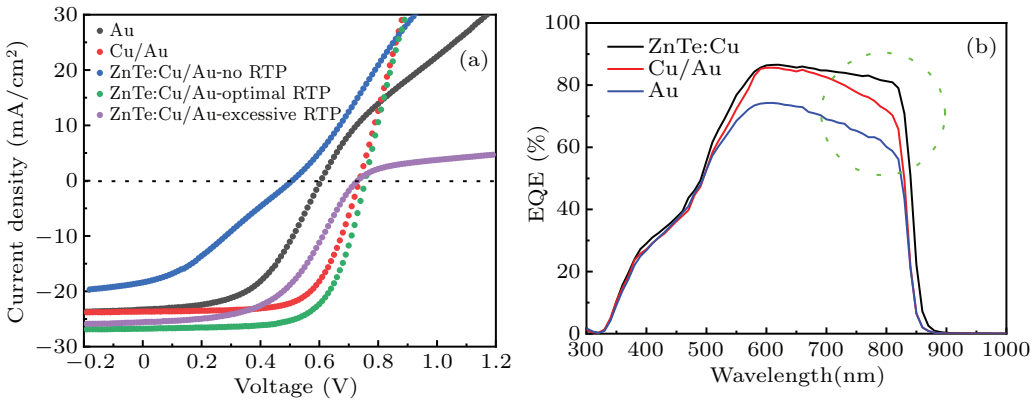


Fig. 6. (a) The *J*–*V* curves and (b) EQE–wavelength curves.

Table 2. Photovoltaic parameters of different devices.

Contact materials	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	E_{ff} (%)	R_s ($\Omega{\cdot}cm^2$)	R_{sh} ($\Omega{\cdot}cm^2$)	A	J (mA/cm^2)
Au	606	23.31	51.51	7.27	9.69	350	2.39	6.4×10^{-7}
Cu/Au	736	23.68	65.86	11.48	5.40	1675	1.70	5.1×10^{-7}
ZnTe:Cu/Au without RTP	508	18.41	30.65	2.87	21.26	86	3.15	5.5×10^{-6}
ZnTe:Cu/Au with optimal RTP	756	26.76	66.60	13.48	4.23	1109	1.64	1.4×10^{-7}
ZnTe:Cu/Au with excessive RTP	730	25.59	51.10	9.55	20.38	450	2.18	5.8×10^{-7}
Solar cell with the novel structure	834	27.98	68.30	15.94	3.44	1244	1.53	9.7×10^{-8}

Annotation: A is the diode ideality factor, and J is the diode reverse saturation current.

As shown in Fig. 6(b), the values of EQE decrease at wavelengths above 600 nm for the device without Cu (with Au electrode only). Similarly, EQE spectrum shape of device with Cu/Au contact material shows a downward trend in a wavelength range of 600 nm–800 nm. Specific to the ZnTe:Cu/Au back contact device with optimized RTP treatment, the EQE spectral keeps relatively stable over the same wavelength range of 600 nm–800 nm without decreasing. In general, because of free carrier recombination near the back contact, the EQE response decreases at long wavelengths.[24] In contrast, the conduction band barrier of device with ZnTe:Cu/Au contact material has an effect on the EQE response, which works as free electron barrier and reduces the recombination rate of free carrier.

To obtain higher conversion efficiency, we prepare CdTe-based solar cells with a novel structure of Cd_2SnO_4 (CTO)/MgZnO (MZO)/CdTe/ZnTe:Cu/Ni. The CTO film (200 nm) is used as the conductive layer instead of FTO film to improve the electrical properties and transmission of TCO layer.[13] The MZO film (80-nm thick) is used as the window layer instead of CdS film to enhance the response of solar cell at short wavelengths.[25] The CdTe absorber prepared by closed space sublimation (CSS) at high temperature replaces the method of magnetron sputtering at low temperatures. In addition, the use of Ni as the back electrode instead of Au can reduce the production cost of solar cells.

Figure 7(a) displays the *J*–*V* curve for the best device with contact materials of ZnTe:Cu/Ni. The *J*–*V* curves exhibit no "roll-over" behavior, with $E_{ff} = 15.94\%$, $V_{oc} = 834$ mV, $J_{sc} = 27.98$ mA/cm^2, $FF = 68.30\%$, $R_s = 3.44\ \Omega{\cdot}cm^2$, and $R_{sh} = 1244\ \Omega{\cdot}cm^2$. Figures 7(b)–7(d) show the box plots obtained from 36 cell efficiencies under the different conditions

of ZnTe:Cu film. Figure 7(b) shows the effect of ZnTe:Cu thickness with RTP at 260 °C for 40 s. The cell with 90-nm-thick ZnTe:Cu layer reaches the best performance (13.09%, average). Figure 7(c) shows the comparison of annealing temperature among devices with 90-nm ZnTe:Cu layer and annealing time of 40 s. When the annealing temperature is 290 °C, the maximum solar cell efficiency is obtained to be an average of 14.00%. Figure 7(d) displays the results of performance for devices with 90-nm-thick ZnTe:Cu film and the same annealing temperature (290 °C). Therefore, ZnTe:Cu back contact layer with a thickness of 90 nm annealed at 290 °C for 40 s can achieve the best conversion efficiency for the devices with novel structure.

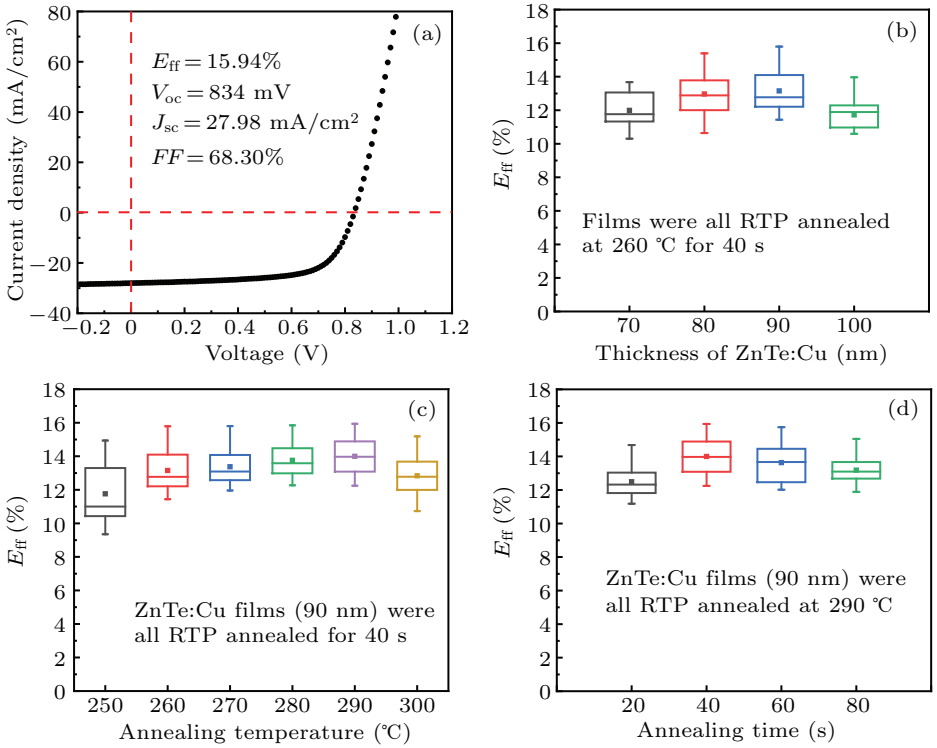


Fig. 7. (a) The *J*–*V* curve, (b) effect of ZnTe:Cu thickness on device efficiency, (c) effect of annealing temperature on device efficiency, and (d) effect of annealing time on device efficiency.

3.3. Analysis of *J*–*V* and *C*–*V* for solar cell

With regard to the characteristic of *J*–*V* behavior, the most important thing is the prevalence of parasitic losses, which can be commonly described by the following diode equations:[24,26]

$$J = J_0 \exp\left[\frac{q}{AkT}(V - R_s J)\right] + GV - J_L, \tag{1}$$

$$g(V) = \frac{dJ}{dV} = J_0 \left[\frac{q\left(V - R_s \frac{dJ}{dV}\right)}{AkT}\right] \exp\left[\frac{q(V - R_s J)}{AkT}\right] + G, \tag{2}$$

$$r(J) = \frac{dV}{dJ} = \frac{AkT}{q}(J + J_L - GV)^{-1} + R_s, \tag{3}$$

$$\ln(J + J_L - GV) = \ln J_0 + \frac{q(V - R_s J)}{AkT}, \tag{4}$$

where J and J_L are the reverse saturation current and photo-generated current, respectively.

The CurVA 2.0 software is used for the numerical analysis of *J*–*V* plot. Figure 8(a) shows the *J*–*V* plots for device with efficiency of 15.94%. This includes sufficient data in the first quadrant and third quadrant where non-ideal effects are not described by Eq. (1), such as current blocking behavior, which are commonly observed in solar cells. Figure 8(b) shows the derivative $g(V)$ with respect to V in a reverse bias voltage region where derivative of diode term in Eq. (2) becomes negligible. In this case, the $g(V)$ curves reveal that $G(\text{dark}) = 0$ mS/cm^2 and $G(\text{light}) = 0.9$ mS/cm^2. In addition, the slope of realistic *J*–*V* curve is very small in the range of reverse bias, so there will be some noise in calculating the derivative under illumination condition. Figure 8(c) shows the dV/dJ *versus* $(J + J_{sc}GV)^{-1}$ plot, which will yield a line if J_L is independent of voltage. From the dark data or the linear region of light data, an intercept is obtained for the series resistance ($R_s = 3.44\ \Omega\cdot\text{cm}^2$) and a slope is calculated for diode ideality factor ($A = 1.53$). Figure 8(d) shows semilogarithmic plot of $(J + J_{sc}GV)$ *versus* $(V - R_s J)$. According to dark data or the linear region of light data, the current indicates that the intercept gives the diode reverse saturation current ($J = 9.7 \times 10^{-8}$ mA/cm^2). The slope is equal to q/AkT, so the

diode ideality factor (A) can be calculated to be 1.53 ($A = 1.53$) which is consistent with the value indicated in Fig. 8(c). In addition, the values of A and J for all devices with different preparation conditions are summarized in Table 2 for comparison. When Cu/Au layers, ZnTe:Cu/Au layers with optimal RTP and ZnTe:Cu/Ni with optimal RTP are used for the back contact of solar cells, the corresponding diode quality factors are 1.70, 1.64, and 1.53, respectively. The results of ideality factor between 1 and 2 indicate that the device operated with dominant trap states is the recombination in space charge region. When Au monolayer, ZnTe:Cu/Au layers without RTP and ZnTe:Cu/Au with excessive RTP are used for the back contact of solar cell, the corresponding diode quality factors are 2.39, 3.15, and 2.18, respectively. When the value of diode ideality factor exceeds 2, the interface and tunneling recombination additionally contribute to the total recombination.[26] This suggests that the better quality absorber layer is necessary for high performance.

To obtain free carrier densities and depletion widths from the PN junction of device, C–V profiling is carried out at room temperature (Fig. 9(a)). The carrier concentration is calculated from the following equations:[27]

$$C(V) = \frac{\Delta Q}{\Delta V} = \frac{\varepsilon}{W} = \sqrt{\frac{q\varepsilon N(W)}{2(V_{\rm D} - V)}}, \tag{5}$$

$$\frac{1}{C^2}(V) = \frac{2(V_{\rm D} - V)}{q\varepsilon N(W)}, \tag{6}$$

$$W = \frac{\varepsilon}{C} = \sqrt{\frac{2\varepsilon(V_{\rm D} - V)}{qN(W)}}, \tag{7}$$

where $C(V)$ is the capacitance per area, ΔQ the incremental depletion charge with an applied voltage ΔV, ε the permittivity of the CdTe, W the depletion width, q the electron charge, $N(W)$ the space charge density, and $V_{\rm D}$ the diffusion voltage.

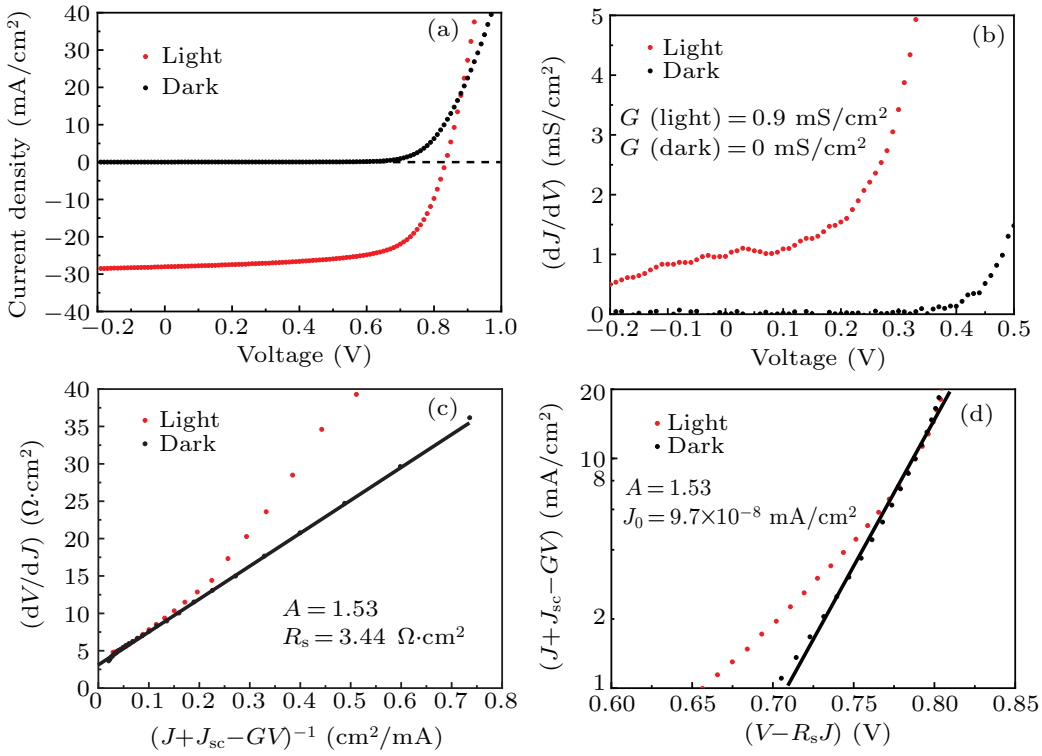


Fig. 8. (a) The J–V plots, (b) $\mathrm{d}J/\mathrm{d}V$ *versus* voltage, (c) $\mathrm{d}V/\mathrm{d}J$ *versus* $(J + J_{\rm sc} - GV)^{-1}$, and (d) $(J + J_{\rm sc} - GV)$ *versus* $(V - R_{\rm s}J)$, for light (red line) and dark (black line) case.

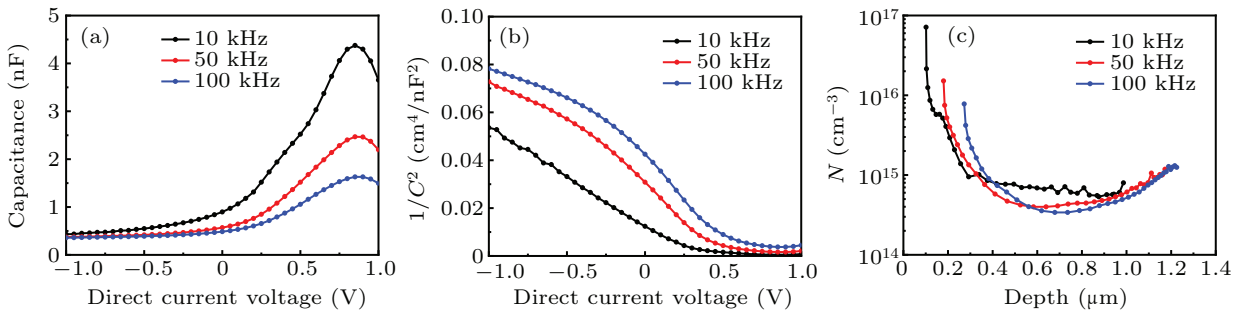


Fig. 9. (a) The C–V plots, (b) $1/C^2$–V plots, and (c) space charge distribution, for different frequencies: 10 kHz (black line), 50 kHz (red line), and 100 kHz (blue line).

Figure 9(b) shows the plot of C^{-2} against V. Under the 10-kHz measurement condition, the data for CdTe device have a line from which the slope and intercept are used to calculate the space charge density (6×10^{14} cm^{-3}) and diffusion voltage ($V_{\rm D}=0.4$ V). Under the 50-kHz and 100-kHz measurement conditions, the device has a varying slope, implying a spatially varying N. The relatively low free carrier value identifies one of the key issues in CdTe solar cell technology, namely, the inability to dope CdTe absorbers to a sufficiently high carrier density. Figure 9(c) indicates the depletion width of device is estimated to be about 900 nm. In addition, the depth profile is U-shaped, presenting a trapped electron density and defect vacancy density, which serve as the leakage paths to reduce the shunt resistance.[9]

4. Conclusions and perspectives

In this work, ZnTe:Cu film (200-nm thick) is sputtered by RF-coupled DC bias voltage system and PDHT, to have the carrier concentration of 9.2×10^{20} cm^{-3} and the doping efficiency of 60.9%. After optimizing ZnTe:Cu films, a systematic study is carried out to incorporate ZnTe:Cu film into CdTe solar cell. Optimized band alignment is supposed to enhance the device performance. However, the device with as-deposited ZnTe:Cu contact material shows low current collection and efficiency. The best efficiency of novel device with optimal PDHT for ZnTe:Cu contact material is 15.94%, with corresponding $V_{\rm oc}=834$ mV, $J_{\rm sc}=27.98$ mA/cm^2, and $FF=68.30\%$. In general, the improvement of device performance can be attributed to barrier reduction and the suppressed leakage of electricity. The further analysis of J–V behavior shows that the results of diode ideality factor ($A=1.53$) between 1 and 2 indicate that the device operates by dominant recombination of trap states in space charge region. The C–V profiling shows that the space charge density remains at 10^{14} level in a frequency range of 10 kHz–100 kHz. Furthermore, the depletion width can be estimated at 900 nm. With all the analysis considered, it is recommended that CdTe-based solar cells be constructed with a ZnTe:Cu back contact layer with optimizing RTP treatment, thereby improving the device performance.

Acknowledgements

The authors are grateful to the Photovoltaic Laboratory at Colorado State University for the CurVA 2.0 software.

Project supported by the Research Foundation of Institute of Electrical Engineering, Chinese Academy of Sciences, (Grant No. Y710411CSB), the Lujiaxi International Team Project of Chinese Academy of Sciences (Grant No. GJTD-2018-05), the Chinese Academy of Sciences President's International Fellowship Initiative (Grant No. 2020VEC0008), and the Fund from the Institute of Electrical Engineering and Advanced Electromagnetic Drive Technology, Qilu Zhongke.

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