

Degradation mechanisms for a-InGaZnO thin-film transistors functioning under simultaneous DC gate and drain biases

Tianyuan Song(宋天源), Dongli Zhang(张冬利), Mingxiang Wang(王明湘), and Qi Shan(单奇)
Citation: Chin. Phys. B, 2022, 31 (**8**): 088101. DOI: 10.1088/1674-1056/ac673e
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Degradation and its fast recovery in a-IGZO thin-film transistors under negative gate bias stress

Jianing Guo(郭佳宁), Dongli Zhang(张冬利), Mingxiang Wang(王明湘), and Huaisheng Wang(王槐生)
Chin. Phys. B, 2021, 30 (**11**): 118102. DOI: 10.1088/1674-1056/ac05aa

Synaptic plasticity and classical conditioning mimicked in single indium-tungsten-oxide based neuromorphic transistor

Rui Liu(刘锐), Yongli He(何勇礼), Shanshan Jiang(姜珊珊), Li Zhu(朱力), Chunsheng Chen(陈春生), Ying Zhu(祝影), and Qing Wan(万青)
Chin. Phys. B, 2021, 30 (**5**): 058102. DOI: 10.1088/1674-1056/abc163

A systematic study of light dependency of persistent photoconductivity in a-InGaZnO thin-film transistors

Yalan Wang(王雅兰), Mingxiang Wang(王明湘), Dongli Zhang(张冬利), and Huaisheng Wang(王槐生)
Chin. Phys. B, 2020, 29 (**11**): 118101. DOI: 10.1088/1674-1056/abb222

Positive gate bias stress-induced hump-effect in elevated-metal metal-oxide thin film transistors

Dong-Yu Qi(齐栋宇), Dong-Li Zhang(张冬利), Ming-Xiang Wang(王明湘)
Chin. Phys. B, 2017, 26 (**12**): 128101. DOI: 10.1088/1674-1056/26/12/128101

Tunable structural color of anodic tantalum oxide films

Sheng Cui-Cui, Cai Yun-Yu, Dai En-Mei, Liang Chang-Hao
Chin. Phys. B, 2012, 21 (**8**): 088101. DOI: 10.1088/1674-1056/21/8/088101

Degradation mechanisms for a-InGaZnO thin-film transistors functioning under simultaneous DC gate and drain biases

Tianyuan Song(宋天源)[1], Dongli Zhang(张冬利)[1,†], Mingxiang Wang(王明湘)[1], and Qi Shan(单奇)[2]

[1] *School of Electronic and Information Engineering, Soochow University, Suzhou* 215006, *China*
[2] *Visionox Technology Co., Ltd, Suzhou* 215006, *China*

(Received 5 January 2022; revised manuscript received 11 April 2022; accepted manuscript online 14 April 2022)

Degradation of a-InGaZnO thin-film transistors working under simultaneous DC gate and drain bias stress is investigated, and the corresponding degradation mechanism is proposed and verified. The maximum degradation occurs under the bias stress condition that makes the electric field and electron concentration relatively high at the same time. Trapping of hot electrons in the etching-stop layer under the extended drain electrode is proven to be the underlying mechanism. The observed degradation phenomena, including distortion in the transfer curve on a logarithmic scale and two-slope dependence on gate bias on a linear scale, current crowding in the output curve, and smaller degradation in transfer curves measured under large drain bias, can all be well explained with the proposed degradation mechanism.

Keywords: a-IGZO, thin-film transistors, hot-carrier effects

PACS: 81.05.Gc, 81.05.Ea, 85.30.Tv **DOI:** 10.1088/1674-1056/ac673e

1. Introduction

Amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) are a promising technology for large-size active-matrix displays owing to their low processing temperature, low leakage current, high uniformity, and relatively high mobility.[1] However, as a switch in the actual work scenario, TFTs are turned on by a gate bias, and then the storage capacitors connected in series will be charged up when a drain bias is applied. The frequent charging processes make the TFTs subjected to a continuous large voltage stress, and the resulting degradation of electrical characteristics of the switch TFTs will seriously affect the quality of the display. Therefore, research on reliability issues of a-IGZO TFTs under simultaneous bias stress appears extremely important.

Previous studies on the reliability of a-IGZO TFTs under bias stress include positive gate bias stress (PBS) and negative gate bias stress (NBS). The positive shift of the characteristic transfer curves of a-IGZO TFTs under PBS has been attributed to carrier trapping in the bulk active layer or at the active layer/gate insulator interface.[2,3] NBS in dark conditions has a negligible effect, but when combined with light illumination (NBIS), large negative threshold voltage shifts are induced, and NBIS has been attributed to defect creation and/or hole trapping at the active-layer/gate-insulator interface.[4–6] In most situations, however, a drain bias is also applied simultaneously with the gate bias. If the gate and drain biases are large, a high current may flow through the TFT and result into joule heating of the TFT's active layer.[7–10]

In this study, the reliability of a-IGZO TFTs under simultaneous gate and drain bias stress is systematically investigated. The degradation mechanism is proposed to be hot electrons trapping in the etching-stop layer (ESL), while the self-heating effect is negligible. The maximum degradation occurs under the bias stress condition in which both the electric field and electron concentration are relatively high at the same time. A larger drain voltage can significantly reduce the potential barrier formed by electrons trapped in the ESL and make the a-IGZO TFT function properly.

2. Experiments

The cross-sectional view of the a-IGZO TFTs used in this study is shown in Fig. 1. A 150-nm-thick molybdenum (Mo) was first deposited and patterned to form the gate. Then, 100-nm-thick SiO_2 was deposited at 300 °C via plasma-enhanced chemical vapor deposition (PECVD) as the gate dielectric. A 50-nm a-IGZO was deposited at 150 °C by sputtering with Ar mixed with 6% O_2 and annealed in dry air at 350 °C for 1 hour. After the a-IGZO was patterned into active islands, 50-nm PECVD SiO_2 was deposited at 150 °C and patterned as the ESL. A 150-nm-thick Mo was deposited and etched to form source/drain electrodes. After the electrodes were defined, a passivation layer of 300-nm SiO_2 was deposited. The source/drain electrodes extending over the ESL formed the extended source electrode (ESE) and the extended drain electrode (EDE) regions, as labeled in Fig. 1, where the length of ESE (L_{ESE}) and the length of EDE (L_{EDE}) are the same.

For the default bias stress condition, a DC bias of 25 V is applied to the gate, and a simultaneous bias stress of 30 V is applied to the drain with the source grounded. The channel width-to-length ratio of a-IGZO TFTs is 10 μm/20 μm. De-

†Corresponding author. E-mail: dongli_zhang@suda.edu.cn
© 2022 Chinese Physical Society and IOP Publishing Ltd

vice degradation is characterized by the change of the turn-on voltage (V_{on}) and threshold voltages (V_{th}) from their respective initial values, where V_{on} is defined as the gate voltage corresponding to $I_D = 10^{-10}$ A, V_{th1} and V_{th2} are extracted by the linear extrapolation method from the first and second linear regions of the transfer curve on a linear scale, which is measured with V_{ds} of 0.1 V.

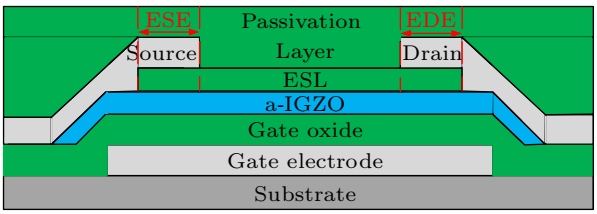


Fig. 1. Schematic cross-sectional diagram of the a-IGZO TFT.

3. Results and discussion

Figure 2 shows the evolution of the transfer curve of the a-IGZO TFT under the stress condition with $V_{gs} = 25$ V and $V_{ds} = 30$ V, where current distortion appears when the drain current transients from the subthreshold region to the on-state region and the subthreshold current exhibits a parallel positive shift without a change in the subthreshold swing, indicating that trap state generation is negligible and the degradation is caused by electron trapping.[3] Correspondingly, the on-state current shows a two-slope dependence on the gate bias in addition to the positive shift of the on-state current. ΔV_{on}, ΔV_{th1}, and ΔV_{th2} of the a-IGZO TFT after the stress are compared in Fig. 3. Note that ΔV_{on} is almost equal to ΔV_{th1} and larger than ΔV_{th2}. For example, after 3000 s stress time, ΔV_{on}, ΔV_{th1}, and ΔV_{th2} are 15.2 V, 15.3 V, and 14.0 V, respectively. The difference in the degradation of the subthreshold current and the on-state current indicates that electron injection occurs in a local region in the gate oxide or the ESL. The logarithmic relationship between the variations in V_{on}, V_{th1}, and V_{th2} and stress time indicates that a similar degradation mechanism is involved.

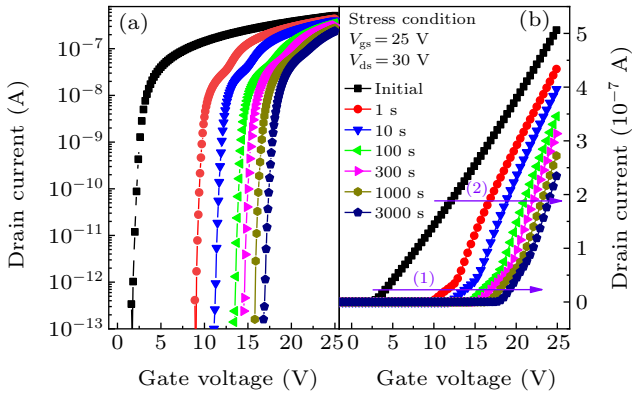


Fig. 2. Evolutions of the transfer curve measured at $V_{ds} = 0.1$ V for the a-IGZO TFTs on (a) logarithmic scale and (b) linear scale under the stress conditions of $V_{gs} = 25$ V and $V_{ds} = 30$ V.

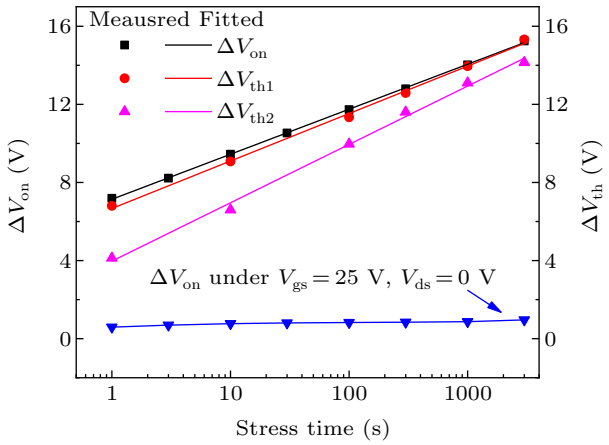


Fig. 3. Comparison of ΔV_{on}, ΔV_{th1}, and ΔV_{th2} of the a-IGZO TFT under bias stresses of $V_{gs} = 25$ V and $V_{ds} = 30$ V and ΔV_{on} under gate bias stresses of $V_{gs} = 25$ V and $V_{ds} = 0$ V. The fitting lines for the dependence of the variations in V_{on}, V_{th1}, and V_{th2} on stress time are added.

After fitting the initial transfer curves of the a-IGZO TFT with the Silvaco Atlas, density of states (DOS) in the channel a-IGZO is extracted and summarized in Table 1. Distributions of the vertical electric field (E_{vert}) and electron concentration (n_e) in the a-IGZO with $V_{gs} = 25$ V and $V_{ds} = 30$ V were then extracted. As shown in Fig. 4(a), the vertical electric field is strong at the back channel interface below the EDE region and at the front channel interface outside the EDE region, where the electric fields are 1.85×10^5 V/cm and 1.19×10^5 V/cm, respectively. For the distribution of electrons, as figure 4(b) shows, electrons also accumulate both at the back channel under the EDE region and at the front channel outside the EDE region, where the electron concentrations are 9.6×10^{18} cm^{-3} and 3.7×10^{18} cm^{-3}, respectively. Therefore, electron trapping during the bias stress could occur at both the back channel under the EDE region and the front channel outside the EDE region.

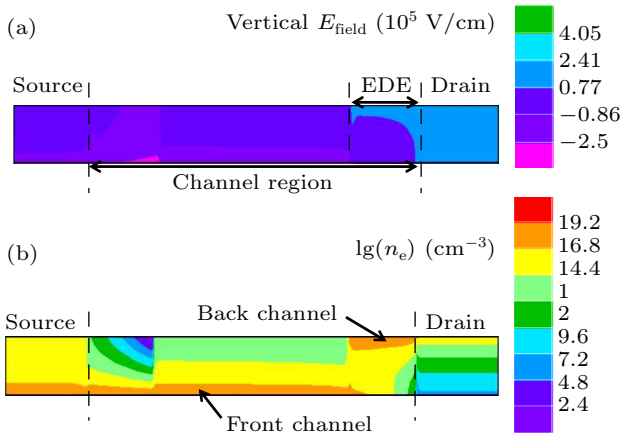


Fig. 4. Distributions of (a) vertical electric field and (b) electrons in a fresh a-IGZO TFT when $V_{gs} = 25$ V and $V_{ds} = 30$ V.

However, when a positive gate bias stress with V_{gs} of 25 V and grounded source/drain was applied, which produces the same electron concentration and electric field in the front channel as those outside the EDE region under $V_{gs} = 25$ V and

$V_{ds} = 30$ V, ΔV_{on} is smaller than 0.96 V, as shown in Fig. 3, indicating that electron trapping in the gate oxide is minimal, probably due to the good quality of the gate oxide, which limits the tunneling of electrons into the gate oxide.[11] Thus, the observed degradation under the simultaneous DC gate and drain biases is attributed to that occurring at the back channel under the EDE region.

To further clarify the degradation mechanism, the gate bias during the bias stress is decreased. As shown in Fig. 5(a), ΔV_{on} increases first and then decreases with the decrease of the gate bias, reaching a peak value at V_{gs} of 7 V. The maximum degradation of the a-IGZO TFT occurs when V_{gs} is relatively small rather than when both V_{gs} and V_{ds} are relatively large at the same time, indicating that the degradation is not dominated by the self-heating effect due to the Joule heat generated by the drain current and drain voltage.[12]

The increased temperature (ΔT) in the a-IGZO TFT during the bias stress with $V_{gs} = 25$ V and $V_{ds} = 30$ V is estimated through the following formula

$$\Delta T = R_{heat} \times P_{heat}, \tag{1}$$

where R_{heat} is the thermal resistance of the oxide layer and P_{heat} is the thermal power generated in the a-IGZO TFT. R_{heat} is estimated to be 1.3×10^3 K/W by the following formula

$$R_{heat} = L/(\lambda \times S), \tag{2}$$

where L is 350 nm, which is the sum of the thickness of the ESL and passivation layer; λ is 1.3, which is the coefficient of the thermal conductivity of SiO_2; and S is the heat dissipation area and is estimated by the product of W (10 μm) and L (20 μm). P_{heat} is estimated as 1.88 mW by the production of the drain voltage and the drain current of one fresh TFT. The increase in the temperature of the a-IGZO channel during bias stress is as small as 2.4 °C. Therefore, the effect of the heat generation during the bias stress on the degradation of a-IGZO TFTs is negligible.

Table 1. Parameters for the distribution of trap states for the simulation of the initial transfer curve of a-IGZO TFT.

Parameters	Value	Description
N_C (cm^{-3})	1×10^{19}	effective density of states (DOS) in conduction band
N_V (cm^{-3})	1×10^{19}	effective DOS in valence band
E_g (eV)	3.2	band-gap
μ_n (cm^2/V·s)	16	electron mobility
Acceptor-like DOS	$g_A(E) = N_{TA} \times \exp\left(\frac{E-E_C}{E_{TA}}\right) + N_{DA} \times \exp\left(\frac{E-E_C}{E_{DA}}\right)$	
N_{TA} (cm^{-3}·eV^{-1})	3×10^{18}	density of acceptor-like tail states at $E = E_C$
E_{TA} (eV)	0.081	characteristic decay energy for the acceptor-like tail states
N_{DA} (cm^{-3}·eV^{-1})	3.25×10^{17}	density of acceptor-like deep states at $E = E_C$
E_{DA} (eV)	0.6	characteristic decay energy for the acceptor-like deep states
Donor-like DOS	$g_D(E) = N_{TD} \times \exp\left(\frac{E_V-E}{E_{TD}}\right)$	
N_{TD} (cm^{-3}·eV^{-1})	1.55×10^{20}	density of donor-like tail states at $E = E_V$
E_{TD} (eV)	0.1	characteristic decay energy for the donor-like tail states
Shallow donor DOS	$g_{OV}(E) = N_{OV} \times \exp\left[-\left(\frac{E-E_{OV}}{\delta}\right)^2\right]$	
N_{OV} (cm^{-3}·eV^{-1})	2.2×10^{16}	peak of oxygen vacancy (OV) states
E_{OV} (eV)	2.9	mean energy of OV states
δ (eV)	0.1	standard deviation of OV states

From the simulation results in Fig. 5(b), the electron concentration at the back channel surface under the EDE region first increases quickly and then gradually as V_{gs} increases. In contrast, the vertical electric field is continuously reduced when V_{gs} increases. Under stresses of $V_{gs} = 25$ V and $V_{ds} = 30$ V, there is a high electron concentration but a low vertical electric field. In contrast, there is a small electron concentration but a high vertical electric field when V_{gs} is 0 V and 3 V. The gate bias of 7 V, which is slightly higher than the threshold voltage, provides both a relatively high electron concentration and electric field at the same time and induces maximum degradation of the a-IGZO TFT, which is a typical condition under which hot-carrier effects occur.

The ΔV_{on} after bias stresses with different V_{ds} are compared in Fig. 6, and a logarithmic time dependence is observed. The relationship between ΔV_{on} and stress time was fitted with $\Delta V_{on} = r_d \log(t/\tau_0)$,[13] where r_d is a function of the tunneling constant and τ_0 is the characteristic time. The logarithmic dependence on stress time indicates that the electrons were tunneled into and trapped in the ESL near the interface and did

not redistribute further after being trapped.[13–16] The dependence of ΔV_{th} on stress time in Fig. 3 can also be fitted with the logarithmic relationship, indicating that the same degradation mechanism is involved for the subthreshold current and on-state current.

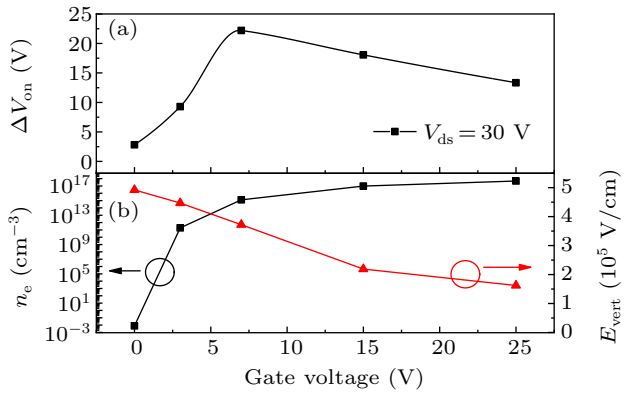


Fig. 5. (a) Effects of V_{gs} during bias stress with V_{ds} of 30 V on ΔV_{on} after 3000-s stress time; (b) simulated E_{vert} and n_e at back channel surface under EDE region when bias stresses with different V_{gs} are applied.

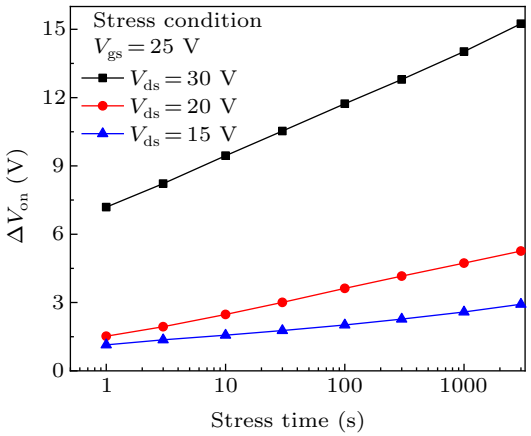


Fig. 6. Comparison of ΔV_{on} under bias stress condition with V_{gs} of 25 V but different V_{ds}.

Figure 7 shows the transfer curves measured at different drain biases after the a-IGZO TFT was stressed for 3000 s under $V_{gs} = 25$ V and $V_{ds} = 30$ V. Obviously, it can be seen that the drain bias during the measurement of the transfer curve affects the amount of the positive shift of the transfer curve. The electron trapped in the ESL under the EDE region induces a potential barrier with a height of 3.55 eV when $V_{ds} = 0.1$ V, as shown in Fig. 8, where electrons with a density of 2.15×10^{18} cm^{-3} are added in 10-nm regions in the ESL under the EDE region to account for the positive shift of the transfer curve. The potential barrier hinders the current flowing to the drain through the back surface of the a-IGZO under the EDE region. However, it is effectively lowered by a drain voltage higher than 10 V, and the current in the a-IGZO channel can flow freely from the source region to the drain region through the back surface of the a-IGZO under the EDE region, as in the fresh TFT, so the observed degradation, *i.e.*, the positive shift of the transfer curve, becomes minimal.

Figure 9 compares the output curves for the a-IGZO TFT before and after a bias stress of $V_{gs} = 25$ V and $V_{ds} = 30$ V. Current crowding appeared after the stress, and the current started to increase only when V_{ds} was larger than 5 V, which means that electrons could not drift freely from the source electrode to the drain electrode in the degraded TFT.[17] This is consistent with the potential barrier formed under the EDE region at the drain side owing to electron trapping after bias stress, which cannot be lowered under a small drain voltage and hinders the flow of electrons in the channel to the drain electrode. As shown in Fig. 9(a), current crowding also appeared in the output curves when V_{ds} was close to 0 V for a fresh TFT, which can also be explained by the same mechanism as electron trapping in the ESL under the EDE region during the measurement of the output characteristic curves.

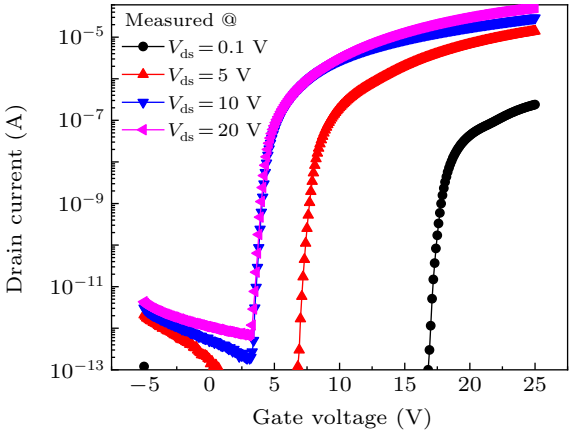


Fig. 7. Comparison of the transfer curves measured at different drain biases for the a-IGZO TFTs after 3000-s stress time under $V_{gs} = 25$ V and $V_{ds} = 30$ V.

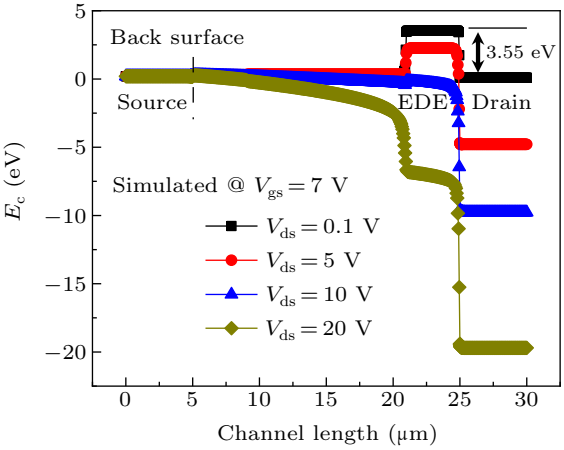


Fig. 8. Comparison of the conduction band at the back a-IGZO surface at different V_{ds} for the a-IGZO TFT after 3000-s stress time under $V_{gs} = 25$ V and $V_{ds} = 30$ V.

As shown in Fig. 10(a), electrons can accumulate in the front channel outside the EDE region with a small V_{gs} of 5 V after 100-s stress time under the default stress condition. However, the channel and accumulated electrons at the back channel under the EDE region disappeared when electrons with a density of 1.6×10^{18} cm^{-3} are added to the 10-nm regions in

the ESL under the EDE region to account for the positive shift of the transfer curve after 100 s under the default stress condition. The trapped electrons in the ESL under the EDE region increase the potential barrier of the a-IGZO channel under the EDE region, thereby increasing the threshold voltage of the parasitic TFT in the drain electrode region. In Fig. 10(b), one can notice that electrons can flow to the drain only when the gate bias is high enough to accumulate electrons in the front channel under the EDE and form the conduction path. Thus, the current crowding phenomena in the output curves starts at a smaller drain bias at a higher gate bias as shown in the Fig. 9. Therefore, the subthreshold current in Fig. 2(a) and the first linear dependence of the drain current on the gate bias in Fig. 2(b) are due to channel formation and current flow in the a-IGZO region outside the EDE region, where the channel length is long. The second linear dependence of the drain current on the gate bias in Fig. 2(b) is dominated by conduction in the channel formed under the EDE region when the gate bias is high enough, where the channel length is short.

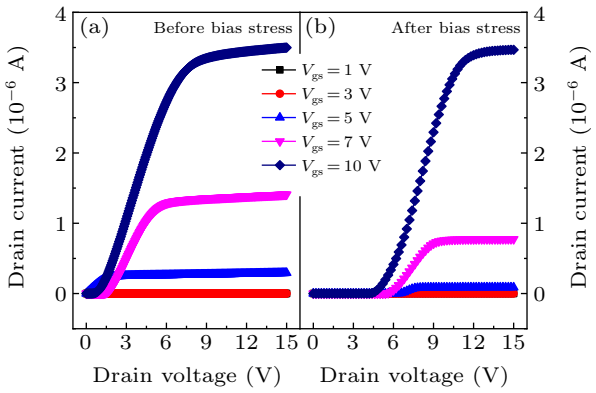


Fig. 9. Evolutions of the output curves for the a-IGZO TFTs (a) before and (b) after bias stresses of $V_{gs} = 25$ V and $V_{ds} = 30$ V.

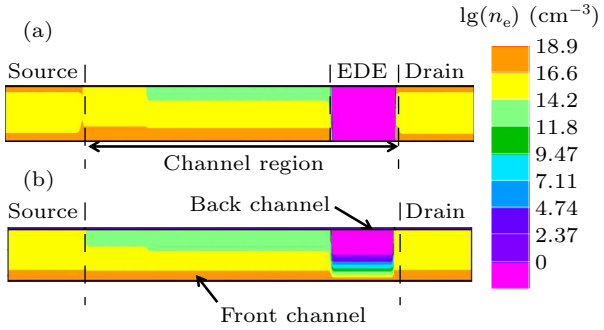


Fig. 10. Distribution of electrons in the a-IGZO at (a) $V_{ds} = 0.1$ V and $V_{gs} = 5$ V and (b) $V_{ds} = 0.1$ V and $V_{gs} = 25$ V, which is extracted for the TFTs after the default stress for 100 s.

As the tunneling of electrons into the ESL is the critical process during the degradation of the a-IGZO TFTs under the simultaneous DC gate and drain bias stress, the stability of the a-IGZO TFT can be enhanced by reducing the electric filed in the ESL under the EDE region, which can be achieved by either make the a-IGZO under the EDE region conductive[18] or increase the thickness of the ESL.

4. Conclusion

The a-IGZO TFTs with an ESL structure exhibit a positive shift of the transfer curve and two-slope dependence of the drain current on the gate bias after a simultaneous DC gate and drain bias stress. The degradation is proven to be a hot-carrier effect degradation and occurs locally in the back channel under the EDE region. Electron trapping in the ESL under the EDE region and the corresponding potential barrier formed in the back surface of channel a-IGZO successfully explained the observed degradation phenomena in both the transfer and output curves.

Acknowledgments

Project supported by the National Natural Science Foundation of China (Grant Nos. 61971299 and 61974101), the Natural Science Foundation of Jiangsu Province of China (Grant No. BK20201201), the Fund from Suzhou Science and Technology Bureau (Grant No. SYG201933), and the Fund from the State Key Laboratory of ASIC and System, Fudan University, (Grant No. 2021KF005).

References

[1] Kamiya T, Nomura K and Hosono H 2010 *Sci. Technol. Adv. Mater.* **11** 044305
[2] Lee J M, Cho I T, Lee J H and Kwon H I 2008 *Appl. Phys. Lett.* **93** 093504
[3] Cho E N, Kang J H, Kim C E, Moon P and Yun I 2011 *IEEE Transactions on Device and Materials Reliability* **11** 112
[4] Ji K H, Kim J I, Mo Y G, Jeong J H, Yang S, Hwang C S, Park S H K, Ryu M K, Lee S Y and Jeong J K 2010 *IEEE Electron Dev. Lett.* **31** 1404
[5] Ji K H, Kim J I, Jung H Y, Park S Y, Choi R, Kim U K, Hwang C S, Lee D, Hwang H and Jeong J K 2011 *Appl. Phys. Lett.* **98** 103509
[6] Wang L, Liu Y, Geng K W, Chen Y Y and En Y F 2018 *Chin. Phys. B* **27** 068504
[7] Urakawa S, Tomai S, Ueoka Y, Yamazaki H, Kasami M, Yano K, Wang D, Furuta M, Horita M, Ishikawa Y and Uraoka Y 2013 *Appl. Phys. Lett.* **102** 053506
[8] Lee S W, Jeon P J, Choi K, Min S W, Kwon H and Im S 2015 *IEEE Electron Dev. Lett.* **36** 472
[9] Zhang D, Wu C, Xu W, Ren F, Zhou D, Yu P, Zhang R, Zheng Y and Lu H 2019 *Chin. Phys. B* **28** 017303
[10] Liu F, Zhou Y, Yang H, Zhou X, Zhang X, Li G, Zhang M, Zhang S and Lu L 2022 *IEEE Electron Dev. Lett.* **43** 40
[11] Wei L, Locatelli M L, Diaham S, Pham C D, Grosset G and Dupuy L 2016 *IEEE International Conference on Dielectrics (ICD)* pp. 1061–1064
[12] Hsieh T Y, Chang T C, Chen T C, Chen Y T, Tsai M Y, Chu A K, Chung Y C, Ting H C and Chen C Y 2012 *IEEE Trans. Electron Dev.* **59** 3389
[13] Suresh A and Muth J F 2008 *Appl. Phys. Lett.* **92** 033502
[14] Liu T, Aygun L E, Wagner S and Sturm J C 2016 *IEEE Transactions on Device and Materials Reliability* **16** 243
[15] Lee J M, Cho I T, Lee J H, Cheong W S, Hwang C S and Kwon H I 2009 *Appl. Phys. Lett.* **94** 222112
[16] Powell M J 1983 *Appl. Phys. Lett.* **43** 597
[17] Wang S, Wang M, Zhang D and Shan Q 2018 *IEEE Trans. Electron Dev.* **65** 995
[18] Song T, Zhang D and Wang M 2021 *IEEE Electron Dev. Lett.* **42** 1623