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Degradation and breakdown behaviors of SGTs under repetitive unclamped inductive switching avalanche stress

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The repetitive unclamped inductive switching (UIS) avalanche stress is conducted to investigate the degradation and breakdown behaviors of conventional shield gate trench MOSFET (C-SGT) and P-ring SGT MOSFETs (P-SGT). It is found that the static and dynamic parameters of both devices show different degrees of degradation. Combining experimental and simulation results, the hot holes trapped into the Si/SiO_2 interface and the increase of crystal lattice temperature should be responsible for the degradation and breakdown behaviors. Moreover, under repetitive UIS avalanche stress, the reliability of P-SGT overcomes that of C-SGT, benefitting from the decreasing of the impact ionization rate at bottom of field oxide caused by the existence of P-ring.

Keywords: shield gate trench MOSFET, repetitive unclamped inductive switching stress, degradation, static and dynamic parameters

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1. Introduction

Benefitting from high current handle capability and low Miller capacitance (C_{GD}), shield gate trench (SGT) MOSFETs have shown great potential in automotive and industrial applications.[1,2] Unfortunately, when incorporated in power systems, the SGT MOSFETs suffer from unclamped inductive switching (UIS) stress, owing to the parasitic inductance or inductive load. This avalanche shock may lead to electrical degradation or severe failure to the Si-based power devices. So far, several constructive mechanisms have been proposed to explain the UIS degradation and failure behaviors. Kim and Ng *et al.* suggested that the degradation could be attributed to triggering the parasitic bipolar junction transistor (BJT).[3,4] Pawel *et al.* performed experiment and simulation, revealing that the inhomogeneous switching phenomenon may lead to degradation of avalanche current.[5] Chen *et al.* suggested that suppressing the channel conduction could improve UIS ruggedness.[6] Tian *et al.* investigated on failure mechanism caused by non-uniform potential distribution of the shield gate.[7] However, previous researches mainly focus on the single-pulse avalanche shock. In order to verify the long-term reliability of SGT MOSFETs, an in-depth investigation on the repetitive UIS avalanche degradation and breakdown behaviors is necessary, which could contribute to the improvement of UIS ruggedness.

In this work, the degradation of conventional SGT (C-SGT) MOSFETs and P-ring SGT (P-SGT) MOSFETs under repetitive avalanche stress is investigated. The static and dynamic parameters of the devices including drain leakage current (I_{DSS}), breakdown voltage (BV), threshold voltage (V_{th}), output capacitance (C_{OSS}) and reverse transfer capacitance (C_{RSS}) are monitored until breakdown. The degradation and failure mechanisms of the devices are discussed with the help of technology computer-aided design (TCAD) simulations and device failure photographs.

2. Device structure and experimental details

Figure 1 shows the cross-section views of the C-SGT and P-SGT fabricated by 0.5 μm PowerMOS manufacturing process in this work.

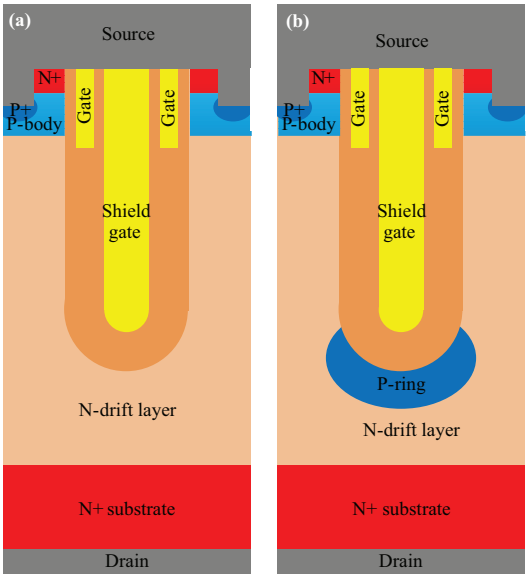


Fig. 1. Cross-section views of (a) C-SGT and (b) P-SGT.

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The key process flow of P-SGT is shown in Fig. 2. Firstly, the N-epi layer is grown on Si substrate. Then, the trench etching, boron ion implantation, thermal oxidation and polysilicon deposition are performed respectively. Next, the polysilicon is etched back to form the shield gate, followed by etching of oxide. After the formation of thin gate oxide, a polysilicon layer is deposited into the gate trenches and etched back to form the gate electrode. Finally, the formation of the P-body, N+ source region and the contacts can be realized by utilizing standard steps of a conventional trench MOSFET. Compared with C-SGT, an extra P-ring region is obtained by the boron ion implantation after trench etching. The introduction of P-ring decreases the electric field (EF) crowding taking place at the bottom of trench, resulting in the increase of *BV*. The main parameters of C-SGT and P-SGT are listed in Table 1.

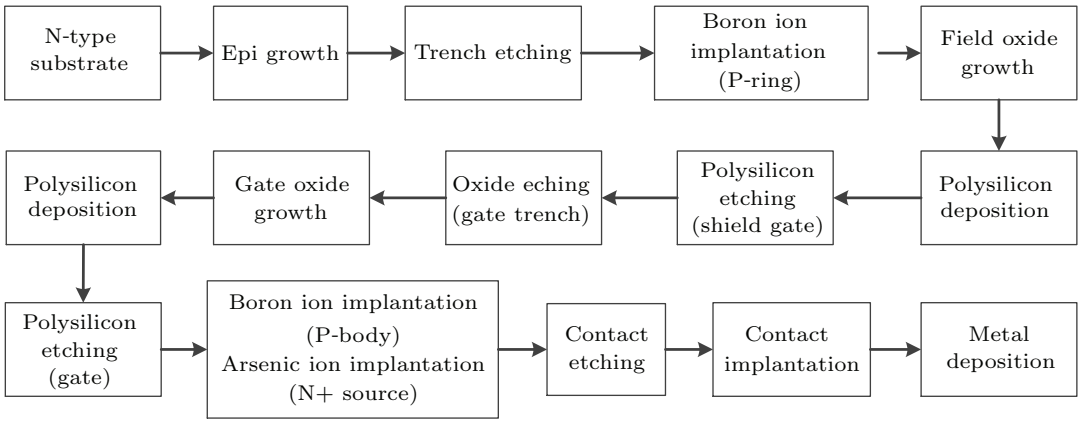


Fig. 2. The key process flow of P-SGT.

Table 1. Main parameters of C-SGT and P-SGT.

Parameter	C-SGT	P-SGT	Unit
Cell pitch	3	3	μm
Thickness of N-drift layer	9.5	9.5	μm
Depth of trench	5.5	5.5	μm
Width of trench	1.5	1.5	μm
Thickness of gate oxide	50	50	nm
Thickness of field oxide	500	500	nm
Concentration of N+ source	1×10^{20}	1×10^{20}	cm^{-3}
Concentration of P-body	7×10^{16}	7×10^{16}	cm^{-3}
Concentration of P-ring	–	2.5×10^{16}	cm^{-3}
Resistivity of N-drift layer	0.35	0.35	Ω·cm
Resistivity of N+ substrate	0.002	0.002	Ω·cm

The schematic of UIS test equivalent circuit is shown in Fig. 3. In the circuit, a 10 V pulse generator is adopted to switch the device under test (DUT) between ON-state and OFF-state, accompanied with a 25 Ω gate resistor. Meanwhile, a direct current (DC) voltage source of 50 V for C-SGT and 60 V for P-SGT is applied, according to the *BV* level of the DUT. A 0.5 mH inductance is used as an inductive load, which stores energy when the DUT turns on, and discharges the avalanche current through the device from drain to source when the DUT turns off. Figure 3(b) shows the schematic diagram of gate–source voltage (V_{GS}), drain–source voltage (V_{DS}), and drain–source current (I_{DS}) versus time of single-pulse UIS test. According to the equation

$$E_{AV} = \frac{1}{2} L I_{peak}^2, \tag{1}$$

the avalanche energy (E_{AV}) is 1.056 J for C-SGT and 1.156 J for P-SGT, respectively. To avoid the instantaneous failure, the selected E_{AV} is less than the single-pulse avalanche breakdown energy. Moreover, since Joule heating is the main cause of device breakdown,[8] a small air cooling equipment and copper heat sink are used to dissipate heat and decrease the influence of thermal accumulation.[9]

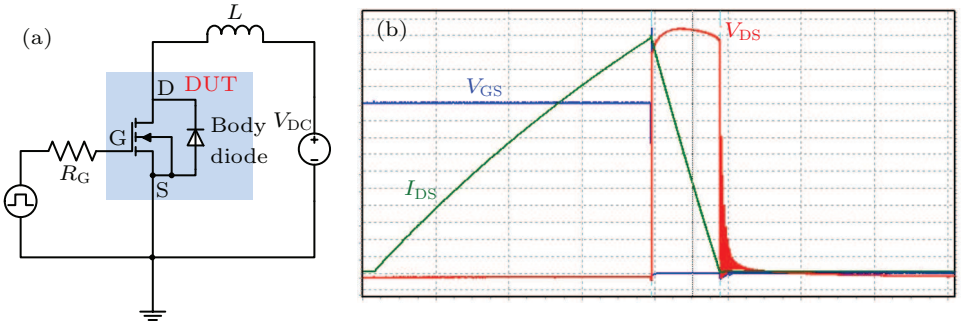


Fig. 3. (a) Schematic of UIS test equivalent circuit and (b) the schematic diagram of V_{GS}, V_{DS}, and I_{DS} versus time of single-pulse UIS test.

3. Results and discussion

Firstly, the impact of repetitive UIS stress on static parameters of DUTs are analyzed. In order to clarify the discharge path of UIS avalanche current, the mixed-mode simulation under the same UIS experiment condition is carried out by Sentaurus TCAD tools. Apart from some essential models (e.g., doping dependency, high field velocity saturation, Shockley–Read–Hall recombination and Auger recombination), bandgap narrowing and UNIBO avalanche model are considered.[10] Figure 4 shows the simulated avalanche current flow path and impact ionization (I.I.) distribution of C-SGT and P-SGT. It can be seen that the body diode and conductive channel are the discharge paths of avalanche current for both devices.

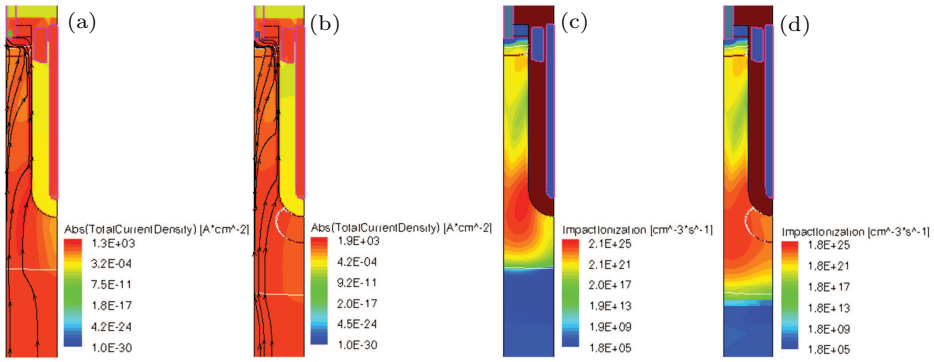


Fig. 4. Simulated avalanche current flow path of (a) C-SGT and (b) P-SGT and impact ionization distribution of (c) C-SGT and (d) P-SGT.

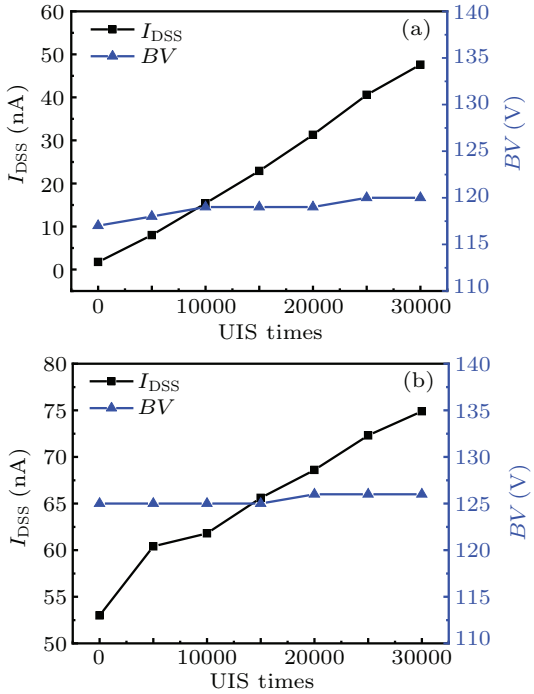


Fig. 5. Variation of I_{DSS} and BV for (a) CSGT and (b) P-SGT under repetitive UIS tests.

For the purpose of investigating the degradation of body diode and gate oxide, the static parameters including I_{DSS}, BV and V_{th} are monitored after every 5-k UIS tests until breakdown. In addition, the I_{DSS} is measured at $V_{GS} = 0$ V and $V_{DS} = BV$, the V_{th} is tested at $V_{GS} = V_{DS}$ and $I_{DS} = 250$ μA by Keysight B1506A at room temperature. As shown in Fig. 5, the I_{DSS} of C-SGT and P-SGT increase by 45.8 nA (2604%) and 21.9 nA (41.3%) from initial values after 30-k UIS tests, respectively. Meanwhile, the BV gradually increases before device breakdown as the number of UIS tests increases. Figure 6 depicts the variation of V_{th} for C-SGT and P-SGT under repetitive UIS tests. The measured results exhibit a slight decrease in V_{th} of C-SGT, but almost no degradation in that of P-SGT.

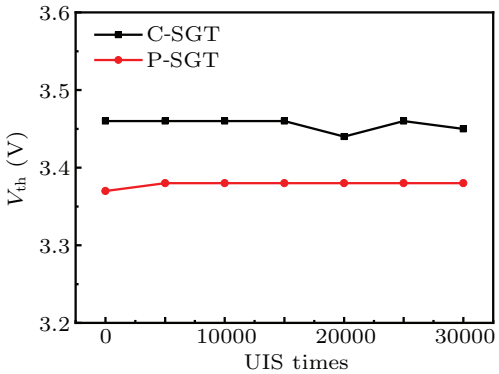


Fig. 6. Variation of V_{th} for C-SGT and P-SGT under repetitive UIS tests.

Combining above experimental and simulation results, the I_{DSS} degradation for both devices can be explained as following: due to the high I.I. along the gate oxide (shown in Fig. 4), the generated hot holes trapped into the Si/SiO_2 interface. To verify the influences of these trapped holes, the interface-trapped charges with uniform distribution are placed along the Si/SiO_2 interface of the devices in TCAD simulations. Figures 7(a), 7(b) and 7(d), 7(e) show the 2-D EF distribution in the fresh device and stressed device of C-SGT (with hole concentration of 7.9×10^{11} cm^{-2}) and P-SGT (with hole concentration of 7.1×10^{11} cm^{-2}) at $V_{DS} = 100$ V, respectively. The hole concentration is estimated according to the I_{DSS} of the 30000th UIS test. Figures 7(c) and 7(f) show the vertical EF curves along AA′ and BB′ cutline, respectively. As can be seen, compared with the fresh device, the holes injected into

the gate oxide widen the boundary of depletion layer toward the surface of stressed device for both devices. Correspondingly, the EF at the P-body/N-drift junction is enhanced, leading to an increase of I_{DSS}.

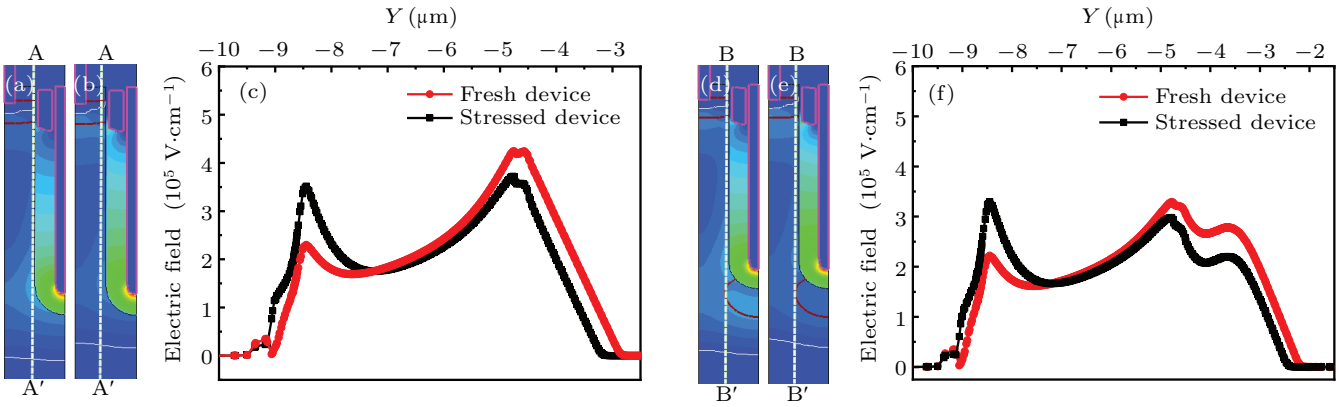


Fig. 7. The 2D EF distribution in the (a) fresh device and (b) stressed device of C-SGT, (c) vertical EF curves along AA′, and EF distribution in the (d) fresh device and (e) stressed device of P-SGT, (f) vertical EF curves along BB′.

Besides, it worth noting that the *BV* of both devices shows an increasing trend before breakdown (shown in Fig. 5). In order to explain this interesting phenomenon, the degradation process under repetitive UIS tests is simulated by increasing the trapped hole concentration of both devices. In Fig. 8, as the trapped holes concentration increases, the *BV* of both devices rise initially and then start to drop rapidly when the trapped holes concentration exceeds 8.3×10^{11} cm^{-2}.[11] It implies that if the number of UIS tests exceeds a certain value, the DUTs are facing extreme high EF at the gate oxide, a rapid increase of trapped hole concentration and instantaneous breakdown, which is in good agreement of preceding experiment results.

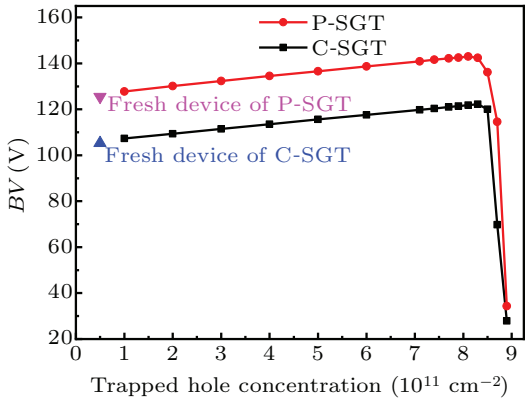


Fig. 8. The *BV* of C-SGT and P-SGT with different trapped hole concentration.

To prove the mechanism of the holes trapping, the *BV* of C-SGT and P-SGT are monitored under the ambient temperature of 450 K after the repetitive avalanche. As shown in Fig. 9, the *BV* of both devices recover with the time increasing, because of the detrapping of holes from the SiO_2 dielectric layer under high temperature.[11]

Further, considering the switching applications of power devices, the degradation of dynamic characteristics for C-SGT and P-SGT are investigated. In SGT MOSFETs, the shield gate is introduced to alleviate the EF non-uniformity in N-type epitaxial layer and reduce gate-to-drain capacitance (C_{GD}). However, the output capacitance (C_{OSS}) is several times greater than the single-gate trench MOSFET, causing a reduction in the switching frequency.[12] Therefore, we focus on the dynamic parameter of C_{OSS} in this work.

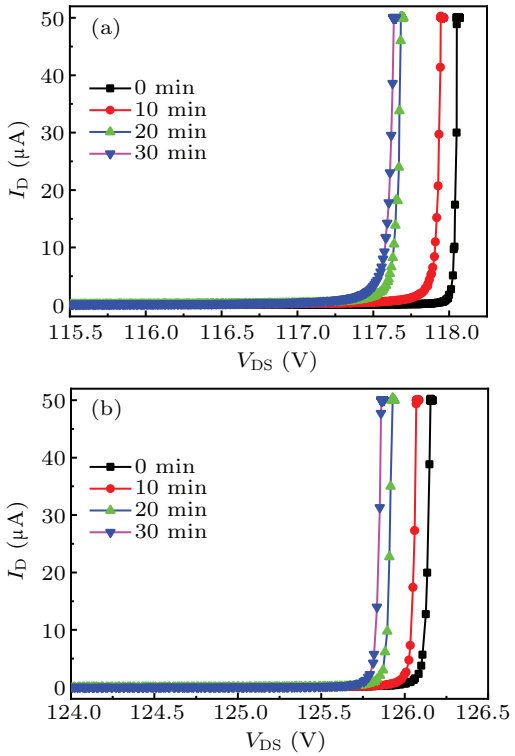


Fig. 9. The *BV* variations of (a) C-SGT and (b) P-SGT under the ambient temperature of 450 K after the repetitive avalanche.

Figure 10 shows the C_{OSS} and C_{RSS} of C-SGT and P-SGT after every 10-k UIS tests until breakdown. In the *C*–*V* measurement, the frequency used is 1 MHz. As shown in Fig. 10(a), the C_{OSS} of C-SGT significantly increases when the drain voltage is in the range of 35 V to 60 V, while the C_{RSS}

shows no degradation. Since the C_{OSS} is composed of the gate-drain capacitance (C_{GD}, also called C_{RSS}) and the drain–source capacitance (C_{DS}), the variation of C_{OSS} is mainly caused by the increase of C_{DS}. The increase of C_{DS} is owing to the reduction of depletion layer of P-body/N-drift junction (shown in Fig. 7), caused by the hot holes injected into the field oxide during repetitive UIS stress. In P-SGT, the C_{OSS} and C_{RSS} almost remain unchanged, benefitting from the decreasing of the impact ionization rate at bottom of field oxide caused by the existence of P-ring.[13]

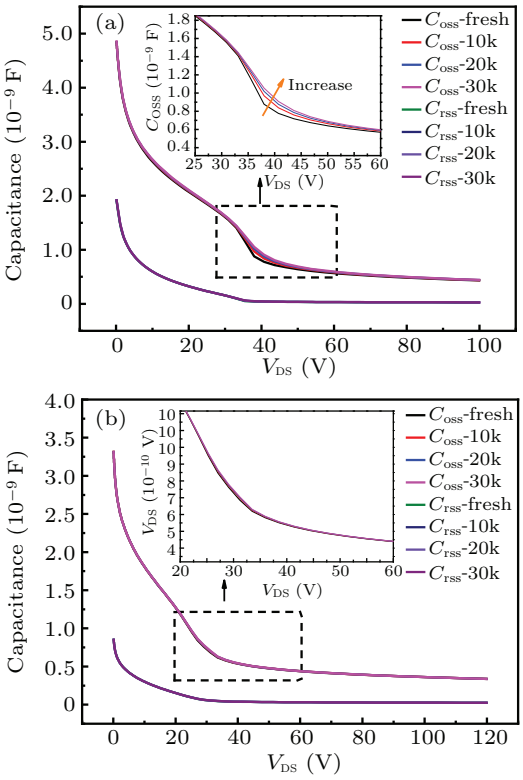


Fig. 10. The C_{OSS} and C_{RSS} of (a) C-SGT and (b) P-SGT measured after every 10-k UIS tests.

After repetitive avalanche breakdown, the de-capsulation of DUTs are carried out. The source metal on the surface of the DUTs are removed using hydrochloric acid. Figure 11 shows the failure photographs of C-SGT and P-SGT, respectively. In both devices, the failure points are located in the cell region instead of the termination region, illustrating that the termination plays an important protective role in repetitive UIS avalanche stress. Based on the above analysis, two reasons may account for repetitive avalanche breakdown. Firstly, the high I.I. arouses a raised electron-hole combination in the P-body/N-drift junction. Since the energy released by combination is absorbed by the crystal lattice of silicon material, it leads to an increase of lattice temperature. When the temperature approaches the intrinsic temperature, the device thermal breakdown. Secondly, the injection of holes into the gate oxide layer increases the EF near the gate oxide. When the EF near the gate oxide exceeds the EF near the field oxide, the device breakdown.

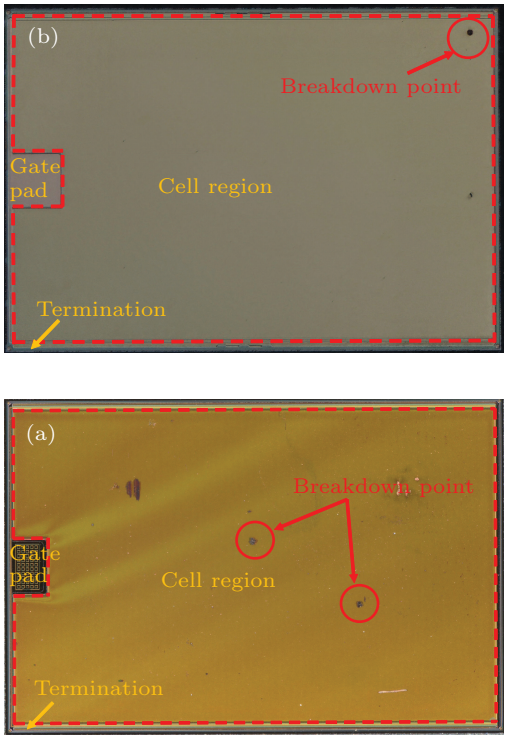


Fig. 11. The failure photographs of (a) C-SGT and (b) P-SGT.

4. Conclusion and perspectives

The degradation and breakdown behaviors of C-SGT and P-SGT under repetitive avalanche stress is investigated in detail. As the hot holes are continuously injected into the Si/SiO_2 interface and the lattice temperature increases, both devices feather different degrees of degradation on static and dynamic parameters. Furthermore, compared with C-SGT, the P-SGT suffer from limited damage of body diode and oxide layer, benefitting from the grounded shield gate and floating P-ring. In term of the long-term reliability of SGT-MOSFETs in practical applications, the degradation of I_{DSS}, BV and C_{OSS} should be carefully considered.

Acknowledgements

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