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# Improvement on short-circuit ability of SiC super-junction MOSFET with partially widened pillar structure

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A novel 1200 V SiC super-junction (SJ) MOSFET with a partially widened pillar structure is proposed and investigated by using the two-dimensional numerical simulation tool. Based on the SiC SJ MOSFET structure, a partially widened P-region is added at the SJ pillar region to improve the short-circuit (SC) ability. After investigating the position and doping concentration of the widened P-region, an optimal structure is determined. From the simulation results, the SC withstand times (SCWTs) of the conventional trench MOSFET (CT-MOSFET), the SJ MOSFET, and the proposed structure at 800 V DC bus voltage are 15 μs, 17 μs, and 24 μs, respectively. The SCWTs of the proposed structure are increased by 60% and 41.2% in comparison with that of the other two structures. The main reason for the proposed structure with an enhanced SC capability is related to the effective suppression of saturation current at the high DC bias conditions by using a modulated P-pillar region. Meanwhile, a good Baliga's FOM ($BV^2/R_{on}$) also can be achieved in the proposed structure due to the advantage of the SJ structure. In addition, the fabrication technology of the proposed structure is compatible with the standard epitaxy growth method used in the SJ MOSFET. As a result, the SJ structure with this feasible optimization skill presents an effect on improving the SC reliability of the SiC SJ MOSFET without the degeneration of the Baliga's FOM.

**Keywords:** silicon carbide (SiC), short-circuit (SC), super-junction (SJ), trench MOSFET

**PACS:** 85.30.–z, 85.30.De **DOI:** 10.1088/1674-1056/ac6159

## 1. Introduction

Compared with the power devices by using the matured silicon materials, the devices with silicon-carbide (SiC) materials can achieve a superior performance owing to the excellent material properties such as wide energy band gap, low intrinsic carrier concentration, and high breakdown electric field.[1,2] In recent years, the commercial SiC power MOSFETs have been regarded as promising candidates to replace the conventional silicon power devices. Meanwhile, the reliability issues are always accompanying the SiC MOSFETs in the harsh application conditions, and more research resources are required to meliorate the device's performance. The short-circuit (SC) failure is one of the most serious reliable issues for SiC power devices. During the SC transient process, the high DC bus voltage and the large saturation current will be applied to the device, resulting in the device's performance degradation or even severe burnout failure if the device is without sufficient SC withstand ability. Therefore, the enhancement of the SC robustness is always a main concern of researchers.

Benefitting from the high-power density, high integration, and low on-resistance, the SiC trench MOSFETs have become the widely used devices in power electronic systems. Many previous studies have focused on the SC failure mode and the comparison of SC performance between the trench structure and the planner structure.[3–17] Unfortunately, these results showed that a weaker SC robustness is found in the SiC trench MOSFET due to its higher power density.[5–7] Whereas, only a few studies on improving the SC reliability of the SiC trench MOSFETs are given. Okada *et al*. have demonstrated the improvement of SC reliability with the SiC SJ trench MOSFET structure,[18] but further structure optimization still needs to be carried out to enhance the SC reliability.

In this paper, a 1200 V SiC SJ MOSFET with a partially widened pillar structure is given by using the Sentaurus TCAD simulation tool.[19] Based on the altered pillar structure, the proposed structure can provide a superior SC ability and maintain a good Baliga's FOM ($BV^2/R_{on}$) simultaneously. Firstly, the basic parameter characteristics of the conventional trench MOSFET (CT-MOSFET), the SJ MOSFET, and the proposed device are compared. Subsequently, the SC characteristics of all devices are investigated under the varied SC pulse time. Finally, the variation of structural parameters for the P-pillar modulation region is analyzed to achieve an optimal device's performance.

## 2. Device structures and simulation setup

Figure 1 shows the cross-sectional schematics of three 1200V SiC MOSFETs investigated in this paper. All devices are designed with an identical epitaxy thickness of 12 μm and doping concentration of $3\times10^{15}$ cm$^{-3}$. Uniform

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channel length (0.8 μm) and P-body doping concentration of $2\times10^{17}$ cm$^{-3}$ at the channel area are used to achieve the same threshold voltage ($V_{th}$). The channel electron mobility is set at 20 cm$^2$/V·s. The current spreading layer (CSL) is added to optimize the on-current capability. The new structure with a partially widened pillar region is shown in Fig. 1(c), where a P-pillar modulation region is extended into the N-pillar. The doping concentration of the P-pillar modulation region keeps consistent with that of P-pillars. The detailed structure dimensions and doping concentration are listed in Table 1. $H_m$ is the distance from the center position of the P-pillar modulation region to the top, and the width of the P-pillar modulation region is defined as $W_m$, as indicated in Fig. 1(c). The fabrication process of the proposed structure is compatible with standard trench SJ MOSFET by using the multiple epitaxial layers growth and ion-implantation,[20,21] as illustrated in Fig. 2. And it only needs to adjust the implanting window at the corresponding position to form the partially widened P-pillar region.

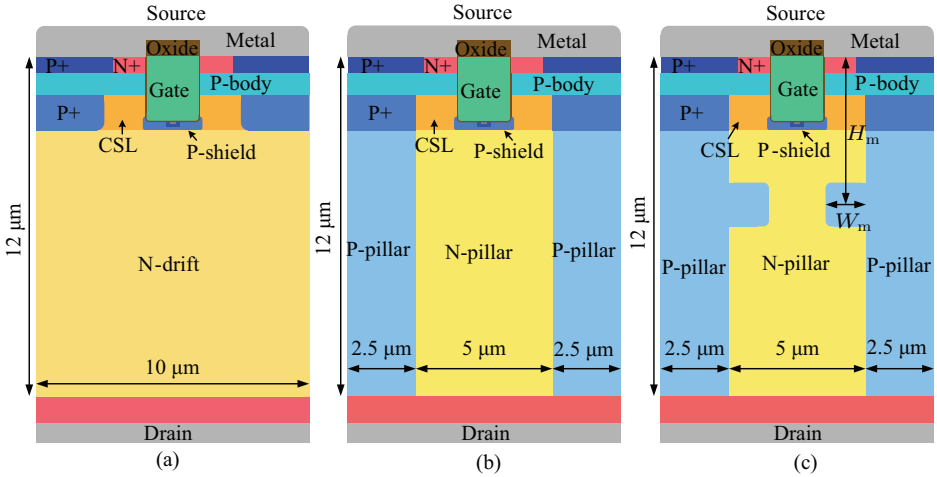



**Fig. 1.** Schematic cross-sectional views (not to scale) of (a) the CT-MOSFET, (b) the SJ MOSFET, (c) the proposed structure.

**Table 1.** Detailed structure parameters of devices.

| Device parameters | CT-MOSFET | SJ MOSFET | Proposed structure |
|---|---|---|---|
| N+ source depth (μm) | 0.2 | 0.2 | 0.2 |
| N+/P+ doping (cm$^{-3}$) | $1\times10^{19}$ | $1\times10^{19}$ | $1\times10^{19}$ |
| Gate oxide thickness (nm) | 50 | 50 | 50 |
| P-body depth (μm) | 0.8 | 0.8 | 0.8 |
| P-body doping (cm$^{-3}$) | $2\times10^{17}$ | $2\times10^{17}$ | $2\times10^{17}$ |
| N-CSL depth (μm) | 1.3 | 1.3 | 1.3 |
| N-CSL doping (cm$^{-3}$) | $1.1\times10^{16}$ | $1.1\times10^{16}$ | $1.1\times10^{16}$ |
| P+ region doping (cm$^{-3}$) | $8\times10^{17}$ | $8\times10^{17}$ | $8\times10^{17}$ |
| P-shield depth (μm) | 0.3 | 0.3 | 0.3 |
| P-shield doping (cm$^{-3}$) | $8\times10^{17}$ | $8\times10^{17}$ | $8\times10^{17}$ |
| N-drift thickness (μm) | 9.7 | – | – |
| N-drift doping (cm$^{-3}$) | $3\times10^{15}$ | – | – |
| N/P-pillar doping (cm$^{-3}$) | – | $1\times10^{16}$ | $1\times10^{16}$ |
| N/P-pillar thickness (μm) | – | 9.7 | 9.7 |
| N /P-pillar width (μm) | – | 5 | 5 |
| $H_m$ (μm) | – | – | 5 |
| $W_m$ (μm) | – | – | 1.5 |
| P-pillar modulation doping (cm$^{-3}$) | – | – | $1\times10^{16}$ |

To achieve more accurate simulation results, a series of physical models including Shockley–Read–Hall (SRH), Auger recombination, anisotropic avalanche (Okuto–Crowell model), incomplete ionization, and mobility degradation by the normal electric field (Enormal) are added in simulation settings. In addition, the thermodynamic model is employed to describe the electrothermal coupling behavior when the device is subjected to a high current density during the SC process. The active area of the chip in this paper is designed with 35 mm$^2$.

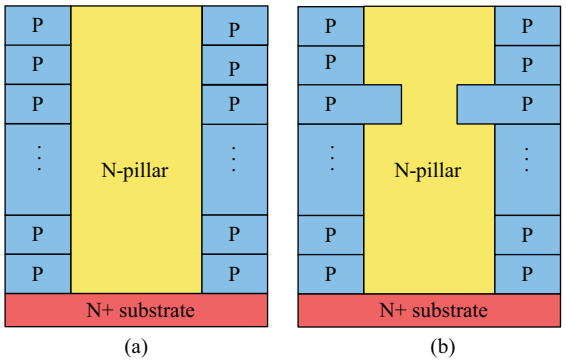



**Fig. 2.** The main fabrication flow of two structures: (a) the SJ structure and (b) the proposed structure with the partially widened pillar.

## 3. Results and discussion

### 3.1. Static parameters

Figure 3 illustrates the simulation results of static characteristics for the aforementioned three MOSFETs. From Fig. 3(a), it can be seen that the $V_{th}$ curves of the three structures almost completely overlap, and the $V_{th}$ of all devices at $I_{ds} = 1$ mA is maintained at 2.19 V owing to the same structure and doping concentration of the channel region. Figure 3(b) shows that the breakdown voltages ($BV$) for three structures at $I_{ds} = 1$ μA are 1913 V, 1836 V, and 1802 V, respectively. All of the structures meet the basic requirement of the 1.2 kV

device design. A little lower $BV$ value in SJ structure can be noted, which is consistent with the previous study.[20]

According to the simulation results of $I$–$V$ characteristics shown in Fig. 3(c), the on-state resistance ($R_{on}$) at the current of 30 A are 40.2 mΩ, 25.4 mΩ, and 29.3 mΩ, respectively. It is worth noting that the $R_{on}$ of the proposed structure is slightly higher compared with the conventional SJ MOSFET due to the narrowing of the current path induced by the partially widened pillar region. But this $R_{on}$ value is obviously smaller than the CT-MOSFET due to the advantages of the N-pillar. In addition, the Baliga's figures of merit (Baliga's FOM $= BV^2/R_{on}$) of all structures are calculated to evaluate overall static performance. It can be found in Table 3 that the Baliga's FOM of SJ MOSFET and the proposed structure are increased by 46.2% and 22% compared with the CT-MOSFET, respectively. Therefore, the proposed structure can maintain a good static ability owing to the advantages of the SJ structure.

As given in Fig. 3(d), the $I_{ds}$ for three structures at $V_{ds} =$ 800 V are 287 A, 278 A and 247 A, respectively. The saturation current value of the SJ MOSFET is close to that of the CT-MOSFET, indicating a similar SC ability. However, the saturation current of the proposed structure is significantly reduced. Under the high $V_{ds}$, the widened P-pillar depletes the N-pillar further and narrows the current path, resulting in the lower saturation current in the proposed structure. Therefore, a superior SC capability at the high drain voltage can be demonstrated.

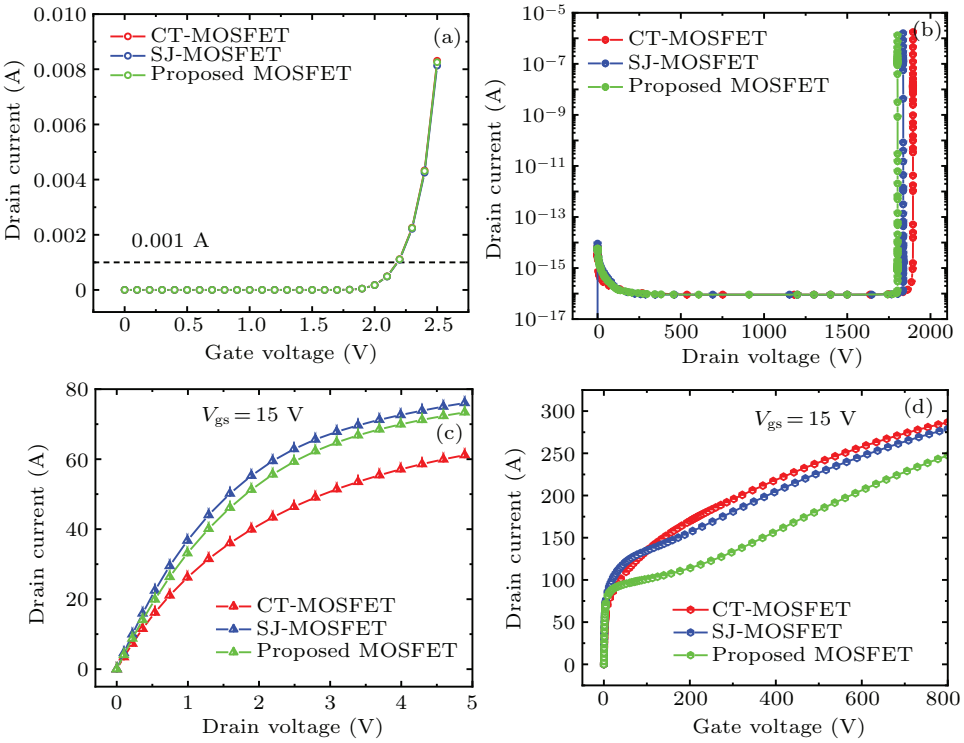



**Fig. 3.** The comparison of simulation results (a) the threshold voltage, (b) the breakdown voltage, (c) the forward $I$–$V$ characteristic and (d) the saturation characteristic.

In addition, it can be noted in Fig. 3(d) that an incomplete saturation state of the $I_{ds}$ curves is found with the increase of drain voltage. The reason is related that the P+ area blocks the depletion layer extension in the P-body during the increasing of $V_{ds}$. Therefore, the pinch-off effect of the channel is affected inevitably, resulting in an incomplete saturation condition.

### 3.2. Optimization of pillar doping concentration in the SJ MOSFET

Obviously, the pillar doping concentration will influence the device characteristics in the SJ MOSFET. It is necessary to select an appropriate pillar doping concentration to achieve optimal performance, and the N-pillar and P-pillar have the same width to maintain charge balance. The static parameters with the variation of pillar doping concentration are illustrated in Fig. 4.

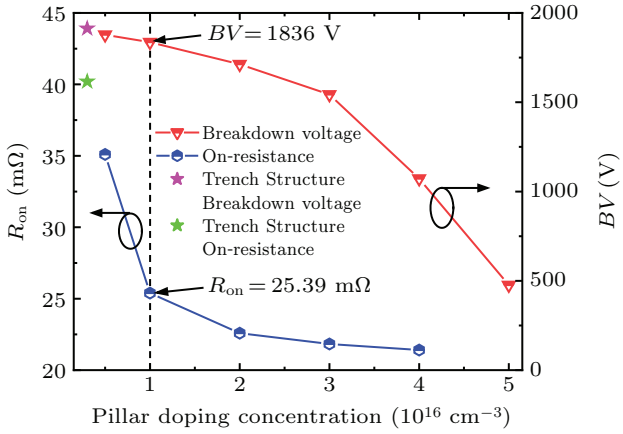



**Fig. 4.** The static performance of the SJ MOSFET with different pillar doping concentrations.

**Table 2.** The simulation results of the SJ MOSFET with varied pillar doping.

| Pillar doping concentration ($cm^{-3}$) | $BV$ (V) | $R_{on}$ (mΩ) | Baliga's FOM (MW) | Saturation current (A) ($V_{ds}$ = 800 V) |
|---|---|---|---|---|
| $5\times10^{15}$ | 1878 | 35.1 | 100 | 263 |
| **$1\times10^{16}$** | **1836** | **25.39** | **133** | **278** |
| $2\times10^{16}$ | 1713 | 22.59 | 130 | 300 |
| $3\times10^{16}$ | 1543 | 21.83 | 109 | 307 |
| $4\times10^{16}$ | 1072 | 21.41 | 53.7 | 314 |

The exact values of the static parameters, the Baliga's FOM, and the saturation current at $V_{ds}$ = 800 V are given in Table 2.

As shown in Fig. 4, the $R_{on}$ and $BV$ of the SJ MOSFET decrease gradually with the pillar doping concentration increasing from $5\times10^{15}$ $cm^{-3}$ to $5\times10^{16}$ $cm^{-3}$. The $BV$ decreases quickly when the pillar concentration exceeds $4\times10^{16}$ $cm^{-3}$, and the $R_{on}$ presents a sudden increase when the pillar concentration drops to $5\times10^{15}$ $cm^{-3}$. Meanwhile, the saturation current of the SJ structure is higher than that of the CT-MOSFET when pillar concentration exceeds $1\times10^{16}$ $cm^{-3}$ from Table 2, indicating a poor SC characteristic. Therefore, the value of $1\times10^{16}$ $cm^{-3}$ is the optimal pillar doping concentration of the SJ structure in this simulation MOSFET after the selection between Baliga's FOM and SC ability.

### 3.3. The SC simulation results and analysis of the three different structures

The circuit of short-circuit mixed-mode simulation is shown in Fig. 5. The parameters are set as follows: the parasitic inductance ($L_p$) is 200 nH, the DC drain–source voltage is 800 V[6,13,14], and the gate resistance ($R_g$) is 2.5 Ω. The single pulse gate voltage of 15 V/0 V with varied pulse times is applied to control the SC times. The simulation waveforms of the drain-source voltage ($V_{ds}$), the drain current ($I_{ds}$), and the lattice temperature ($T_{max}$) are captured to inspect the SC performance.

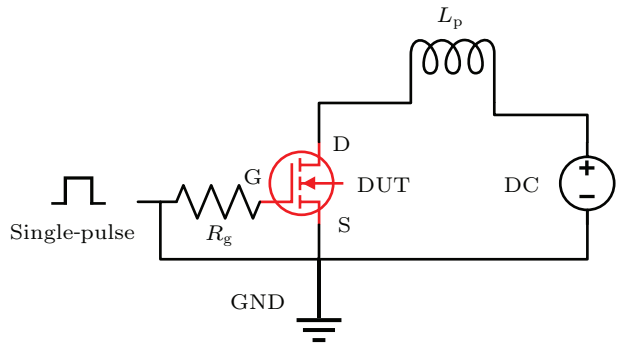



**Fig. 5.** Schematic of circuit used for SC simulation in this paper.

The SC waveforms under different gate pulses of the CT-MOSFET are shown in Fig. 6. It is found that the $I_{ds}$ gradually decreases to 0 A at $T_{pulse}$ =15 μs, which means the device is at normal turn-off condition. Once the gate pulse time ($T_{pulse}$) increases to 16 μs, the $I_{ds}$ cannot drop to 0 A and shows a gradual increase at the final time of the SC process, indicating an abnormal turn-off process. Furthermore, it can be seen that a rapid increase of the $I_{ds}$ when the $T_{pulse}$ increases to 20 μs, resulting in a severe burnout failure. Therefore, the SC withstand time (SCWT) of the CT-MOSFET is 15 μs, and the SC saturation current is about 495 A, as given in Fig. 6.

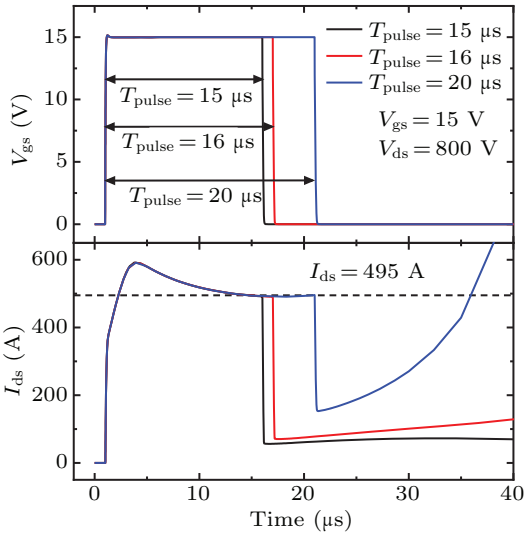



**Fig. 6.** The SC simulation results of the CT-MOSFET under different gate pulses.

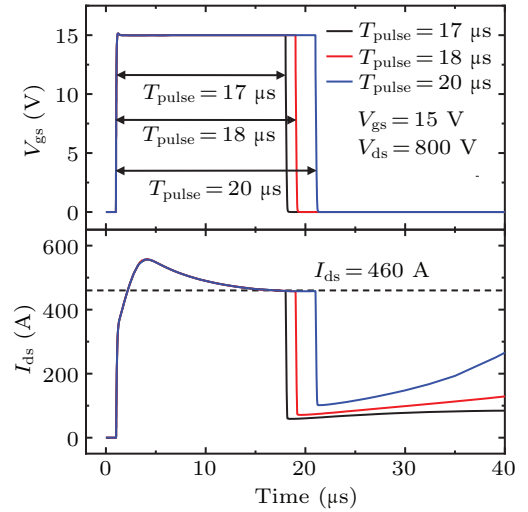



**Fig. 7.** The SC simulation results of the SJ MOSFET under different gate pulses.

A similar situation of the SJ MOSFET can be found in Fig. 7. The SC saturation current of the SJ MOSFET is about 460 A, which is slightly lower than that of the CT-MOSFET.

Thus, the SCWT of the SJ MOSFET is 17 μs. The SJ MOSFET shows a slightly better SC performance than the CT-MOSFET, which is consistent with the results given by Okada *et al.*[17]

Figure 8 shows that the SC saturation current of the proposed structure is about 360 A, which is much less than the other two structures. The SCWT is increased to 24 μs, which is improved by 60% and 41.2% compared with the CT-MOSFET and SJ MOSFET, respectively. All parameters comparison of the three structures obtained from the simulation is summarized in Table 3.

It can be inferred from the above discussion that the burnout failure occurs after the devices are subjected to a harsh SC pressure. The internal lattice temperature rises rapidly due to the high SC current and voltage, then the electro-thermal coupling effect with the positive feedback phenomenon will occur continually. After a long SC time, the current inside the device still rises sharply even if the gate is turned off, resulting in the dynamic avalanche breakdown and heat accumulation at the local region. Thus, this failure is directly affected by the magnitude of the SC current, and the device with a lower SC current demonstrates a robust SC withstand ability.

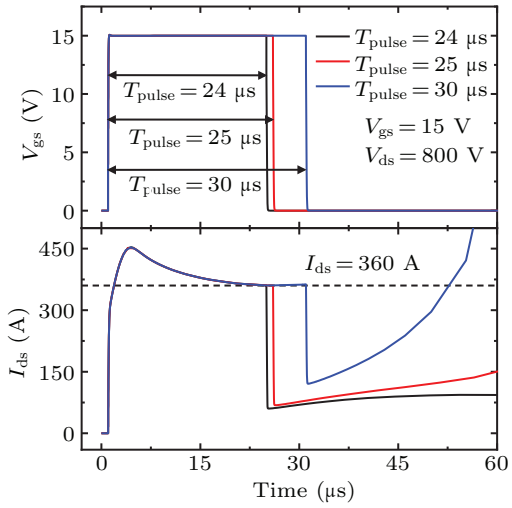



**Fig. 8.** The SC simulation results of the proposed structure under different gate pulses.

**Table 3.** The simulation results of the three different MOSFETs.

| Structure | *BV* (V) | $R_{on}$ (mΩ) | Baliga's FOM (MW) | SC saturation current (A) | SCWT (μs) |
|---|---|---|---|---|---|
| CT-MOSFET | 1913 | 40.2 | 91 | 495 | 15 |
| SJ MOSFET | 1836 | 25.4 | 133 | 460 | 17 |
| Proposed structure | 1802 | 29.3 | 111 | 360 | 24 |

### 3.4. Analysis of the physical mechanism inside the devices

To analyze the inner physical mechanism of different SC abilities, as shown in Fig. 9, the same gate voltage pulse time of 20 μs is applied to the three structures. The distribution of the electric field, the total current density, and the lattice temperature at the time points 20 μs and 40 μs are obtained in Figs. 10, 11, and 12, respectively. From the comparison waveforms, the proposed structure can turn off safely, while the CT-MOSFET and the SJ MOSFET fail at this SC pressure.

From Fig. 9, it can be seen that the $I_{ds}$ increases firstly and then decreases during the SC process. We believe that these changes are attributed to the channel mobility. The rise of $I_{ds}$ at the beginning is related to the weakening of Coulomb scattering mechanism from two aspects. The inversion charge increases with the rise of lattice temperature when the channel is formed, and the influence of Coulomb scattering on carrier mobility was shielded by abundant free electrons. In addition, the trapped charge reduces due to the energy band narrowing with the lattice temperature rising, then the Coulomb scattering effect caused by the interface charged center is weakened. Subsequently, the continuous increase in lattice temperature leads to the increase of surface roughness scattering and phonon scattering, which in return causes the decrease of inversion layer carrier mobility and the subsequent decline of SC current.

As shown in Fig. 10, the distribution of electric field is changed due to the addition of the partially widened p-pillar. Most importantly, the cumulation of the electric field at the trench bottom area is suppressed. It can be seen that the high electric field is transferred to the bottom of the widened P-pillar region, which also helps to protect the gate oxide below the trench.

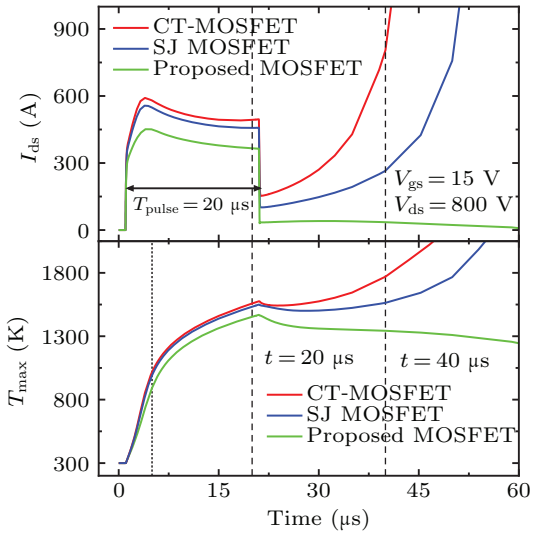



**Fig. 9.** Comparative simulation results of the three different structures under the same gate pulse of 20 μs, including the waveforms of $I_{ds}$ and $T_{max}$.

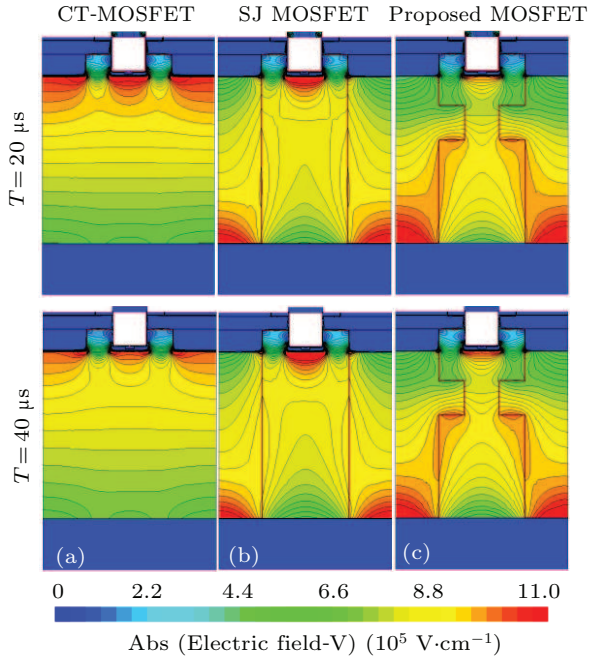



**Fig. 10.** Simulation results of electric field distribution inside the devices at time points 20 μs and 40 μs for (a) the CT-MOSFET, (b) the SJ MOSFET, (c) the proposed structure.

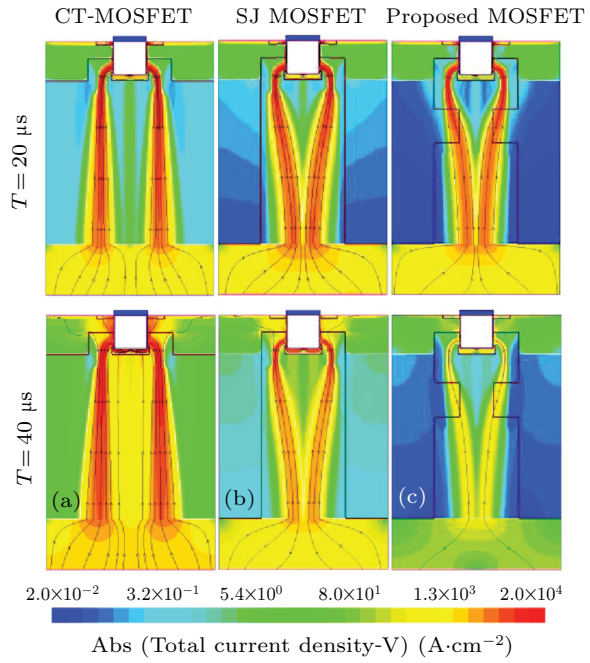



**Fig. 11.** Simulation results of total current density distribution inside the devices at time points 20 μs and 40 μs for (a) the CT-MOSFET, (b) the SJ MOSFET, (c) the proposed structure.

As depicted in Fig. 11, the current flowing path of the proposed device is modulated compared with the CT-MOSFET and the SJ MOSFET. It can be seen that the widened P-pillar region squeezes the electron flowing path in the N-pillar, which is similar to the JFET effect in the planar DMOSFET. Meanwhile, when the proposed structure is under a high $V_{ds}$, the hot spot is transferred to the widened P-pillar region, as illustrated in Fig. 12. Therefore, the huge SC saturation current caused by the larger avalanche injection is weakened. Although, it can be seen that the current still flow within the widened P-pillar region due to the dynamic avalanche accumulation at that area. But the saturation current is suppressed effectively.

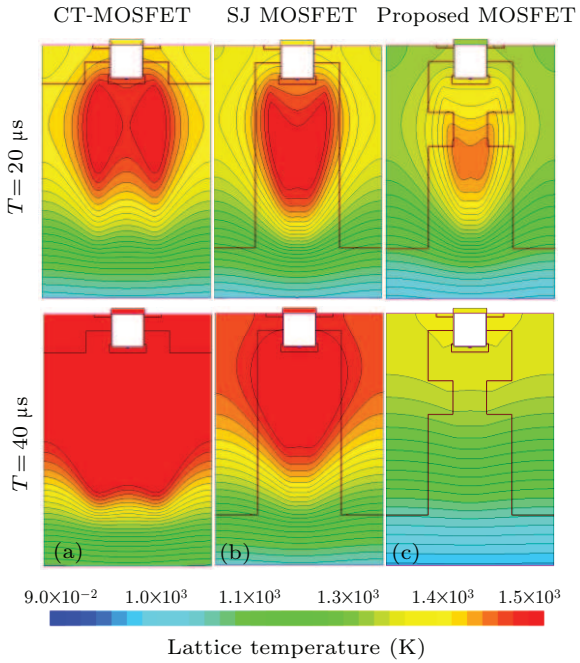



**Fig. 12.** Simulation results of lattice temperature distribution inside the device at time points 20 μs and 40 μs for (a) the CT-MOSFET, (b) the SJ MOSFET, (c) the proposed structure.

Under the influence of electric field and current density, the internal peak junction temperature of the proposed structure is significantly lower than that of the CT-MOSFET and the SJ MOSFET at times 20 μs and 40 μs, as shown in Fig. 12. Consequently, the electro-thermal coupling effect with the positive feedback phenomenon is suppressed in the proposed structure, resulting in the improvement of the SC reliability.

### 3.5. Proposed structure parameters optimization

The influence of structure parameters in the proposed structure is investigated, including the position ($H_m$) and width ($W_m$) of the P-pillar modulation region. The doping concentration of the P-type region is fixed at $1\times10^{16}$ cm$^{-3}$ as the same with the aforementioned SJ MOSFET to avoid the complex fabrication variation and the over intensified JFET effect. According to the structure and cell pitch of the proposed MOSFET, the $H_m$ is adjusted from 4 μm to 7 μm and the $W_m$ is increased from 1 μm to 2 μm to analyze the device's performance. Figure 13 shows the proposed MOSFET's static parameters and saturation current varying with $H_m$ and $W_m$, and the detailed simulation results are summarized in Table 4.

From Fig. 13, it can be seen that the $BV$ degrades slightly with the descending of location ($H_m$) and the widening of width ($W_m$) for the P-pillar modulation region, which is caused by partial charge imbalance behavior. That means the changing of the $BV$ is little with the variation of $H_m$ and $W_m$ for

the small modulation region. Meanwhile, it is worth noting that the $R_{on}$ keeps unchanged if the $H_m$ is over 5 μm. On the contrary, the $R_{on}$ increases sharply and the Baliga's FOM degenerates severely once the $H_m$ decreases to 4 μm. The reason is that the current flowing path will be seriously suppressed when the position of the P-pillar modulation region is too close to the P-shield region. Moreover, the $R_{on}$ gradually increases with the widening of $W_m$. The more obvious increase of $R_{on}$ and the critical degradation of Baliga's FOM are found at the $W_m$ of 2 μm.

Figure 13(b) and Table 4 exhibit that the saturation current of the proposed structure gradually decreases with the rising of location ($H_m$) and the widening of width ($W_m$) for the P-pillar modulation region. That means the distinct suppression effect can be found if the P-pillar modulation region is close to the top side, bringing a better SC reliability. However, it may cause the sacrificing of the static performance as we mentioned before. After comprehensive consideration, the $H_m = 5$ μm and the $W_m = 1.5$ μm are selected as the optimal structural parameters by comparing static characteristics and SC performance.

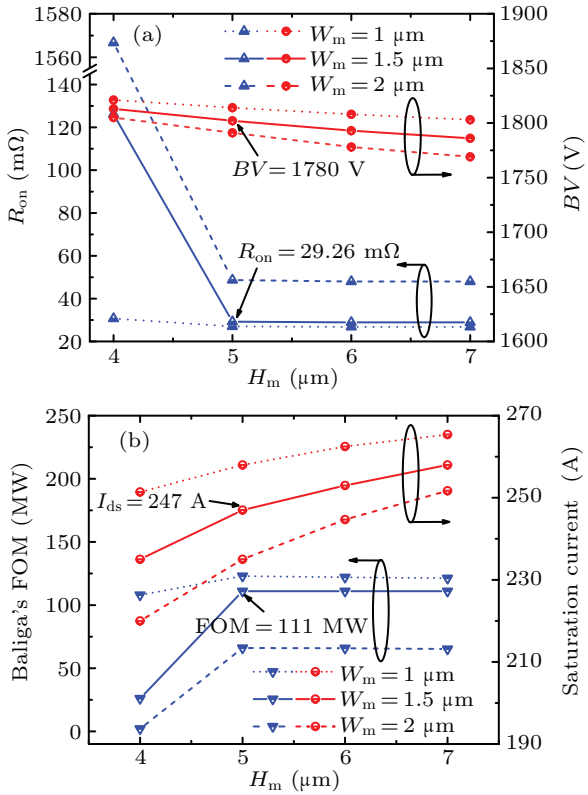



**Fig. 13.** The (a) $R_{on}$ and $BV$; (b) Baliga's FOM and saturation current ($V_{ds} = 800$ V) of the proposed structure with different $H_m$ and $W_m$ values.

**Table 4.** The simulation results of the proposed structure with varied $W_m$ and $H_m$.

| $W_m$ (μm) | $H_m$ (μm) | $BV$ (V) | $R_{on}$ (mΩ) | Baliga's FOM (MW) | Saturation current (A) ($V_{ds} = 800$ V) |
|---|---|---|---|---|---|
| 1 | 4 | 1821 | 30.7 | 108 | 251 |
| | 5 | 1814 | 27.0 | 123 | 258 |
| | 6 | 1808 | 26.8 | 122 | 263 |
| | 7 | 1803 | 26.8 | 121 | 265 |
| 1.5 | 4 | 1813 | 126.1 | 26 | 235 |
| | **5** | **1802** | **29.2** | **111** | **247** |
| | 6 | 1793 | 28.9 | 111 | 253 |
| | 7 | 1786 | 28.9 | 111 | 258 |
| 2 | 4 | 1805 | 1566.7 | 2 | 220 |
| | 5 | 1791 | 48.7 | 66 | 235 |
| | 6 | 1778 | 48.0 | 66 | 245 |
| | 7 | 1769 | 48.0 | 65 | 252 |

## 4. Conclusion

In this study, a 1200 V SiC super-junction (SJ) MOSFET with a partially widened pillar is proposed to improve the SC capability. By investigating the static characteristics and the SC performance, it is found that the Baliga's FOM ($BV^2/R_{on}$) of the proposed structure increased by 22% compared to the conventional trench structure. Meanwhile, a superior SC performance is also achieved. Compared with the conventional trench structure and SJ structure, the SC withstand time (SCWT) of the proposed structure increased by 60% and 41.2%, respectively. The enhancement of SC ability is attributed to the suppression of the saturation current at the SC transient process without sacrificing the on-state current ability. In addition, the fabrication technology is compatible with the standard epitaxy growth method with simple implant window adjustment.

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