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Enhancement of f_{MAX} of InP-based HEMTs by double-recessed offset gate process

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A double-recessed offset gate process technology for InP-based high electron mobility transistors (HEMTs) has been developed in this paper. Single-recessed and double-recessed HEMTs with different gate offsets have been fabricated and characterized. Compared with single-recessed devices, the maximum drain–source current ($I_{D,max}$) and maximum extrinsic transconductance ($g_{m,max}$) of double-recessed devices decreased due to the increase in series resistances. However, in terms of RF performance, double-recessed HEMTs achieved higher maximum oscillation frequency (f_{MAX}) by reducing drain output conductance (g_{ds}) and drain to gate capacitance (C_{gd}). In addition, further improvement of f_{MAX} was observed by adjusting the gate offset of double-recessed devices. This can be explained by suppressing the ratio of C_{gd} to source to gate capacitance (C_{gs}) by extending drain-side recess length (L_{rd}). Compared with the single-recessed HEMTs, the f_{MAX} of double-recessed offset gate HEMTs was increased by about 20%.

Keywords: InP, HEMT, maximum oscillation frequency (f_{MAX}), double-recess, offset gate

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1. Introduction

InP-based high electron mobility transistors (HEMTs) are regarded as the most promising candidates for millimeter-wave integrated circuits (MMIC) and even terahertz monolithic integrated circuits (TMIC) because of their extremely excellent high-frequency, high-gain and low-noise characteristics.[1–4] They play key roles in radio-astronomy and deep-space communication. In recent years, the requirements for higher operation frequency and larger output power of TMIC result in a strong push of THz transistor technologies with high cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}).[4–9] The f_{MAX} of InP-based HEMTs were mainly improved by scaling down the gate length.[10] Lai *et al*. reported the first InP-based HEMT with a f_{MAX} exceeding 1 THz by reducing the gate length to 50 nm.[4] Mei *et al*. demonstrated 25 nm gate length InP-based HEMTs with f_{MAX} of 1.5 THz and realized the first TMIC with 1 THz amplification.[8] However, the gate length is seriously limited by the available lithography technology. At present, it is difficult to increase f_{MAX} by continuously reducing the gate length. Another way to improve the f_{MAX} is to optimize parasitic effects. Various efforts have been made in this regard, such as reducing the source-to-drain spacing (L_{SD}),[11] gate-to-channel distance (t_{ins}),[12] as well as optimizing the gate recess,[9,13,14] and the gate stem height.[15,16]

In this paper, we will report on a novel double-recessed offset gate process for improving the f_{MAX} of InP-based HEMT instead of a gate scaling that would often be used to obtain high RF performance. A double-recess gate structure has been used previously in GaAs-based HEMTs to improve breakdown voltage, which in turn increases output power.[17] We form the double-recess gate structure by selectively etching the cap layers. Compared with the traditional double-recess gate structure, the incompletely removed cap layer can effectively reduce the exposed area of the active region and inhibit the surface effects. By controlling the gate offset, the parasitic effects can be further optimized for improved performances. Single-recessed HEMTs, and double-recessed HEMTs with different gate offsets have been fabricated and characterized. In addition, the parasitic parameters of devices are extracted and analyzed by using the small-signal model, which explains the influence of the double-recessed offset gate process.

2. Experiment

The schematic cross-section of double-recessed InP-based HEMTs is shown in Fig. 1. The epitaxial layers of the devices were grown by gas source molecular beam epitaxy (GSMBE) on 3 inch semi-insulating InP (100) substrates. From bottom to top, the layers consist of a 500 nm $In_{0.52}Al_{0.48}As$ buffer layer, a 15 nm $In_{0.53}Ga_{0.47}As$ channel layer, a 3 nm unstrained $In_{0.52}Al_{0.48}As$

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spacer layer, a Si delta doping layer with 5×10^{12} cm^{-2} doping concentration, an 8 nm unstrained $\ln_{0.52}Al_{0.48}As$ Schottky barrier layer, a 4 nm InP etch-stop layer for preventing over etching and a 15 nm/15 nm/10 nm Si-doped $\ln_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/In_{0.65}Ga_{0.35}As$ composite contact layer with a concentration of 1×10^{19} cm^{-3}/1×10^{19} cm^{-3}/3×10^{19} cm^{-3}. The 10 nm strained and heavily doped $In_{0.65}Ga_{0.35}As$ layer to reduce the actual metal-semiconductor contact resistance, a 15 nm heavily doped $In_{0.53}Ga_{0.47}As$ layer, and a 15 nm heavily doped $\ln_{0.52}Al_{0.48}As$ layer to lower the potential barrier across the Schottky barrier layer in the source and drain access regions.[18,19] Hall measurements were made at the room temperature, showing a carrier mobility of over 10000 cm^2/(V·s).

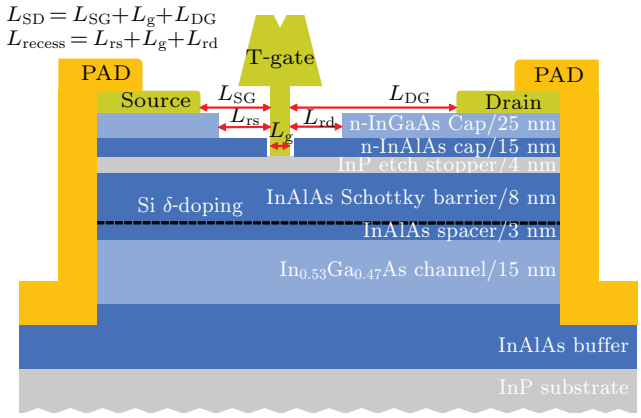


Fig. 1. Schematic cross-section of double-recessed InP-based HEMTs.

The fabrication process of double-recessed InP HEMTs mainly contains five steps, including mesa isolation, ohmic contact formation, gate recesses, T-gates and connection pads. Firstly, isolating mesa was formed by utilizing phosphorus acid-based wet chemical etching. Next, the source and drain were spaced 2.4 μm through a lithography process, followed by Ti/Pt/Au (15 nm/15 nm/50 nm) evaporated to satisfy the requirement of Ohmic contact by electron beam evaporation without annealing.

Afterward, the 0.8 μm first gate recess was defined by electronic beam lithography (EBL) with a ZEP520A e-beam resist layer, and the $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ cap layers were etched by a citric acid based solution with an etch selectivity of 20:1 to $\ln_{0.52}Al_{0.48}As$. The distance between the source and drain from the center of the first gate recess is 0.9 μm and 1.5 μm, respectively. The source-side recess length (L_{rs}) and the drain-side recess length (L_{rd}) are controlled by adjusting the position of the T-shaped gate to form symmetrical or asymmetric gate recess. T-gates were defined by EBL with a PMMA/Al/UVIII (200 nm/10 nm/800 nm) e-beam resist stack. The top UVIII was exposed by a small dose and wide line, then developed by TMAH and rinsed in DI water to determine the gate cap. And then the bottom PMMA was exposed by a big dose and narrow line, then developed by 1, 2-dimethylbenzene to define the gate foot. After that, the second gate recess was etched in the $\ln_{0.52}Al_{0.48}As$ cap layer by a phosphate based solution, and a Ti/Pt/Au (25 nm/25 nm/300 nm) metal stack was evaporated and lifted off. Three different gate positions were used to observe the dependence of RF performance on gate offset. The gate was located at the first gate recess center, with an offset to the source or drain side. The gate length of all devices is 100 nm, as shown in Fig. 2. Finally, the Ti/Au (15 nm/300 nm) connection pads were evaporated for on-wafer DC and RF characteristics measurements.

Single- and double-recessed HEMTs were identically processed, except for additional recess etching. The detailed parameters of fabricated HEMTs are shown in Table 1. All devices were deposited by plasma-enhanced chemical vapor deposition (PECVD) with 20 nm Si_3N_4 as a passivation layer.

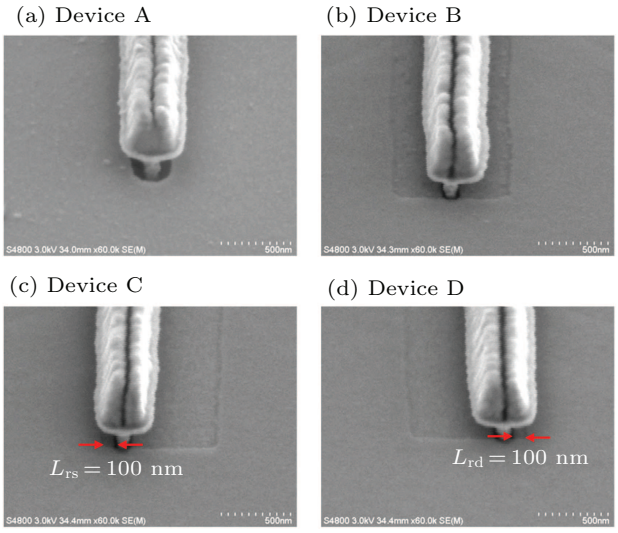


Fig. 2. SEM photograph of the T-Gate and gate recesses of the HEMTs.

Table 1. The detailed parameters of fabricated HEMTs.

Device	Recess	L_g (μm)	L_{SD} (μm)	L_{recess} (μm)	L_{rs} (μm)	L_{rd} (μm)	L_{SG} (μm)	L_{DG} (μm)
A	single	0.1	2.4	–	0.35	0.35	0.85	1.45
B	double	0.1	2.4	0.8	0.35	0.35	0.85	1.45
C	double	0.1	2.4	0.8	0.1	0.6	0.6	1.7
D	double	0.1	2.4	0.8	0.6	0.1	1.1	1.2

3. Results and discussion

3.1. Double-recessed structure

DC properties were characterized by using a HP4142 semiconductor parameter analyzer at the room temperature. Figure 3 shows the I_D–V_D output characteristics and transfer characteristics of the single-recessed HEMTs (device A) and double-recessed HEMTs (device B). Due to the higher series resistances, such as the source and drain resistance (R_s and R_d) caused by the removal of more cap layer during the formation of the first gate recess, the double-recessed HEMTs exhibit lower maximum drain–source current ($I_{D,max}$) and maximum extrinsic transconductance ($g_{m,max}$) than the single-recessed HEMTs. Extrinsic transconductance g_m is expressed by

$$g_{m,ext} = \frac{g_{m,int}}{1 + R_s \cdot g_{m,int}}, \tag{1}$$

where $g_{m,int}$ is the intrinsic transconductance of the HEMTs. It can be seen from Eq. (1) that the increase of R_s will lead to a significant decrease of $g_{m,max}$.

The RF performance is characterized via an Agilent E8363B PNA vector network analyzer from 0.1 GHz to 40 GHz. Before measurement, the devices were de-embedded by using on-wafer open and short pad structures to exclude the parasitic effect. Figure 4 shows the H_{21} and MAG/MSG versus frequency of the single-recessed HEMTs (device A) and double-recessed HEMTs (device B) at their respective $g_{m,max}$ points. Since the test frequency range was limited from 0.1 GHz to 40 GHz, the f_T and f_{MAX} were obtained by extrapolating the curve of H_{21} and MAG/MSG followed by a slope of −20 dB/dec, respectively. The f_T and the f_{MAX} of

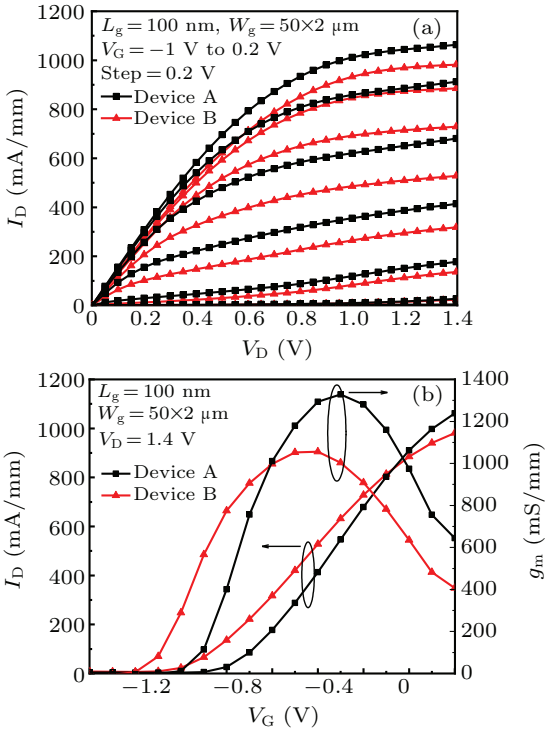


Fig. 3. DC output (a) and transfer (b) characteristics of the single- and double-recessed HEMTs.

single-recessed HEMTs are 296 GHz and 355 GHz, respectively, while the f_T and the f_{MAX} of double-recessed HEMTs are 261 GHz and 396 GHz, respectively. However, the device was still unstable ($k < 1$) at the maximum test frequency of 40 GHz, and the actual f_{MAX} will be larger than that obtained by extrapolation. The f_T and f_{MAX} are expressed by

$$f_T = \frac{g_{mi}}{2\pi} \frac{1}{(C_{gs} + C_{gd})\left[1 + g_{ds}(R_s + R_d)\right] + C_{gd} \cdot g_{mi}(R_s + R_d)}, \tag{2}$$

$$f_{MAX} = \frac{f_{T,int}}{\sqrt{4g_{ds}(R_g + R_i + R_s) + \frac{2C_{gd}}{C_{gs}}\left(\frac{C_{gd}}{C_{gs}} + g_{mi}(R_i + R_s)\right)}}, \tag{3}$$

where g_{mi} is the intrinsic transconductance, C_{gs} and C_{gd} are the parasitic capacitances from gate to source and gate to drain respectively, g_{ds} is conductance between drain and source, R_g is the parasitic resistances of gate, R_i is the intrinsic resistance in the channel region, and $f_{T,int}$ represents the cut-off frequency of the intrinsic part of HEMTs without parasitic resistance and capacitance.

To analyze the effect of the gate recess structures on RF performance, we use a small-signal model to extract the parasitic parameters of the devices. The small-signal model parameters were tuned repeatedly until very good fitting of *S*-parameters was obtained within the test frequency, as shown in Fig. 5. According to the method in Ref. [20], the relative error between the *S*-parameters of the small-signal model and the measured *S*-parameters is extracted. In the range of 5 GHz–40 GHz, the average relative error is only 2.75%.

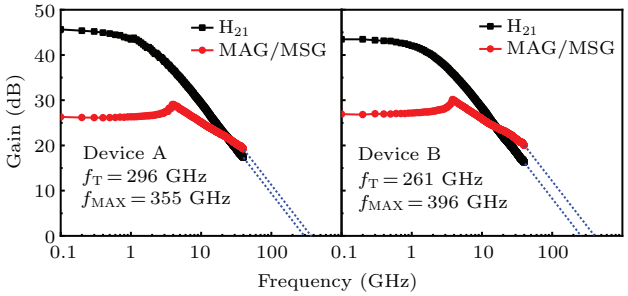


Fig. 4. The H_{21} and MAG/MSG versus frequency of the single and double recessed HEMTs.

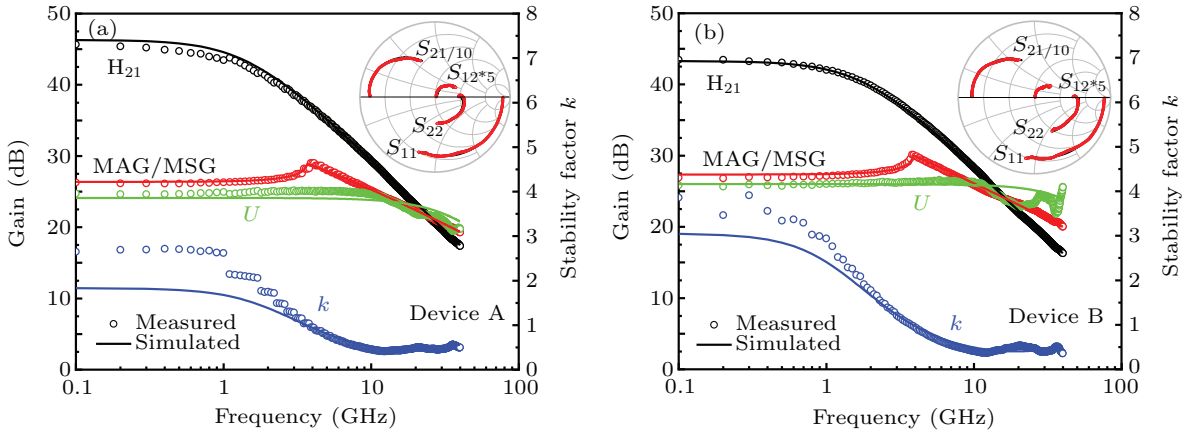


Fig. 5. Measured (symbols) and small-signal modeled (lines) RF gains (H_{21}, U, MAG/MSG) and stability factor (k) of the single and double recessed HEMTs.

Table 2. The parameters of the small-signal equivalent circuit of devices.

Device	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	g_{ds} (mS)	R_s (Ω)	R_d (Ω)	R_g (Ω)	R_i (Ω)	g_{mi} (mS)	$f_{T,model}$ (GHz)	$f_{T,meas}$ (GHz)
A	85	4.9	31.9	11	1.66	4	4.5	3.7	190	294	296
B	74.7	3.65	31.4	6.4	1.68	5.5	4.5	3.45	141	262	261

Table 2 summarizes the small-signal modeling parameters of the single and double recessed HEMTs, and also includes $f_{T,meas}$ for comparison. The measured ($f_{T,meas}$) and the modeled f_T ($f_{T,model}$) are very similar, increasing the credibility of our analysis. Equations (2) and (3) suggest that C_{gs}, C_{gd}, R_s, and R_d are the key parasitic parameters that affect f_T and f_{MAX}.[21] The heavily doped $In_{0.53}Ga_{0.47}As/In_{0.65}Ga_{0.35}As$ cap layers are partially removed in the etching process of the first gate recess, which significantly increases the series resistances (R_s and R_d), resulting in the f_T of double-recessed HEMTs being lower than that of the single-recessed HEMTs. On the other hand, double-recessed HEMTs achieve greater f_{MAX} due to the decrease in C_{gd} and g_{ds}. The decrease of g_{ds} is attributed to the effective suppression of impact ionization by the double recess structure.[22]

3.2. Gate offset in the first gate recess

The performances of double-recessed HEMTs with different gate offsets are compared. The gates of devices B, C, and D are located in the middle of the first gate recess, toward the source or toward the drain, respectively. The drain-side recess length (L_{rd}) of devices B, C, and D are 0.35 μm, 0.6 μm, 0.1 μm, respectively, while the width of the first gate recess remained 2.4 μm.

Figure 6 shows the I_D–V_D output characteristics and transfer characteristics of the devices B, C, and D. When L_{rd} increased, namely, gate position shifted from drain side to source side in the first gate recess, both $I_{D,max}$ and $g_{m,max}$ increased. Device C shows the highest $I_{D,max}$ of 1038 mA/mm and $g_{m,max}$ of 1151.6 mS/mm.

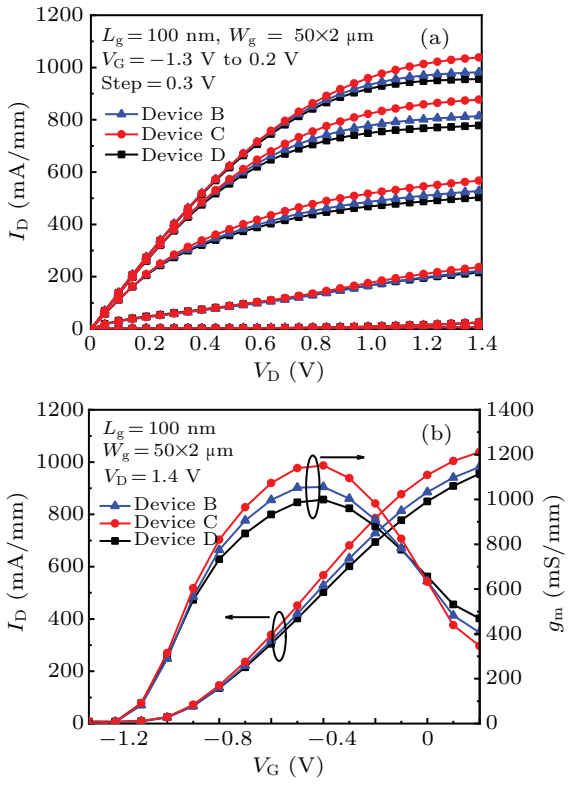


Fig. 6. DC output (a) and transfer (b) characteristics of devices B, C, and D.

Figure 7 shows the H_{21} and MAG/MSG versus frequency of devices B, C, and D at $V_G = -0.4$ V and $V_D = 1.4$ V. As the gate position shifts from drain side to source side in the first gate recess, f_T decreases from 287 GHz to 258 GHz and f_{MAX} increases from 342 GHz to 425 GHz. To explain the variation of RF performance, the parameters are extracted based on the small-signal model, as shown in Table 3.

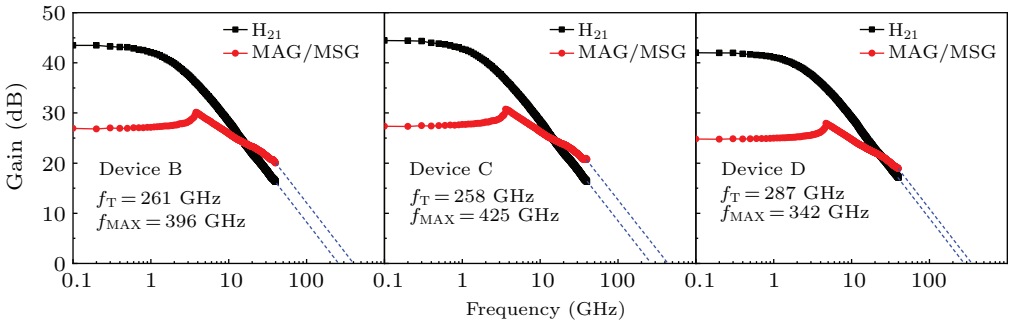


Fig. 7. The H_{21} and MAG/MSG versus frequency of devices B, C, and D.

Table 3. The parameters of the small-signal equivalent circuit of devices.

L_{rd} (μm)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_s (Ω)	R_d (Ω)	R_g (Ω)	R_i (Ω)	g_m (mS)	$f_{T,model}$ (GHz)	$f_{T,meas}$ (GHz)
0.1	62.7	4.6	28.6	1.73	5	4.5	3.45	135	286	287
0.35	74.7	3.65	31.4	1.68	5.5	4.5	3.45	141	262	261
0.6	82.1	3.45	34.2	1.58	6.5	4.5	3.45	155	260	258

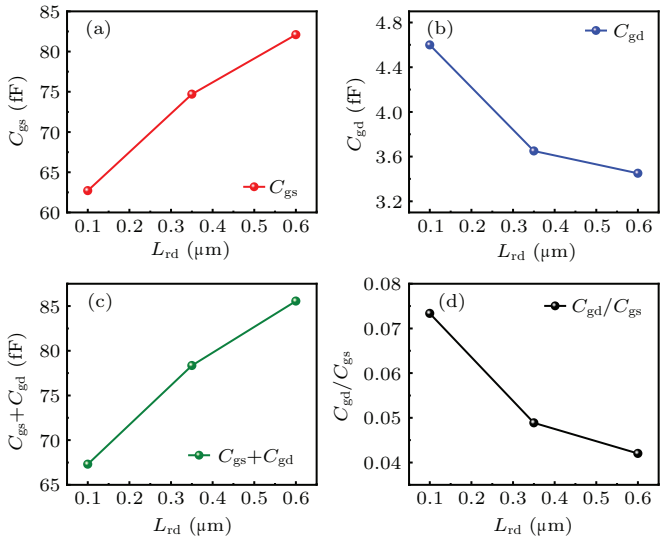


Fig. 8. Dependence of C_{gs} (a), C_{gd} (b), $C_{gs}+C_{gd}$ (c) and C_{gd}/C_{gs} (d) on L_{rd} for double-recessed HEMTs.

Figure 8 shows some key parasitic parameters as the functions of L_{rd}. The parameters C_{gs} and C_{gd} were extracted by Eqs. (4) and (5). The C_{gs} increased and C_{gd} decreased by extending L_{rd} from 0.1 μm to 0.6 μm, as shown in Fig. 8. Although the changes of C_{gs} and C_{gd} with the extension of L_{rd} are not the same, the increase of $C_{gs}+C_{gd}$ well explains the observed decrease of f_T. On the other hand, since the opposite changes of C_{gs} and C_{gd} lead to the further reduction of C_{gd}/C_{gs}, the device C with the gate offset to the source side exhibits a maximum f_{MAX} of 425 GHz. Compared with the single-recessed HEMTs (device A) with f_{MAX} of 355 GHz, the increase of f_{MAX} is about 20%.

$$C_{gs} = \frac{(1+d^2)}{\omega}\left(\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})\right), \tag{4}$$

$$C_{gd} = -\frac{\mathrm{i}(Y_{12})}{\omega}, \tag{5}$$

Table 4 summarizes the reported performance of InP HEMT devices with a gate length of about 100 nm. Our device exhibits outstanding f_{MAX} in devices with gate length over 100 nm by using double-recessed offset gate process technology. The device performances can be further improved by reducing the gate length or using InAs-rich channel materials in the future.

Table 4. Compared with the published InP HEMT with a gate length of about 100 nm.

Ref.	L_g (nm)	Channel	$G_{m,max}$ (mS/mm)	f_T (GHz)	f_{MAX} (GHz)
[23]	100	$In_{0.68}Ga_{0.32}As$	700	183	230
[24]	100	$In_{0.53}Ga_{0.47}As$	724	249	415
[25]	120	$In_{0.53}Ga_{0.47}As$	1100	166	340
[12]	87	$In_{0.8}Ga_{0.2}As$	3000	559	671
[26]	75	InAs	1331	260	800
This work	100	$In_{0.53}Ga_{0.47}As$	1152	258	425

4. Conclusion

In summary we demonstrated a novel double-recessed offset gate process for InP HEMTs. The double-recessed HEMTs can effectively improve f_{MAX} by reducing g_{ds} and C_{gs}. With the gate offset from the drain side to the source side, f_{MAX} can be further improved by suppressing C_{gd}/C_{gs}. Finally, the f_{MAX} of double double-recessed offset gate HEMTs is 20% higher than that of single-recessed HEMTs.

Acknowledgements

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