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An electromagnetic simulation assisted small signal modeling method for InP double-heterojunction bipolar transistors

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We present a convenient and practical electromagnetic (EM) assisted small-signal model extraction method for InP double-heterojunction bipolar transistors (DHBTs). Parasitic parameters of pad and electrode fingers are extracted by means of 3D EM simulation. The simulations with a new excitation scheme are closer to the actual on-wafer measurement conditions. Appropriate simulation settings are calibrated by comparing measurement and simulation of OPEN and SHORT structures. A simpler π-type topology is proposed for the intrinsic model, in which the base-collector resistance R_μ, output resistance R_{ce} are deleted, and a capacitance C_{ce} is introduced to characterize the capacitive parasitic caused by the collector finger and emitter ground bar. The intrinsic parameters are all extracted by exact equations that are derived from rigorous mathematics. The method is characterized by its ease of implementation and the explicit physical meaning of extraction procedure. Experimental validations are performed at four biases for three InGaAs/InP HBT devices with 0.8×7 μm, 0.8×10 μm and 0.8×15 μm emitter, and quite good fitting results are obtained in the range of 0.1–50 GHz.

Keywords: electromagnetic simulation, InP double-heterojunction bipolar transistor, parameter extraction, small-signal modeling

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1. Introduction

Indium-phosphide-based heterojunction bipolar transistors (InP HBTs) have been exploited and investigated for integrated circuits operating during the last decades, with their high power and high-speed characteristics, it is widely used in many technology fields such as optical communications and telephone systems.[1] Compared to silicon-based technologies, InP HBTs have higher electron mobility, better noise performance, and anti-radiation characteristics.[2–4] InP HBTs also have higher thermal conductivity and higher electron mobility than GaAs-based devices, so InP is the most suitable semiconductor material for terahertz applications.[5]

For most high-frequency electronic circuits, transistors are the core active components, they should be characterized and modeled before moving to the circuit design, so transistor modeling plays a fundamental role in its utility. De-embedding is the crucial step in device modeling, it can be conceptually understood as shifting the electrical reference planes closer to the actual DUT,[6] and intrinsic parameters can be extracted accurately only when extrinsic parts (such as probe pads and interconnects) are subtracted from the raw measurement data. De-embedding methods have been developing and improving in recent years, the most widely used open-short method[7] is based on lumped approximation, which is generally applicable within 30 GHz. The four step method[8] addresses issues of substrate coupling and contact effects. An improved three step method[9] was proposed and the method is applied not only to *S*-parameter measurements but also to large-signal measurements for the first time. The well-known 4-port method[1] treats the parasitic network as a 4-port network, which does not require any equivalent approximation and is compatible with noise de-embedding. The pad-thru-short[3] method accurately removes parasitic parts of the nonshielding input and output interconnects and dangling leg.

As the application frequency of circuit design has reached the terahertz domain and the size of transistor is small enough, the values of extrinsic elements become comparable to values of intrinsic parameters, making it more challenging to de-embed and accurately characterize devices up to the submillimeter wave range. Normally, this is achieved by measurement methods like open-collector (to extract extrinsic resistances and inductances) and cut-off (to extract extrinsic capacitances), these traditional techniques have obvious disadvantages. Open-collector measurement requires a very high base current, which may damage the device and obtain inappropriate data. In addition, the resistances obtained are the mixture of the outer and inner parts. In cut-off measurement, it is difficult to separate the extrinsic capacitance and intrinsic capacitance. Electromagnetic (EM) simulation-based de-embedding is an alternative approach that can solve these problems. Electrical characteristics can be directly obtained from EM simulations if the port and simulation setups are defined properly, the

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process does not need any standards, and many measurements and errors from measurements can be avoided. Up to now, the method has been applied in the small-signal model building for kinds of transistors such as complementary metal-oxide-semiconductor field-effect transistors,[11,12] GaAs p-type high electron mobility transistors (HEMTs),[13] GaN HEMTs,[14] and InP HBTs.[15–18] Furthermore, the EM simulation approach can also be used in the noise model building for microwave transistors. In Ref. [19], a low-noise transistor model has been developed based on EM simulations.

This paper presents a systematical EM simulation-based method to extract small-signal model for InP DHBTs with three steps. In the first step, the ports for simulations and setups are properly defined. An extended L-2L port calibration[2] is used to eliminate the port discontinuity, and the suitable simulation setups is determined by fitting the simulation results and measurements data of OPEN and SHORT structures, this step is illustrated in Section 2. In the second step, the parasitic elements of the device are de-embedded, seven 3D dummy structures are applied to extract parasitic parameters of probe pads, interconnection lines, and electrode fingers, all the dummy structures are simulated in EM simulation software and the simulation results are analyzed in Agilent advanced design system (ADS), this step is illustrated in Section 3. The last step is to extract intrinsic parameters, an intrinsic small-signal model simpler than conventional model[21,22] is proposed, the base-collector resistance R_μ and the output resistance R_{ce} are deleted for their relatively high value, C_{ce} is introduced to characterize the capacitance generated from the collector finger and emitter ground bar, this step is illustrated in Section 4. In Section 5, experimental validations for the three transistors with different emitter sizes are performed at four bias points.

2. EM simulation setups and port calibration

The core procedure of this work is electromagnetic field simulation, simulation accuracy directly evolves with the success of the final modeling result, so the simulation settings should be the primary concern and ought to be set up properly to ensure the correctness of the simulation. There are three key aspects to note: Firstly, a radiation boundary should be applied to the airbox of the simulation structures because radiation boundary creates an approximation of free space that allows electromagnetic waves to radiate infinitely far into space. Secondly, lumped ports ought to be applied internally in the solution space. Analogous to a probe of a testing system, the lumped port inputs current signals into the structure, so we must set its port impedance to 50 Ω in order to make it consistent with the internal characteristic impedance of the test system. Thirdly, the lumped port must be calibrated. The excitation scheme in this work mainly refers to the surrounding ground ring approach reported in Ref. [2], the vertical 2D rectangle lumped port touches the simulation structure and the opposite side edge touches the vertical perfect electric conductor bridge, a perfect electric conductor (PEC) is an idealized material exhibiting infinite electrical conductivity or zero resistivity. Hence the parasitism of this excitation mainly comes from PEC bridges and the lumped ports. A lumped port generates S, Y, Z parameters and fields in EM simulations, therefore its parasitic elements should be de-embedded. We use the extended L-2L method to calculate the parasitic inductance from the PEC bridge and the parasitic capacitance from the port. After port calibration, the two extracted parasitic values are estimated to be a 14 pH inductance and a 4.5 fF capacitance, which are almost independent of frequency as shown in Fig. 1, indicating that the calibration technique is reliable. The two parasitic parameters will be subtracted from all the subsequent EM simulation data. All the conditions of simulation structures should be set as close as possible to the actual on-wafer measure conditions. The structure simulated consists of three layers. The top metal is set as gold material with conductivity 3.8×10^7 S/m and a thickness of 0.5 μm. The layer below is BCB, its relative permittivity is set as 2.6, and thickness is set as 7 μm. The two materials above are laid on the InP substrate with a thickness of 600 μm and relative permittivity of 10.6.

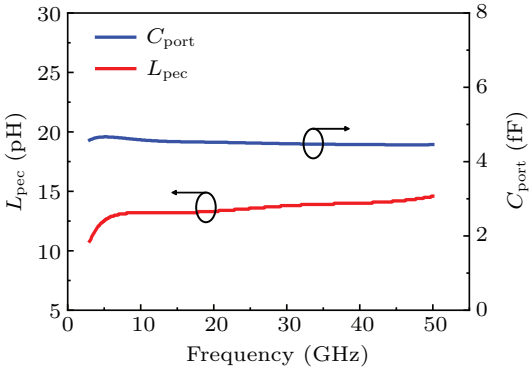


Fig. 1. The extracted parasitic inductance of PEC bridge and parasitic capacitance of lumped port, estimated to be 1.4 pH and 4.5 fF, respectively.

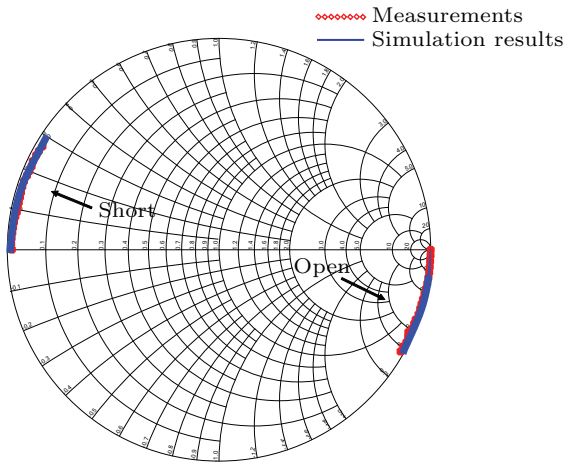


Fig. 2. Comparisons of $S(1,1)$ between measurements and simulation results of OPEN and SHORT structures. Good agreements are obtained.

Experimental data within 0.1–50 GHz of conventional SHORT and OPEN structures are used as references for checking the correctness of the excitation scheme and simulation settings. Figure 2 shows that EM simulation results of OPEN and SHORT structures fit well with their measurement data, which explains that the simulation settings are reasonable. The determined setups from this procedure will be applied to the subsequent EM simulations.

3. EM simulation assisted extraction of parasitic parameters

The complete small-signal equivalent circuit of InP DHBTs is shown in Fig. 3. Before we start establishing the small-signal model of the intrinsic part, all the parasitic out of the intrinsic part should be de-embedded. The outermost parasitic capacitances (C_{pbg}, C_{pcg}, C_{pbcg}), resistances (R_{bx}, R_{cx}, R_{ex}) and inductances (L_{bx}, L_{cx}, L_{ex}) are from probe pads, and the similar RCL network of the inner part (C_{pbg}, C_{pcg}, C_{pbcg}, R_{bx}, R_{cx}, R_{ex}, L_{bx}, L_{cx}, L_{ex}) are the parasitic elements of the electrode fingers.

$$Y_{outer-cap} = Y_{open-pad}. \tag{1}$$

The Z parameter of the outer pad RL network is obtained by subtracting the Y parameter of the open-pad structure from the short-pad structure shown in Fig. 5(b) and calculating its inverse matrix.

$$Z_{outer-RL} = [Y_{short-pad} - Y_{open-pad}]^{-1}. \tag{2}$$

The Y parameter of the device electrode fingers can be calculated from the full-open structure shown in Fig. 5(c). The parasitic inductances and capacitances are subtracted from the full-open structure.

$$Y_{inner-cap} = \{[Y_{full-open} - Y_{open-pad}]^{-1} - Z_{outer-RL}\}^{-1}. \tag{3}$$

The Z parameter of the inner electrodes RL network is calculated by subtracting pad parasitic elements and electrode parasitic capacitances from the full-short structure shown in Fig. 4(d).

$$Z_{inner-RL} = \{\{[Y_{full-short} - Y_{open-pad}]^{-1} - Z_{outer-RL}\}^{-1} - Y_{inner-cap}\}^{-1}. \tag{4}$$

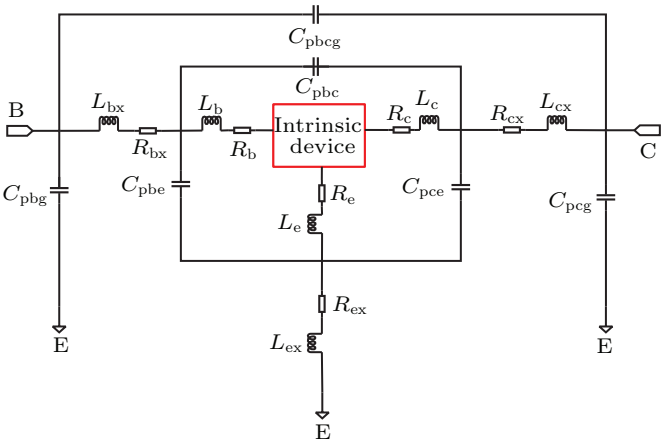


Fig. 3. The complete small-signal equivalent circuit model of the InP HBT.



Fig. 4. View of the InP HBT structure in Ansys HFSS. All sizes and layouts are strictly drawn in accordance with the actual device.

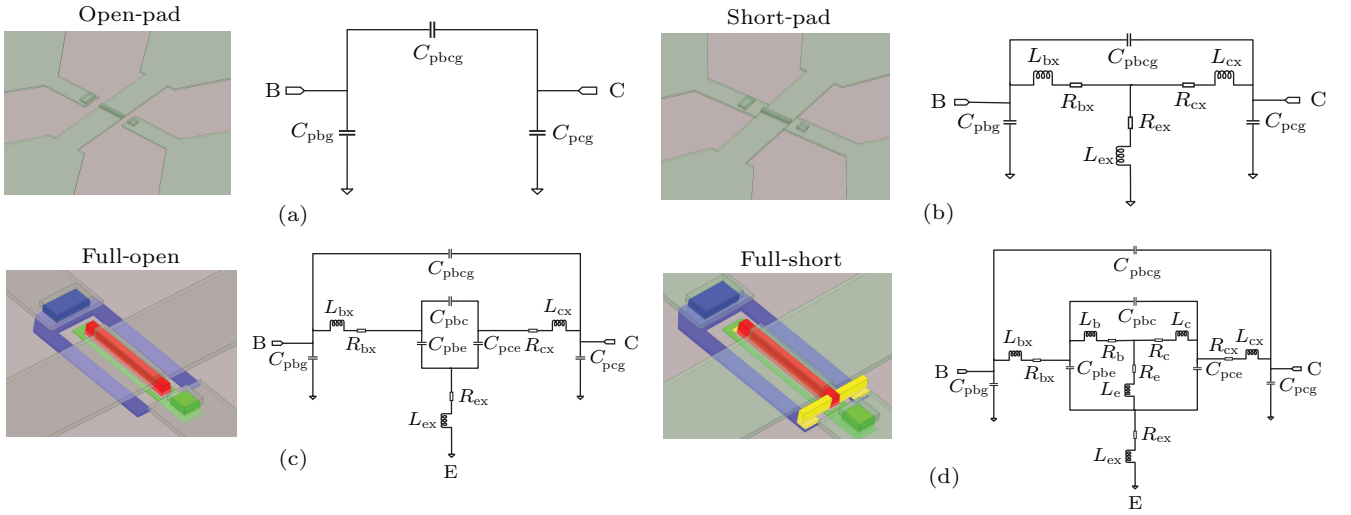


Fig. 5. Four of the seven dummy structures for finding out the matrix of intrinsic device. (a) Open-pad structure. (b) Short-pad structure. (c) Full-open structure. All the electrodes are in open state. (d) Full-short structure. The open end of the base electrode and collector electrode are connected to the emitter electrode.

Then we can obtain the Z parameters of the intrinsic device with Eq. (5), where $Y_{\rm raw}$ is the unprocessed measured data, and $Z_{\rm deem}$ is the impedance parameter to extract intrinsic parameters in Section 4.

$$Z_{\rm deem} = \{\{[Y_{\rm raw} - Y_{\rm open-pad}]^{-1} - Z_{\rm outer-RL}\}^{-1} - Y_{\rm inner-cap}\}^{-1} Z_{\rm inner-RL}. \tag{5}$$

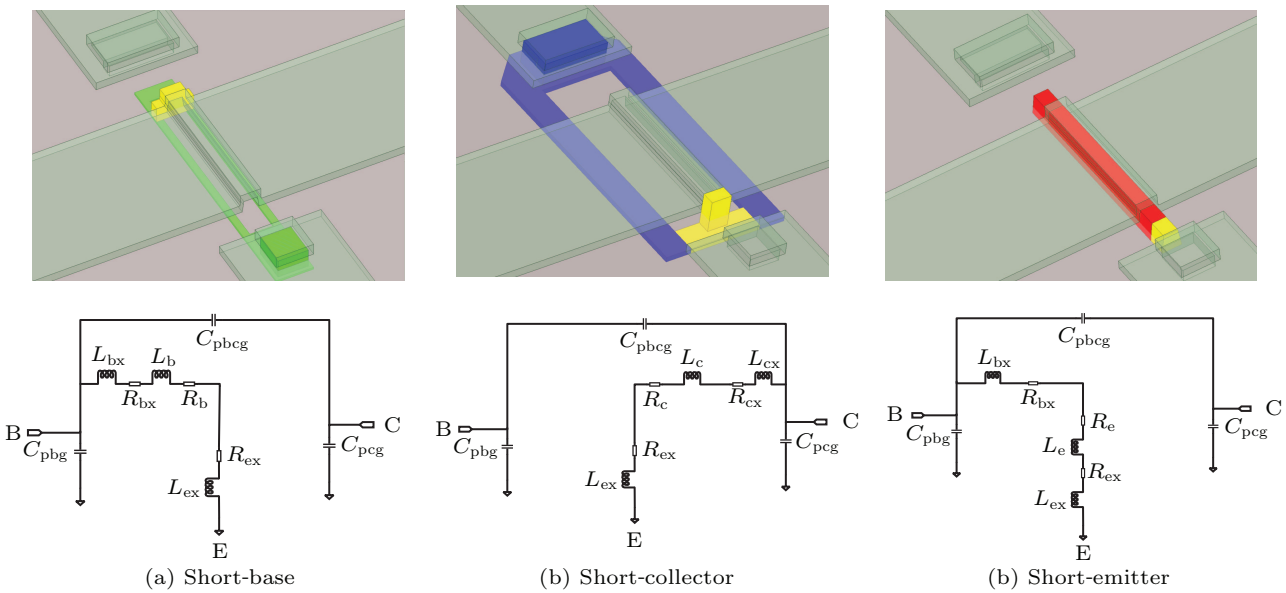
$$Z_{\rm inner-RL} = \begin{bmatrix} {\rm j}w(L_{\rm b}+L_{\rm e}-2M_{\rm be})+R_{\rm b}+R_{\rm e} & {\rm j}w(L_{\rm b}+M_{\rm bc}-M_{\rm ec}-M_{\rm be})+R_{\rm ef} \\ {\rm j}w(L_{\rm b}+M_{\rm bc}-M_{\rm ec}-M_{\rm be})+R_{\rm ef} & {\rm j}w(L_{\rm c}+L_{\rm e}-2M_{\rm ec})+R_{\rm bf}+R_{\rm ef} \end{bmatrix}. \tag{6}$$

To extract the three mutual inductances, values of $L_{\rm b}$, $L_{\rm c}$ and $L_{\rm e}$ must be solved. The Y parameter of parallel RL network in the three structures (circled with red line in Fig. 6) can be written as

$$Y_{\rm sb} = Y_{\rm short-Base} - Y_{\rm open-pad} = \begin{bmatrix} 1/({\rm j}wL_{\rm b}+{\rm j}wL_{\rm bx}+{\rm j}wL_{\rm ex}+R_{\rm b}+R_{\rm ex}+R_{\rm bx}) & 0 \\ 0 & 0 \end{bmatrix}, \tag{7}$$

$$Y_{\rm sc} = Y_{\rm short-Collector} - Y_{\rm open-pad} = \begin{bmatrix} 1/({\rm j}wL_{\rm c}+{\rm j}wL_{\rm cx}+{\rm j}wL_{\rm ex}+R_{\rm c}+R_{\rm ex}+R_{\rm cx}) & 0 \\ 0 & 0 \end{bmatrix}, \tag{8}$$

$$Y_{\rm se} = Y_{\rm short-Emitter} - Y_{\rm open-pad} = \begin{bmatrix} 1/({\rm j}wL_{\rm e}+{\rm j}wL_{\rm bx}+{\rm j}wL_{\rm ex}+R_{\rm e}+R_{\rm ex}+R_{\rm bx}) & 0 \\ 0 & 0 \end{bmatrix}. \tag{9}$$



(a) Short-base (b) Short-collector (b) Short-emitter

Fig. 6. (a) Short-base (B) structure. The collector and emitter electrodes are removed and the base electrode is shorted to the ground. (b) Short-collector (C) structure. The emitter and base electrodes are removed and the collector electrode is shorted to the ground. (c) Short-emitter (E) structure. The collector and base electrodes are removed and the emitter electrode is shorted to the base pad.

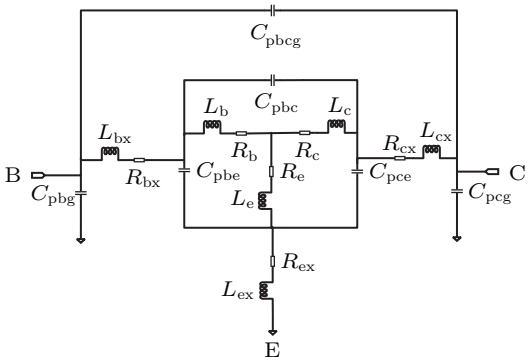


Fig. 7. Equivalent circuit of full short after considering electrode mutual inductance. $M_{\rm bc}$, $M_{\rm be}$ and $M_{\rm ce}$ are the three mutual inductances among three electrodes.

As for the rest three structures in Fig. 6, i.e., short-base, short collector and short emitter, they are introduced for considering the influence of mutual inductance between the electrode fingers. As shown in Fig. 7, after taking the influence of mutual inductance into account, there exist mutual inductances $M_{\rm bc}$, $M_{\rm be}$ and $M_{\rm ce}$ among $L_{\rm b}$, $L_{\rm c}$ and $L_{\rm e}$. The Z parameters of the RL network circled with read dotted line in the full-short structure in Fig. 7 should be

$L_{\rm b}$, $L_{\rm c}$ and $L_{\rm e}$ that can be calculated with the following equations:

$$L_{\rm b} = {\rm imag}\left(\frac{1}{Y_{sb11}} - L_{\rm bx} - L_{\rm ex}\right), \tag{10}$$

$$L_{\rm c} = {\rm imag}\left(\frac{1}{Y_{sc11}} - L_{\rm cx} - L_{\rm ex}\right), \tag{11}$$

$$L_{\rm e} = {\rm imag}\left(\frac{1}{Y_{se11}} - L_{\rm bx} - L_{\rm ex}\right). \tag{12}$$

Now that values of $L_{\rm b}$, $L_{\rm c}$ and $L_{\rm e}$ have already been solved, we can extract $M_{\rm bc}$, $M_{\rm be}$ and $M_{\rm ce}$ easily. Figure 8 gives the extraction results (0.8×10 μm transistor). The electrode inductances with consideration of mutual inductance $L_{\rm bm}$, $L_{\rm cm}$,

L_{em} can be calculated by

$$L_{bm} = L_b - M_{bc} - M_{be} + M_{ce}, \tag{13}$$

$$L_{cm} = L_b - M_{bc} - M_{ce} + M_{be}, \tag{14}$$

$$L_{em} = L_e - M_{ce} - M_{be} + M_{bc}. \tag{15}$$

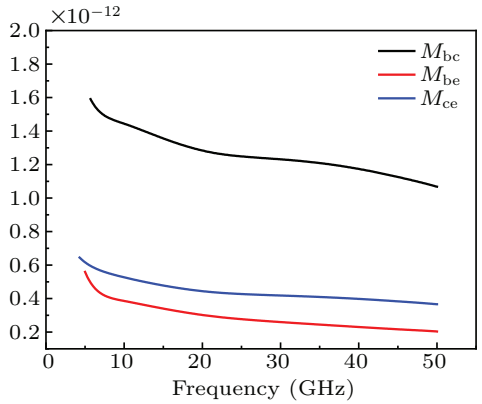


Fig. 8. Extraction results of electrode mutual inductance M_{bc}, M_{be} and M_{ce} (0.8×10 μm transistor).

All the extracted extrinsic parameters are listed in Table 1, and emitter electrode resistance and inductance versus emitter length are shown in Fig. 9, the inductance and resistance of the electrode increase as the length of the electrode increases, which proves the physical soundness and consistency of this de-embedding method.

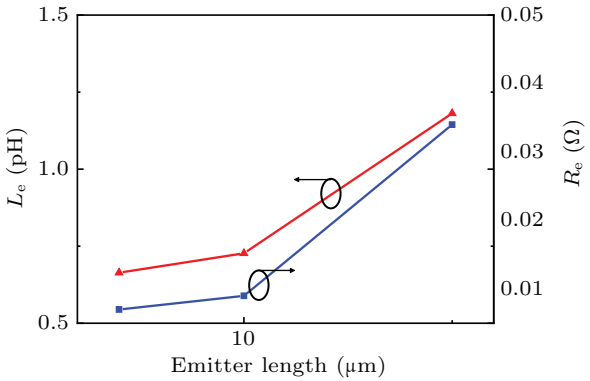


Fig. 9. Emitter resistance and inductance versus emitter length.

Table 1. Extraction results of parasitic parameters.

Elements	0.8×7 μm	0.8×10 μm	0.8×15 μm	Elements	0.8×7 μm	0.8×10 μm	0.8×15 μm
C_{pbcg} (fF)	1.868	1.814	2.208	C_{pbc} (fF)	1.972	2.108	2.030
C_{pbg} (fF)	14.55	14.60	20.65	C_{pbe} (fF)	8.347	9.739	9.975
C_{pcg} (fF)	14.49	14.53	20.61	C_{pce} (fF)	9.224	10.264	10.531
L_{bx} (pH)	41.55	40.50	40.86	L_{bm} (pH)	2.289	2.749	4.339
L_{cx} (pH)	39.75	40.19	40.34	L_{cm} (pH)	1.363	1.619	2.581
L_{ex} (pH)	8.726	8.178	7.543	L_{em} (pH)	0.664	0.727	1.181
R_{bx} (Ω)	0.461	0.464	0.472	R_b (Ω)	2.003	2.669	3.777
R_{cx} (Ω)	0.449	0.459	0.468	R_c (Ω)	0.306	0.500	0.607
R_{ex} (Ω)	0.160	0.130	0.103	R_e (Ω)	0.007	0.009	0.034

4. Extraction of intrinsic parameters

The intrinsic equivalent circuit we proposed is shown in Fig. 10. R_{bi} is the intrinsic base resistances, R_π is the intrinsic base-emitter resistance. C_μ and C_π are the intrinsic base-collector and base-emitter capacitance, respectively, and C_{cx} is the extrinsic base-collector capacitance. G_{m0} is the DC transconductance and G_m is the small signal transconductance, τ is delay time.

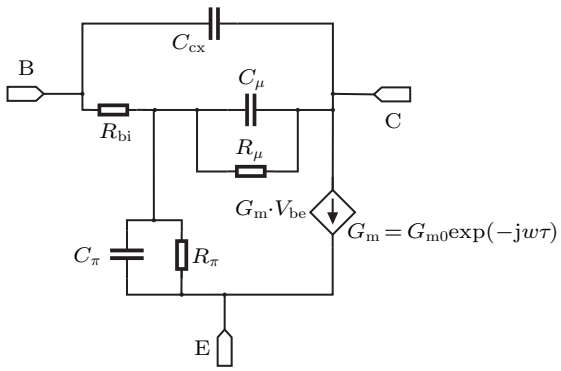


Fig. 10. Proposed intrinsic equivalent circuit.

Considering the simplicity of the model, we omitted base-collector resistance R_μ and the output resistance R_{ce}, because these two parameters have relatively high values. Capacitance C_{ce} is introduced for the characterization of the capacitive parasitic caused by the collector electrode finger and the emitter ground bar, as shown in Fig. 12.

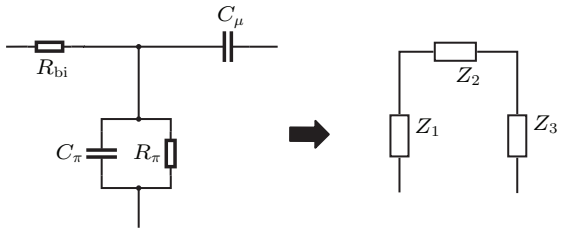


Fig. 11. The T–π transformation.

First, we use the T–π transformation[23,24] displayed in Fig. 11 for this equivalent circuit. The three impedance parameters in Fig. 11 are

$$Z_1 = \frac{X}{Z_\mu}, \tag{16}$$

$$Z_2 = \frac{X}{Z_\pi}, \tag{17}$$

$$Z_3 = \frac{X}{Z_{\rm bi}}, \tag{18}$$

where

$$Z_\mu = \frac{1}{{\rm j}wC_\mu}, \tag{19}$$

$$Z_\pi = \frac{R_\pi}{1} + {\rm j}wC_\pi, \tag{20}$$

$$Z_{\rm bi} = R_{\rm bi}, \tag{21}$$

$$X = Z_\mu \cdot Z_\pi + Z_\mu \cdot Z_{\rm bi} + Z_\pi \cdot Z_{\rm bi}. \tag{22}$$

The Y parameters of the intrinsic part can be expressed as

$$Y_{\rm deem} = \begin{bmatrix} \frac{1}{Z_1} + \frac{1}{Z_2} + {\rm j}wC_{\rm cx} & -\frac{1}{Z_2} - {\rm j}wC_{\rm cx} \\ \frac{X \cdot G_{\rm m}}{Z_1 \cdot Z_2} - \frac{1}{Z2} - {\rm j}wC_{\rm cx} & \frac{X}{Z_2 \cdot Z_3} \cdot G_{\rm m} + \frac{1}{Z_2} + \frac{1}{Z_3} + {\rm j}w(C_{\rm cx} + C_{\rm ce}) \end{bmatrix}, \tag{23}$$

where

$$G_{\rm m} = G_{\rm m0} \cdot {\rm e}^{-{\rm j}w\tau}. \tag{24}$$

From the Y parameters above, we have

$$R_\pi = {\rm real}(Y_{{\rm deem}_{11}} + Y_{{\rm deem}_{12}})^{-1}, \tag{25}$$

$$C_\pi = {\rm imag}\left(\frac{Y_{{\rm deem}_{11}} + Y_{{\rm deem}_{12}}}{w}\right), \tag{26}$$

$$G_{\rm m0} = {\rm mag}\left(\frac{Y_{{\rm deem}_{21}} - Y_{{\rm deem}_{12}}}{Y_{{\rm deem}_{11}} + Y_{{\rm deem}_{12}}} \cdot \frac{1 + {\rm j}w \cdot C_{\rm be}}{Rbe}\right), \tag{27}$$

$$R_{\rm bi} = {\rm real}\left(\frac{1 + {\rm j}wC_\pi}{Y_{11} + Y_{12}}\right) - R_\pi, \tag{28}$$

$$C_{\rm bc} = \frac{\frac{{\rm imag}\left(\frac{1 + {\rm j}wC_\pi}{Y_{11} + Y_{12}}\right)}{w \cdot R_{\rm bi}} - C_\pi}{R_\pi}, \tag{29}$$

$$C_{\rm cx} = -\frac{{\rm imag}(Y_{{\rm deem}_{12}} + \frac{1}{Z_2})}{w}, \tag{30}$$

$$C_{\rm ce} = \frac{{\rm imag}(Y_{{\rm deem}_{22}} - \frac{X}{Z_2 Z_3} G_{\rm m} - \frac{1}{Z_2} - \frac{1}{Z_3})}{w} - C_{\rm c_x}. \tag{31}$$

Parameter τ is obtained by fitting the measured S parameters. Table 2 shows the intrinsic parameter extraction results of bias at $V_{\rm ce} = 1.2$ V, $I_{\rm b} = 60$ μA, $V_{\rm ce} = 1.7$ V, $I_{\rm b} = 40$ μA, $V_{\rm ce} = 2.2$ V, $I_{\rm b} = 140$ μA, $V_{\rm ce} = 2.7$ V, $I_{\rm b} = 160$ μA. By this step, all the parameters in the small signal model of the three transistors are extracted.

Table 2. Extraction results of intrinsic parameters.

	$V_{\rm c} = 1.2$ V, $I_{\rm b} = 60$ μA			$V_{\rm c} = 1.7$ V, $I_{\rm b} = 40$ μA		
Elements	0.8×7 μm	0.8×10 μm	0.8×15 μm	0.8×7 μm	0.8×10 μm	0.8×15 μm
$C_{\rm cx}$ (fF)	7.258	8.477	9.205	6.549	11.32	5.299
C_μ (fF)	4.417	4.862	12.32	8.363	5.15	15.05
C_π (fF)	65.85	60.99	85.95	64.44	46.74	89.31
$C_{\rm ce}$ (fF)	26.93	23.25	24.01	23.25	17.22	24.54
R_π (Ω)	950	1003	1163	1300	1360	1127
$R_{\rm bi}$ (Ω)	14.29	13.62	7.860	15.15	16.74	6.908
$G_{\rm m0}$ (S)	0.051	0.043	0.030	0.033	0.027	0.030
τ (ps)	0.949	0.918	1.161	1.163	1.02	1.260
	$V_{\rm c} = 2.2$ V, $I_{\rm b} = 140$ μA			$V_{\rm c} = 2.2$ V, $I_{\rm b} = 160$ μA		
Elements	0.8×7 μm	0.8×10 μm	0.8×15 μm	0.8×7 μm	0.8×10 μm	0.8×15 μm
$C_{\rm cx}$ (fF)	8.679	11.22	10.32	5.996	12.89	9.353
C_μ (fF)	6.330	2.507	8.80	7.272	4.554	9.189
C_π (fF)	122.5	117.5	170.25	92.70	133.3	195.69
$C_{\rm ce}$ (fF)	21.37	26.94	17.38	23.25	26.35	15.04
R_π (Ω)	545	508.9	452.2	500	421.38	342.06
$R_{\rm bi}$ (Ω)	13.69	14.73	6.01	12.63	15.06	5.113
$G_{\rm m0}$ (S)	0.112	0.096	0.108	0.120	0.124	0.139
τ (ps)	1.418	1.001	1.314	1.02	1.205	1.50

5. Verification and discussion

In order to verify the correctness of the proposed small-signal model building method, InGaAs/InP DHBT devices with the emitter sizes 0.8×7 μm, 0.8×10 μm and 0.8×15 μm are used here for validation. The devices are manufactured in the Microwave Integrated Circuit Research Laboratory of the IMECAS. Measurements were performed at Agilent E8363B vector network analyzer (0.1–50 GHz) after an on-wafer short-open-load-through (SOLT) calibration.[25] Cascade probe sta-

tion is used.

$$\mathrm{Err} = \frac{1}{4N}\sum_{i,j=1}^{2}\sum_{f=1}^{N}\frac{|S_{ij}^{\mathrm{meas}}(f) - S_{ij}^{\mathrm{sim}}(f)|}{\max(|S_{ij}^{\mathrm{meas}}(f)|)}. \tag{32}$$

Figure 13 shows comparisons between measured and simulated S parameters at four different bias, quite good agreements are obtained, frequency is varied from 0.1 GHz to 50 GHz. The S parameters shown in Fig. 12 have been multiplied by some coefficients to make fitting results more clearly presented. It is worth noting that the kink phenomenon of S_{22} in smith chart is observed, an abrupt change in the behavior of S_{22} occurs at a certain frequency. It has been reported in HEMTs [26,27] and HBTs[28,29] that such an effect is caused by the shifty output impedance at different frequencies, transistors show a series RC circuit at low frequencies and a parallel RC circuit at high frequencies. In addition, the kink phenomenon is much easier to see in bipolar transistors, especially in heterojunction bipolar transistors rather than field effect transistors because it was found that the kink effect is enhanced as the transconductance increases. Residual error of 0.8×10 μm transistor at the four bias points are given in Table 3 according to the error function (28), where N is the total number of frequency points taken in the range of 0.1–50 GHz, here its value is 500, $S_{ij}^{\mathrm{meas}}(f)$ is the measured S parameter at frequency point f, and $S_{ij}^{\mathrm{sim}}(f)$ is the simulated S parameter of the small signal model.

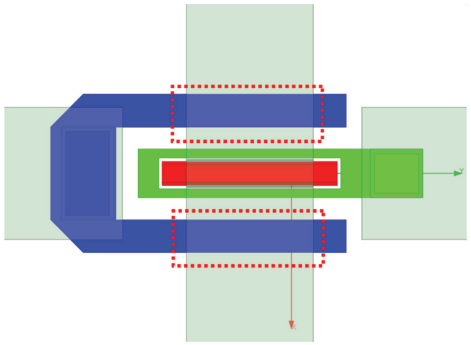


Fig. 12. Introduced capacitance C_{ce} (circled with red dotted square).

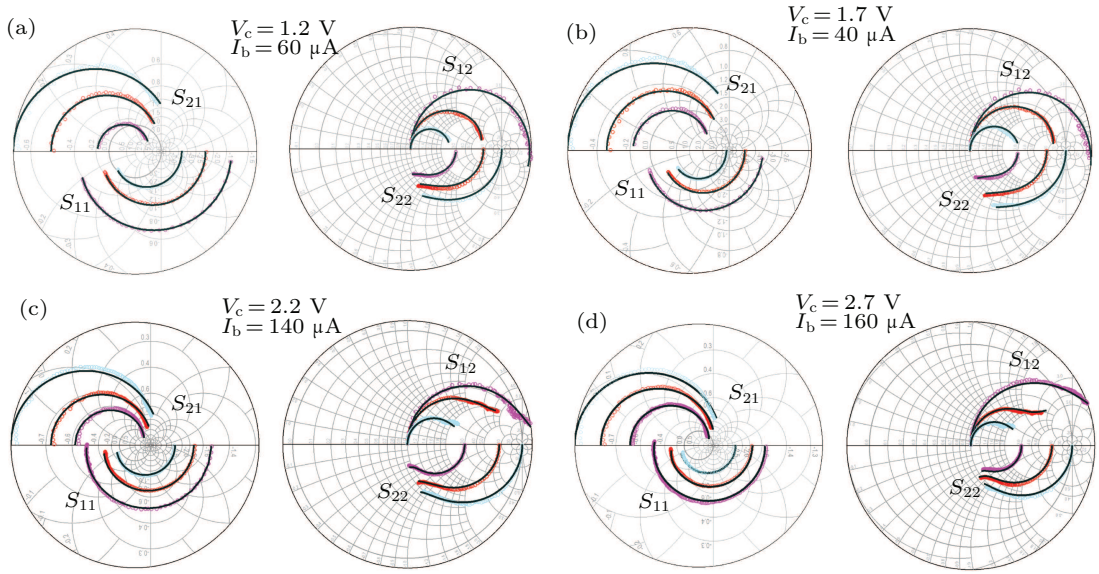


Fig. 13. Comparison of S parameter between measurements (circles) and simulation results (solid lines) for 0.8×7 μm (blue), 0.8×10 μm (red), 0.8×15 μm (pink) InP DHBTs from 0.1 GHz to 50 GHz. (a) Bias at $V_{\mathrm{ce}} = 1.2$ V, $I_{\mathrm{b}} = 60$ μA. (b) Bias at $V_{\mathrm{ce}} = 1.7$ V, $I_{\mathrm{b}} = 40$ μA. (c) Bias at $V_{\mathrm{ce}} = 2.2$ V, $I_{\mathrm{b}} = 140$ μA. (d) Bias at $V_{\mathrm{ce}} = 2.7$ V, $I_{\mathrm{b}} = 160$ μA.

Table 3. Residual data-fitting error of the four extracted bias points (0.8×10 μm device).

Bias point	$V_{\mathrm{ce}} = 1.2$ V, $I_{\mathrm{b}} = 60$ μA	$V_{\mathrm{ce}} = 1.7$ V, $I_{\mathrm{b}} = 40$ μA	$V_{\mathrm{ce}} = 2.2$ V, $I_{\mathrm{b}} = 140$ μA	$V_{\mathrm{ce}} = 2.7$ V, $I_{\mathrm{b}} = 160$ μA
Residual error	1.88%	2.36%	1.55%	1.26%

6. Conclusion

This paper presents an EM simulation-based small-signal model building method for InGaAs/InP DHBTs. Seven dummy structures are simulated to extract the parasitic elements rigorously, and port calibration is performed before simulation. Two typical structures OPEN and SHORT are used to determine the proper EM simulation settings. A simpler intrinsic equivalent circuit is proposed, C_{ce} is introduced to the conventional intrinsic small signal model to characterize the parasitic capacitance generated from collector electrode finger and emitter ground bar, all the intrinsic parameters are obtained through mathematical method carefully. The simulation results of the small-signal model are compared to the measurement data of three kinds of InP HBT devices with different emitter sizes, within the frequency range 0.1–50 GHz, excellent agreements are achieved at four different biases, which proves the effectiveness of the method. The errors of S parameters are also given. This accurate EM-based simulation method makes it convenient to extract parameters directly,

and the method avoids several disadvantages of conventional methods, leading to a more reliable small-signal building technique.

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