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A 4H-SiC trench MOSFET structure with wrap N-type pillar for low oxide field and enhanced switching performance

Pei Shen(沈培)[1,2], Ying Wang(王颖)[1,†], and Fei Cao(曹菲)[1]

[1] *The Key Laboratory of RF Circuits and Systems, Ministry of Education, Hangzhou Dianzi University, Hangzhou* 310018, *China*
[2] *The School of Mechanical and Electronic Engineering, Pingxiang University, Pingxiang* 337055, *China*

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An optimized silicon carbide (SiC) trench metal-oxide-semiconductor field-effect transistor (MOSFET) structure with side-wall p-type pillar (p-pillar) and wrap n-type pillar (n-pillar) in the n-drain was investigated by utilizing Silvaco TCAD simulations. The optimized structure mainly includes a p+ buried region, a light n-type current spreading layer (CSL), a p-type pillar region, and a wrapping n-type pillar region at the right and bottom of the p-pillar. The improved structure is named as SNPPT-MOS. The side-wall p-pillar region could better relieve the high electric field around the p+ shielding region and the gate oxide in the off-state mode. The wrapping n-pillar region and CSL can also effectively reduce the specific on-resistance ($R_{on,sp}$). As a result, the SNPPT-MOS structure exhibits that the figure of merit (FoM) related to the breakdown voltage (V_{BR}) and $R_{on,sp}$ ($V_{BR}^2 R_{on,sp}$) of the SNPPT-MOS is improved by 44.5%, in comparison to that of the conventional trench gate SJ MOSFET (full-SJ-MOS). In addition, the SNPPT-MOS structure achieves a much faster-witching speed than the full-SJ-MOS, and the result indicates an appreciable reduction in the switching energy loss.

Keywords: 4H-silicon carbide (4H-SiC) trench gate MOSFET, breakdown voltage (V_{BR}), specific on-resistance ($R_{on,sp}$), switching energy loss, super-junction

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1. Introduction

Wide-band gap third-generation semiconductor material silicon carbide offers excellent switching properties, temperature stability and low electromagnetic interference (EMI), making it ideal for next-generation power conversion applications such as switching power supplies, electric vehicles, and industrial power.[1–4] In recent years, SiC power MOSFETs with the V_{BR} of 600–1700 V level dominated have been commercialized, but higher V_{BR} of the SiC MOSFETs are less studied. Especially, the SiC trench gate MOSFET generally has low $R_{on,sp}$ due to the small cell-pitch using the trench gate configuration.[5–7] However, SiC trench gate MOSFET has a fatal disadvantage. As the drain–source voltage increases, the electric field at the bottom corner of the gate trench increases, affecting the gate oxide stability.[8,9] To overcome this issue, some good methods and novel structures are proposed to overcome the electric field concentration at the bottom corner of the gate trench.[10–12] The most commonly used way to shield highly the electric field at the bottom corner of the gate trench is to increase the p+ shield region under the gate trench,[13–15] yet with a marked increase in $R_{on,sp}$. With charge-balanced n-pillar and p-pillar, the super-junction (SJ) MOSFET has more superior electrical characteristics compared with conventional SiC trench MOSFET.[16–20] Vudumula *et al.*[16] studied the static and dynamic characteristics of the CoolSiC trench MOSFET structure by introducing the concept of super-junction, and the structure provides a good trade-off between gate oxide reliability and $R_{on,sp}$. Orouji *et al.*[17] proposed to replace the p+ shield region with an n-type pillar and a p-type pillar at the bottom of the gate trench. The new device structure improves the V_{BR} and reduces the $R_{on,sp}$, and has good switching characteristics. Deng *et al.*[18] studied a novel structure embedded in a floating p-column in the drift region, which ensures that the V_{BR} is not reduced, allowing for a compromise between the $R_{on,sp}$, and the short-circuit characteristics. Kim[19] proposed a novel SJ structure with a hetero-junction diode for improved reverse recovery characteristics and switching energy loss. He *et al.*[20] investigated a new SJ structure by using grounded p+ buried layers and connected p columns to encapsulate deep trench gate oxide to reduce the saturation current.

Moreover, the practical feasibility of fabricating super-junction structures has been discussed by using the trench-filling epitaxial growth method in some papers. Ji *et al.*[21,22] studied and made possible uniform epitaxial filling in the 4H-SiC trench between 7 μm and 50 μm deep. There have also been significant advances in understanding the mechanisms of epitaxial growth of trench filling.[23–25] In addition, Ryoji *et al.*[26] have established a key manufacturing process of super-junction structure with thickness over 20 μm and high aspect ratio, and the theoretical limit of 6.5-kV class 4H-SiC super-junction MOSFET is broken through by the trench filling epitaxial growth method. Consequently, it is feasible to study the trench-filled epitaxial growth method of SiC super-junction devices with high breakdown voltage.

†Corresponding author. E-mail: wangying7711@yahoo.com
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In this article, an improved structure of 4H-SiC trench gate MOSFET with a side-wall p-pillar and a wrapping n-pillar at the right of the p-pillar is studied to reduce the gate oxide electric field and switching energy loss. The Silvaco TCAD simulation results demonstrate that the SNPPT-MOS exhibits good static and dynamic performance. The SNNPT-MOS structure is a significant optimization of the full-SJ-MOS structure. In addition, in the second section, some preliminary manufacturing techniques are discussed, and their feasibility is proved from the processing point of view.

2. Description of the device structure and fabrication procedure

Figure 1 shows the schematic cross-section of the SNPPT-MOS and full-SJ-MOS.[27] The main device-related parameters of the two structures are shown in Figs. 1(a) and 1(b). The SNPPT-MOS structure mainly includes a p^+-SiC buried region, CSL region, a p-pillar, and a wrap n-pillar. The gate oxide thickness of both sidewalls and the bottom is about 50 nm. The height of the CSL region was 1.7 μm ($L_{CSL} = 1.7$ μm). The height of the p-pillar was 24 μm ($L_{p-pillar} = 24$ μm). The wrapped n-pillar junction depth (L_{wn}) was set to be 1 μm to decrease the impact to V_{BR} and gate-drain charge. The distance between the wrap n-pillar and the gate was set at 0.5 μm ($W_{ng} = 0.5$ μm). The thickness of the gate oxide was set at 50 nm. The n-drift region dopant concentration (N_d) was set to be 3×10^{15} cm^{-3}. Moreover, in the super-junction (SJ) MOSFET structure, the charge balance between the n-pillar and p-pillar must be precisely controlled. Thus, the products of the width and doping concentration of the n-pillar region of the two structures must equal to the product of the width and doping concentration of the p-pillar region the according to[16,17,28,29]

$$W_p \times N_p \approx W_n \times N_n, \tag{1}$$

where W_p and W_n are the widths of the p-pillar and n-pillar, N_p and N_n are doping concentrations of the p-pillar and n-pillar, respectively. The detailed parameters of the simulation used for the two structures are listed in Table 1.

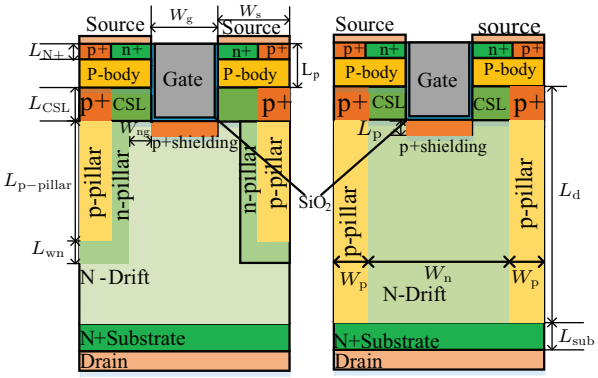


Fig. 1. The schematic cross-section of the (a) SNPPT-MOS and (b) full-SJ-MOS.

Table 1. Device parameters in simulations.

Device parameters	SNPPT-MOS	full-SJ-MOS
n+ source junction depth (L_{N+})	0.2 μm	0.2 μm
p+ junction depth	0.2 μm	0.2 μm
p-body junction depth	0.5 μm	0.5 μm
Gate trench depth	1.5 μm	1.5 μm
The thickness of the n-drift (L_d)	29.0 μm	29.0 μm
The thickness of the gate oxide	50 nm	50 nm
n-type current spreading layer depth (L_{CSL})	1.7 μm	1.7 μm
p-pillar depth ($L_{p-pillar}$)	24.0 μm	27.0 μm
Wrapped n-pillar junction depth (L_{wn})	1 μm	–
Width of the trench (W_g)	2.0 μm	2.0 μm
Width of the source (W_s)	2.5 μm	2.5 μm
n-drift doping concentration (N_d)	3.0×10^{15} cm^{-3}	1×10^{16} cm^{-3}
p-body doping concentration	2.0×10^{17} cm^{-3}	2.0×10^{17} cm^{-3}
n-type current spreading layer doping concentration	4.0×10^{16} cm^{-3}	4.0×10^{16} cm^{-3}
p-pillar doping concentration (N_p)	2.0×10^{16} cm^{-3}	2.0×10^{16} cm^{-3}
n-pillar doping concentration (N_n)	6.0×10^{16} cm^{-3}	–

A feasible manufacturing process of the SNPPT-MOS is shown in Fig. 2. An n-drift was grown on a 4H-SiC n+ substrate, as shown in Fig. 2(a). Fabrication of the super-junction structure began with a deep stripe-trench formation in an n-drift by using inductively coupled plasma etching in an SF_6/O_2 gas ambient, as shown in Fig. 2(b). The p-pillar region was fabricated with the trench-filling epitaxial (TFE) growth method,[26] as shown in Fig. 2(c). After TFE growth, the wafer surface was flattened by thinning the TFE grown wafer to the initial epitaxial wafer thickness by using grinding and polishing, as shown in Fig. 2(d). And then, CSL grew on the flat surface of the wafer. After CSL was formed, a mask plate of a certain size (distance between the two p-pillar) was manufactured to mask CSL, and p^+-SiC buried region were generated on both sides of the mask plate through ion implantation. The resulting structure is shown in Fig. 2(e). Then

remove the mask based on the structure in Fig. 2(e), and grow another layer of p-type 4H-SiC to form the p-body region. After the p-body region was formed, n^+-SiC source region was formed by ion implantation. Then, masks of the same size were used to mask certain n^+-SiC source region, and p^+-SiC source region was generated on both sides of the mask by ion implantation. The final structure is shown in Fig. 2(f). Finally, the p^+-shielding, the oxide layer, the gate structure, and the electrode were implemented in a similar way to the conventional SiC trench MOSFET, as shown in Figs. 2(g) and 2(h).

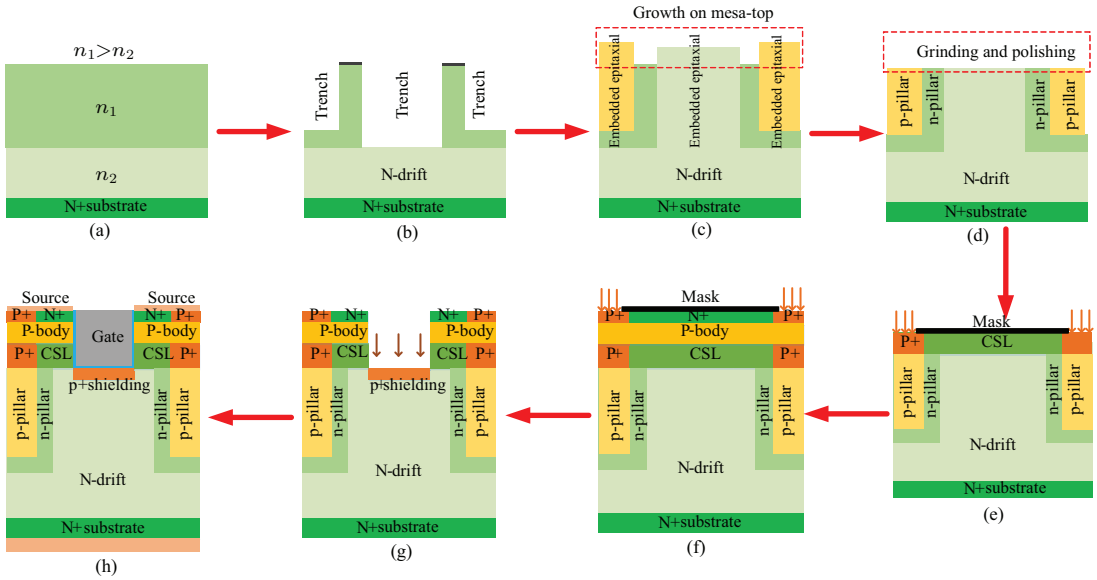


Fig. 2. The key fabrication procedure of the SNPPT-MOS.

Moreover, it is a very important step to align p^+-SiC buried region and p^+-SiC source region with p-pillar in the process of SNPPT-MOS structure. Firstly, for Fig. 1(d), ensure that the polishing process thinned the epitaxial wafer to the initial thickness of the epitaxial wafer, so that the wafer surface becomes sufficiently flat. Secondly, the size of the mask in Fig. 1(e) can be determined, that is, the distance between the p-pillar on both sides. In addition, in SiC devices, due to the low diffusion coefficient of dopant,[30] p^+-SiC buried region is formed by ion implantation, and the doping amount of ion implantation impurity can be precisely controlled. For Fig. 1(f), the p^+-SiC source region is firstly formed by ion implantation on both sides of the n^+-SiC source region. The mask used is the same size as that used in Fig. 1(e). And the p^+-SiC source region on both sides of the n^+-SiC source region is also formed by ion implantation, which can accurately control the amount of impurity doping. Therefore, the accurate alignment of align p^+-SiC buried region and p^+-SiC source with p-pillar is ensured to a certain extent.

At the same time, in order to better illustrate the feasibility of SNPPT-MOS structure. The V_{BR}, $R_{on,sp}$, and FoM ($V_{BR}^2 R_{on,sp}$) of p^+-SiC buried region width and p^+-SiC source region width from -10% to $+10\%$ deviation are simulated and discussed, as shown in Table 2. As can be seen from Table 2, the V_{BR} and $R_{on,sp}$ of the device are almost constant when the error of the alignment widths of the p^+-SiC source region and p^+-SiC buried region with p-pillar ranges from 0 to -10%. When p^+-SiC source region and p^+-SiC buried region are aligned with the width of p-pillar from 0 to $+10\%$, the V_{BR} of the device increases slightly and then decreases slightly, the $R_{on,sp}$ changes accordingly, and the FoM ($V_{BR}^2 R_{on,sp}$) is calculated to be almost the same.

Table 2. The V_{BR}, $R_{on,sp}$ and FoM ($V_{BR}^2/R_{on,sp}$) of p^+-SiC buried region width and p^+-SiC source region width from -10% to $+10\%$.

p^+-SiC buried width (μm)	p^+-SiC source width (μm)	V_{BR} (V)	$R_{on,sp}$ (mΩ·cm^2)	FoM ($V_{BR}^2/R_{on,sp}$) (MW/cm^2)
1.35	1.35	4712	9.87	2.24
1.38	1.38	4712	9.87	2.24
1.41	1.41	4713	9.90	2.24
1.44	1.44	4713	9.90	2.24
1.47	1.47	4713	9.90	2.24
1.50	1.50	4713	9.90	2.24
1.53	1.53	4752	10.01	2.25
1.56	1.56	4784	10.18	2.24
1.59	1.59	4802	10.23	2.25
1.62	1.62	4561	9.24	2.25
1.65	1.65	4628	9.56	2.24

3. Numerical simulation and result analysis

In this section, the static characteristics and the dynamic characteristics of the SNPPT-MOS were simulated by using the 2-D Silvaco ATLAS tool and compared the performance of the full-SJ-MOS with the performance of the SNPPT-MOS. In this simulation, some physical models were used. The physical models are divided into four parts. The first part is the mobility model, where the simulation uses the concentration and temperature-related mobility model (ANALYTIC) and the

parallel electric field correlation model (FLDMOB). The second part is the composite model, where the simulation uses the Shockley–Read–Hall complex model (SRH) and the Auger complex model (AUGER). The third part is the carrier generation model, where the IMPACT SELB model is used in the simulation. The fourth part is the carrier statistical model. The incomplete ionization model (INCOMPLETE) is used in the simulation.[31–33]

3.1. On-state characteristic

The on-state output characteristic curves of the SNPPT-MOS and full-SJ-MOS at $V_{gs} = 20$ V, $V_{gs} = 16$ V, $V_{gs} = 12$ V, and $V_{gs} = 8$ V are shown in Fig. 3. The $R_{on,sp}$ of the SNPPT-MOS was 9.90 mΩ·cm^2, and the $R_{on,sp}$ of the full-SJ-MOS was 11.5 mΩ·cm^2, at $V_{gs} = 16$ V and $V_{ds} = 1$ V. The wrap n-pillar and CSL region in the optimized structure provide two diffusion paths for current diffusion and compress the depletion region. The thin light doping of the CSL region causes the electrons to diffuse horizontally earlier.

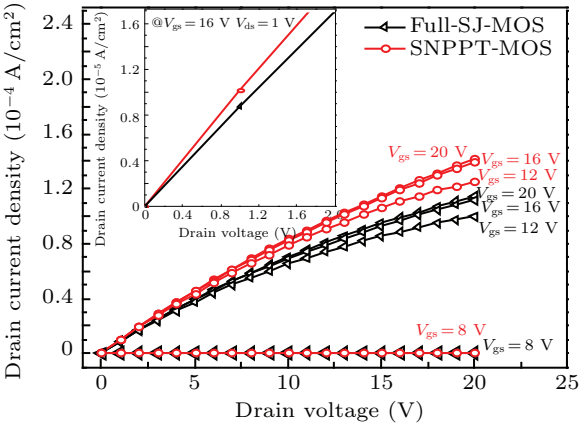


Fig. 3. The on-state output characteristic curves for the SNPPT-MOS and full-SJ-MOS.

In addition, the wrap n-pillar allows the current to flow vertically. We know that the more narrow the depletion region, the wider the current path of the electron, resulting in the lowest $R_{on,sp}$. Compared with full-SJ-MOS, the $R_{on,sp}$ of SNPPT-MOS decreased by 16.2%. The $R_{on,sp}$ of the SNPPT-MOS is slightly lower than that of full-SJ-MOS because the SNPPT-MOS structure has a higher doping concentration in wrap n-pillar. In the SNPPT-MOS structure, the wrap n-pillar under the CSL the electron concentration in the channel region, while the depletion region decreases, increasing the current path in the SNPPT-MOS structure, as shown in Fig. 4. The equation of the $R_{on,sp}$ can be described as

$$R_{on,sp} = \left(\frac{W_d}{q\mu_n N_d}\right), \tag{2}$$

where W_d is the maximum depletion width and the μ_n is the electron's mobility.

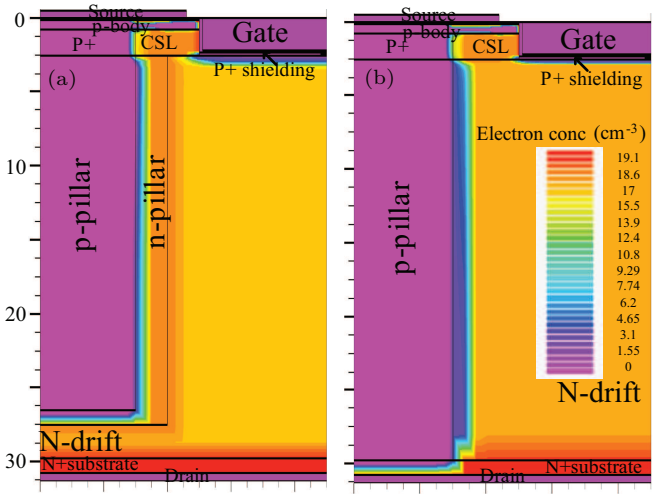


Fig. 4. Distribution of the electron concentration for (a) SNPPT-MOS and (b) full-SJ-MOS.

3.2. Off-state characteristics

Figure 5 shows the off-state breakdown characteristic curves for the SNPPT-MOS and full-SJ-MOS. The corresponding electric field in the gate oxide distributions is shown in Fig. 6.

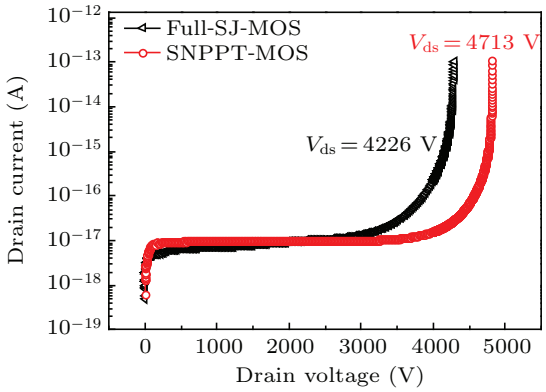


Fig. 5. OFF-state breakdown characteristic curves of the SNPPT-MOS and full-SJ-MOS.

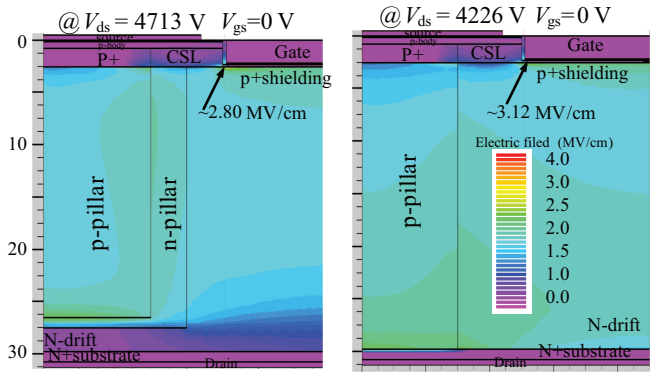


Fig. 6. OFF-state corresponds to electric field curves of (a) SNPPT-MOS and (b) full-SJ-MOS.

We can see that the peak electric field in the gate oxide ($E_{peak-goe}$) in the full-SJ-MOS structure has reached 3.12 MV/cm with a drain bias voltage of 4226 V. In the SNPPT-MOS structure, the value of the $E_{peak-goe}$ is about

2.80 MV/cm with a drain bias of 4713 V. The SNPPT-MOS exhibits lower $E_{\text{peak-goe}}$ than the full-SJ-MOS, this is because of the mutual depletion effect of the p-pillar and the wrap n-pillar in the n-drift, and the electric field around the bottom of the gate trench could be screened effectively. As for the full-SJ-MOS structure, it could also alleviate the high electric field around the bottom of the gate trench to a certain extent due to the p-pillar embedded n-drift region, while the high doping concentration of the n-drain region and thus the $E_{\text{peak-goe}}$ (3.12 MV/cm) is slightly higher than the SNPPT-MOS, resulting in a V_{BR} witha drain bias of 4226 V. The vertical electric field distributions of the SNPPT-MOS and the full-SJ-MOS from 0 to 30 μm are shown in Fig. 7. The maximum gate oxide electric field is about 2.5 μm vertically. From 2.5 μm onward, the vertical electric field curve of SNPPT-MOS is almost as flat as that of the full-SJ-MOS. Because of the mutual depletion effect of the p-pillar and the wrap n-pillar in the n-drain region, the field distributions for the SNPPT-MOS at the p-pillar and the wrap n-pillar interface are uniforms.

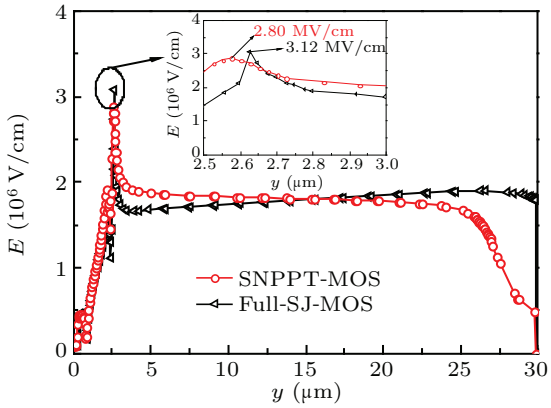


Fig. 7. The vertical distribution of the electric field from 0 to 30 μm.

3.3. Reverse transfer capacitance and gate charge characteristics

The smaller reverse transfer capacitance is of great importance for reducing the switching loss and preventing the false turn-on. It helps improve the switching characteristics. The reverse transfer capacitance ($C_{\text{rss}} = C_{\text{gd}}$) properties of the SNPPT-MOS and full-SJ-MOS are shown in Fig. 8. Compared with the C_{rss} of the full-SJ-MOS, the SNPPT-MOS exhibits a lower C_{gd} than the full-SJ-MOS, owing to the effective electric field shielding of the p-pillar and wrap n-pillar. And they have a smaller p–n junction area than the conventional full super-junction structure.

The specific gate charge ($Q_{\text{g,sp}}$) characteristic curves of the SNPPT-MOS and the full-SJ-MOS are evaluated as well, as shown in Fig. 9. The $Q_{\text{g,sp}}$ is extracted by using the mix-mode simulation. The simulation circuit schematic diagram is inserted in the bottom right corner of Fig. 9. The extracted $Q_{\text{gd,sp}}$ of the SNPPT-MOS is 101 nC/cm^2. The SNPPT-MOS exhibits a lower miller charge compared with that of the 154 nC/cm^2 for the full-SJ-MOS due to the p-pillar and wrapped n-pillar having smaller p–n junction area and effective electric field shielding ability. The FoM ($R_{\text{on,sp}} \times Q_{\text{gd,sp}}$) is a widely used parameter to measure the device performance in high-frequency switching applications.[34–36] According to the calculation, the FoM ($R_{\text{on,sp}} \times Q_{\text{gd,sp}}$) of the full-SJ-MOS structure is 1771 mΩ·nC. The SNPPT-MOS structure obtained superior $R_{\text{on,sp}} \times Q_{\text{gd,sp}}$ with a value of 999.9 mΩ·nC, which decreases by 77.1% compared with the full-SJ-MOS structure.

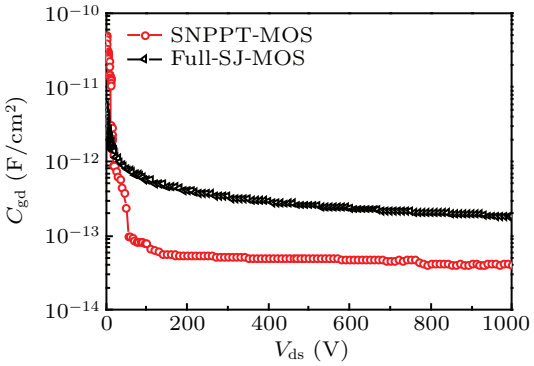


Fig. 8. The C_{rss} property curves of the SNPPT-MOS and full-SJ-MOS.

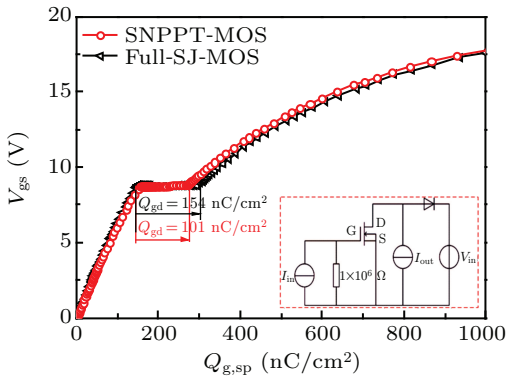


Fig. 9. The $Q_{\text{g,sp}}$ characteristic curves of the SNPPT-MOS and full-SJ-MOS.

3.4. Dynamic characteristics

To better study the switching characteristics of the SNPPT-MOS, the double-pulse test (DUT) circuit is used to investigate the switching performance of the two structures, as shown in Fig. 10. The basic parameters of the DUT circuit are listed in Table 3. Figure 11 shows the switching waveforms of the SNPPT-MOS and full-SJ-MOS. As can be seen from Fig. 11, the full-SJ-MOS needs a longer period to arrive at high V_{ds} and high I_{ds} compared with the SNPPT-MOS. T_{OFF} is defined as the turn-off delay time and turn-off fall time. T_{ON} is defined as the turn-on delay time and turn-on fall time.

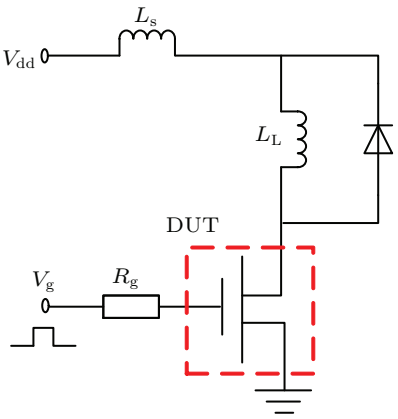


Fig. 10. The double-pulse test circuit.

Table 3. The basic parameters of the DUT circuit.

Parameters	Values	Unit
Supply voltage (V_{dd})	300	V
Gate resistor (R_g)	20	Ω
Inductive load (L_L)	200	μH
Stray inductance (L_s)	10	nH
Gate voltage (V_g)	0–20	V

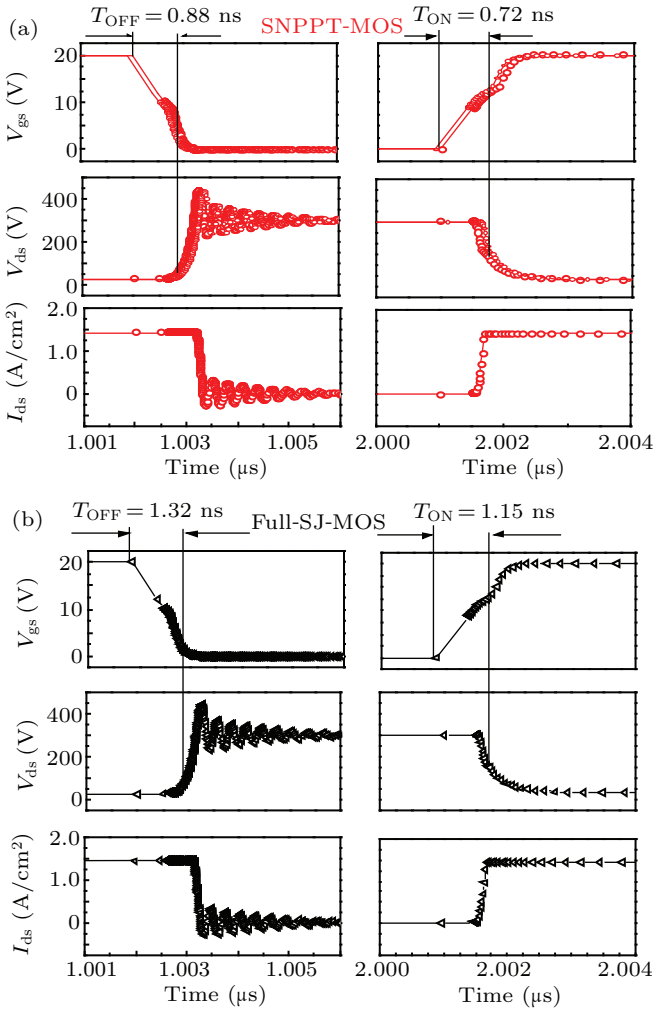


Fig. 11. Switching waveforms of (a) SNPPT-MOS and (b) full-SJ-MOS.

Figure 12 shows the switching energy loss for the SNPPT-MOS and the full-SJ-MOS. The calculated energy loss values of turn-on (E_{on}) and turn-off (E_{off}) for SNPPT-MOS are 32.5 mJ/cm^2 and 31.7 mJ/cm^2. The calculated values of E_{on} and E_{off} for full-SJ-MOS are 40.3 mJ/cm^2 and 36.5 mJ/cm^2. It can be discerned that in the SNPPT-MOS structure, the energy loss during E_{on} is reduced as a respective decrease of 24.% compared with the full-SJ-MOS, and the E_{off} is a respective decrease of 15.1% compared with the full-SJ-MOS. The equation of the E_{on} and E_{off} can be described as

$$E_{on} = \int_{T_1}^{T_2} V_{ds} \times I_{ds}\,dt, \tag{3}$$

$$E_{off} = \int_{T_3}^{T_4} V_{ds} \times I_{ds}\,dt, \tag{4}$$

where T_1 (10% of V_{gs}(on)), T_2 (2% of V_{dd}), T_3 (90% of V_{gs}(on)) and T_4 (2% of I_{ds}).

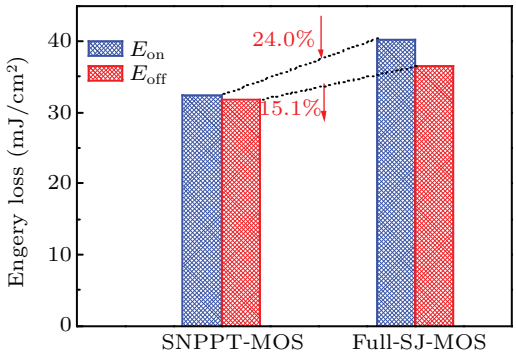


Fig. 12. Switching energy loss of the SNPPT-MOS and full-SJ-MOS.

3.5. Parameters optimization

To get the optimized device structure, the added wrap n-pillar dopant concentration (N_n), p-pillar dopant concentration (N_p), and the height of the p-pillar (H) have a great influence on the device performance. In the SJ MOSFET structure, to obtain high V_{BR}, it is necessary to control accurately the charge balance between n-pillar and p-pillar regions. So the products of the width and concentration of the n-pillar region of the SNPPT-MOS must equal the product of the width and concentration of the p-pillar region. Figure 13 shows the V_{BR} and $R_{on,sp}$ of this SNPPT-MOS structure in the case of N_p from 1×10^{16} cm^{-3} to 3×10^{16} cm^{-3}, N_n from 3×10^{16} cm^{-3} to 9×10^{16} cm^{-3}, and H from 10 μm to 24 μm. And the FoM ($V_{BR}^2/R_{on,sp}$) corresponding to different H is given in detail. Figure 14 shows FoM ($V_{BR}^2/R_{on,sp}$) as a function of the different N_n, N_p, and H. The maximum FoM that appears at the N_n, N_p, and H are 6×10^{16} cm^{-3}, 2×10^{16} cm^{-3}, and 24 μm, respectively. We also investigated the most suitable W_{ng}. The W_{ng} from 0.1 μm to 0.7 μm, as shown in Fig. 15, we can see that the smaller the W_{ng} was, the smaller the $R_{on,sp}$ of the SNPPT-MOS was. However, the V_{BR} also decreased. As can be seen from Fig. 15, we can find that the most suitable W_{ng} was 0.5 μm.

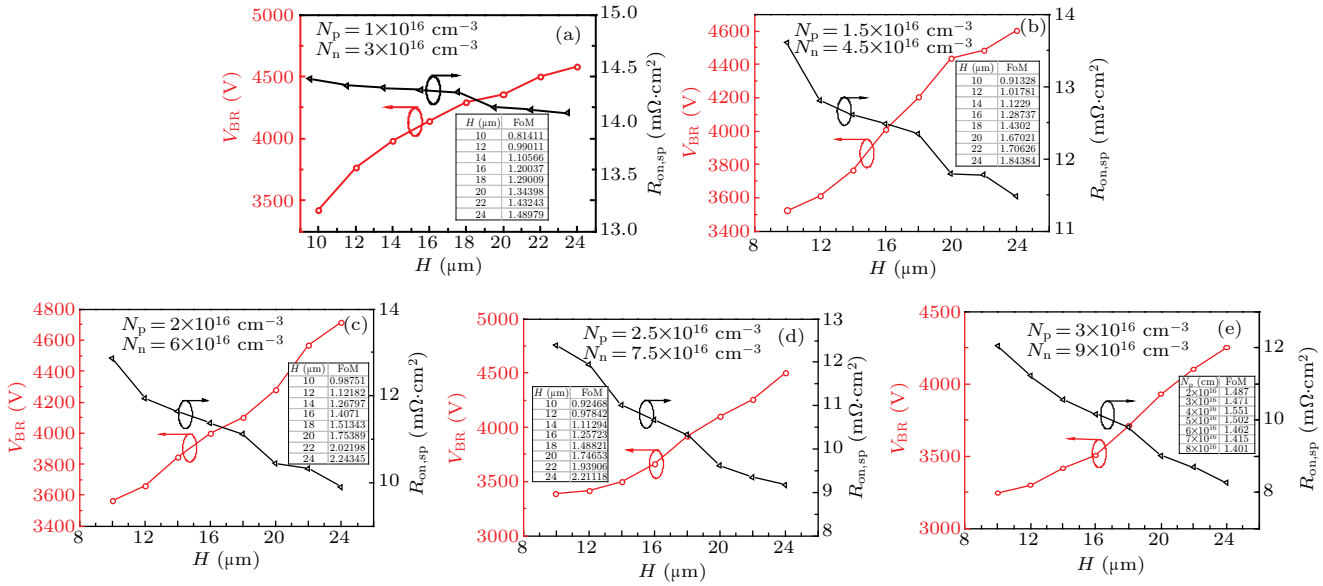


Fig. 13. The V_{BR} and $R_{on,sp}$ as function N_p and N_n for different heights of the p-pillar.

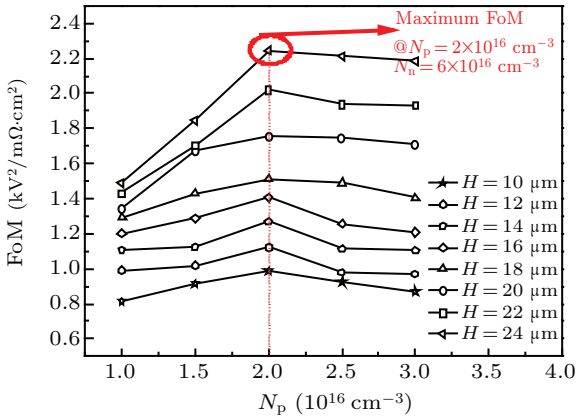


Fig. 14. FoM ($V_{BR}^2/R_{on,sp}$) as a function of the different N_n, N_p, and H.

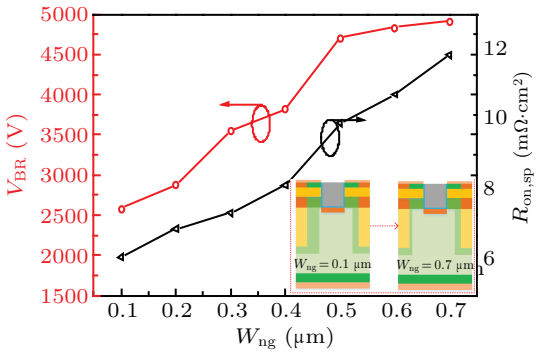


Fig. 15. The V_{BR} and $R_{on,sp}$ for the different distances between the n-pillar and the gate (W_{ng}).

Table 4 gives the V_{BR}, $R_{on,sp}$, and FoM when W_{ng} is set at 0.5 μm. The higher the N_n, and the smaller the V_{BR} and $R_{on,sp}$ of the SNPPT-MOS. The FoM value increases firstly and then decreases. The main reason is that when N_n is low, the depletion region in the n-pillar is wider, which makes the current path narrow. As the N_n value increases, the electron path becomes wider. As the doping concentration of n-pillar is higher than that of drift, the increase of N_n significantly improves the reduction of $R_{on,sp}$. When N_n is low, the reduction of $R_{on,sp}$ has more effect on FoM than that of V_{BR}. However, when N_n is high, the effect of the decrease of $R_{on,sp}$ on FoM is less than that of the decrease of V_{BR}.

Table 4. The V_{BR}, $R_{on,sp}$, and FoM at $W_{ng} = 0.5$ μm.

N_n (cm^{-3})	V_{BR} (V)	$R_{on,sp}$ (mΩ·cm^2)	FoM ($V_{BR}^2/R_{on,sp}$)
2.0×10^{16}	4901	13.10	1.83
4.5×10^{16}	4826	10.62	2.19
6.0×10^{16}	4713	9.90	2.24
7.5×10^{16}	4003	8.33	1.92
9.0×10^{16}	3807	7.69	1.88

Table 5 gives the V_{BR}, $R_{on,sp}$, and FoM when N_n is 6×10^{16} cm^{-3}. As can be seen from Table 5, we can find that the wider the W_{ng}, the larger the $R_{on,sp}$ and the V_{BR}. The FoM value increases firstly and then decreases. The main reason is that when the W_{ng} is smaller, the larger the area of the electron flow through the n-pillar. The area of electrons flow through in the n-pillar is larger than the depletion region. With the increase of W_{ng}, the area of electrons flowing through the n-pillar increases. It is because of the high doping concentration of the n-pillar that the area of electrons flows through the n-pillar increases, which promotes the decrease of $R_{on,sp}$. When W_{ng} is small, the effect of $R_{on,sp}$ on FoM is greater than that of V_{BR}. With the increase of W_{ng}, the contribution of $R_{on,sp}$ to FoM decreased. In the larger W_{ng} condition, the increase of $R_{on,sp}$ had less effect on FoM than that of V_{BR}. Therefore, we choose these two parameters as the basement of our simulations and the following discussion. The electrical property of the full-SJ-MOS and the SNPPT-MOS are listed in Table 6.

Table 5. The V_{BR}, $R_{on,sp}$, and FoM at $N_n = 6 \times 10^{16}$ cm^{-3}.

W_{ng} (μm)	V_{BR} (V)	$R_{on,sp}$ (mΩ·cm^2)	FoM ($V_{BR}^2/R_{on,sp}$)
0.1	2583	6.09	1.09
0.2	2880	6.89	1.2
0.3	3550	7.35	1.71
0.4	3823	8.13	1.79
0.5	4713	9.9	2.24
0.6	4840	10.72	2.18
0.7	4921	11.84	2.04

Table 6. Electrical property of the SNPPT-MOS and the full-SJ-MOS.

Parameters	SNPPT-MOS	full-SJ-MOS	Unit
V_{BR}	4713	4226	V
$R_{on,sp}$	9.90	11.50	mΩ·cm^2
$Q_{gd,sp}$	101	154	nC/cm^2
FOM ($V_{BR}^2/R_{on,sp}$)	2.24	1.55	MW/cm^2
FOM ($R_{on,sp} \times Q_{gd,sp}$)	999.9	1771	mΩ·nC
E_{on}	32.5	40.3	mJ/cm^2
E_{off}	31.7	36.5	mJ/cm^2

4. Conclusion and perspectives

An optimized structure of the 4H-SiC trench MOSFET is studied in this article. The improved structure exhibits good electrical characteristics due to the incorporating side-wall p-pillar region and a wrapping n-pillar region in the drift region. The SNPPT-MOS structure has significantly protected the gate oxide and relieves the electric field around the p+ shielding region. With charge-balanced n-pillar and p-pillar under the p-body, the improved structure help reducing the $R_{on,sp}$, which leads to the tradeoff of the V_{BR} and $R_{on,sp}$. In addition, the improved structure exhibit superior switching property during both the turn-on and the turn-off transients.

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