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**Citation:**Chin. Phys. B, 2022, 31 (**5**): 057301. DOI: 10.1088/1674-1056/ac48fb
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Chin. Phys. B, 2020, 29 (**8**): 087304. DOI: 10.1088/1674-1056/ab8daa

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# Improved device performance of recessed-gate AlGaN/GaN HEMTs by using *in-situ* $N_2O$ radical treatment

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(Received 31 August 2021; revised manuscript received 7 November 2021; accepted manuscript online 7 January 2022)

The $N_2O$ radicals *in-situ* treatment on gate region has been employed to improve device performance of recessed-gate AlGaN/GaN high-electron-mobility transistors (HEMTs). The samples after gate recess etching were treated by $N_2O$ radicals without physical bombardment. After *in-situ* treatment (IST) processing, the gate leakage currents decreased by more than one order of magnitude compared to the sample without IST. The fabricated HEMTs with the IST process show a low reverse gate current of $10^{-9}$ A/mm, high on/off current ratio of $10^8$, and high $f_T \times L_g$ of 13.44 GHz·μm. A transmission electron microscope (TEM) imaging illustrates an oxide layer with a thickness of 1.8 nm exists at the AlGaN surface. X-ray photoelectron spectroscopy (XPS) measurement shows that the content of the Al–O and Ga–O bonds elevated after IST, indicating that the Al–N and Ga–N bonds on the AlGaN surface were broken and meanwhile the Al–O and Ga–O bonds formed. The oxide formed by a chemical reaction between radicals and the surface of the AlGaN barrier layer is responsible for improved device characteristics.

**Keywords:** AlGaN/GaN, high-electron-mobility transistors, low gate leakage, radio frequency, radical treatment

**PACS:** 73.40.Kp, 81.05.Ea, 85.30.De, 85.30.Tv **DOI:** 10.1088/1674-1056/ac48fb

## 1. Introduction

As a typical representative of the third generation semiconductors, gallium nitride (GaN) is widely used in high frequency, high voltage, high power, and many other fields due to its superior material characteristics.[1–5] For many years, recessed gate process has been widely used in the fabrication of GaN-based devices. However, in the process of plasma etching gate recess, it often suffers from either serious etching damage or large device leakage current.[6–8] In order to improve the device characteristics, different interface treatment methods after recess etching have been widely studied, such as annealing after recess etching,[9] plasma treatment,[10–12] solution treatment,[13,14] and so on. Mi *et al.* used $N_2O$ plasma to treat the interface by plasma-enhanced chemical vapor deposition (PECVD).[15] Chiu *et al.* employed reactive ion etching (RIE) to produce $N_2O$ plasma for oxidizing the interface of the device.[16] Therefore, $N_2O$ has become popular for improving the interface quality in the fabrication process of GaN-based devices.[17,18] However, high temperature annealing could not only increase the complexity of the process, but also activate deep level defects and exacerbate current collapse.[19] Solution treatment also has to face the challenge of environmental problems. Moreover, physical bombardment resulting from negative self-bias voltage is inevitable in the process of PECVD and RIE plasma treatments, which will weaken the suppression of gate leakage current.[11,18] Therefore, an interface processing method with no or little physical bombardment is urgently needed to enhance the suppression effect of gate leakage current.

The surface damage caused by physical bombardment can be effectively avoided in the process of interface treatment by inductively coupled plasma (ICP) plasma. The ICP etching system consists of two RF power sources with the frequency of 13.56 MHz. When only the ICP coil power is turned on and the ICP bias power is set to zero, there is no self-bias voltage, since the charged particles are not accelerated in the direction towards the wafer, in these conditions. This plasma is mainly composed of unionized molecules, various electrically neutral radicals and charged particles. Among them, the radicals have the most active chemical activities without bombardment effect, and the chemical reactions of plasma are mainly the contribution of these active radicals.[20] Therefore, radicals produced by ICP can be utilized as a new interface treatment method.

In this work, we propose the $N_2O$ radicals *in-situ* treatment (IST) on gate region to reduce the gate leakage current of gate recessed AlGaN/GaN high-electron-mobility transistors (HEMTs). After gate recess etching by chlorine, the sample were treated by $N_2O$ radicals in etcher. Compared with the sample without IST, the gate leakage current of the sam-

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ple after IST processing decreased by more than one order of magnitude. The fabricated HEMTs with gate length of 0.6 μm after the IST process show a low reverse gate current of $2.4 \times 10^{-9}$ A/mm, high on/off current ratio of $3.6 \times 10^{8}$, and high $f_T \times L_g$ of 13.44 GHz · μm. An oxide layer with a thickness of 1.8 nm exists on the AlGaN surface according to the transmission electron microscope (TEM) imaging. X-ray photoelectron spectroscopy (XPS) measurement shows that the content of the Al–O and Ga–O bonds increased after IST, indicating that the Al–N and Ga–N bonds on the surface were broken and meanwhile the Al–O and Ga–O bonds formed. The oxide formed by a chemical reaction between radicals and the surface of the AlGaN barrier layer is responsible for improved device characteristics.

## 2. Device fabrication

As illustrated in Fig. 1(a), the HEMT in this work is composed of AlN nucleation layer, GaN buffer layer (1.5 μm), unintentionally doped GaN channel, AlN insert layer (1 nm), $Al_{0.24}Ga_{0.76}N$ barrier layer (22 nm) and GaN cap layer (2 nm) grown by MOCVD on sapphire substrate. Room-temperature Hall measurements showed an electron sheet concentration of $8.16 \times 10^{12}$ cm$^{-2}$ and a mobility of 1937 cm$^2$/V·s.

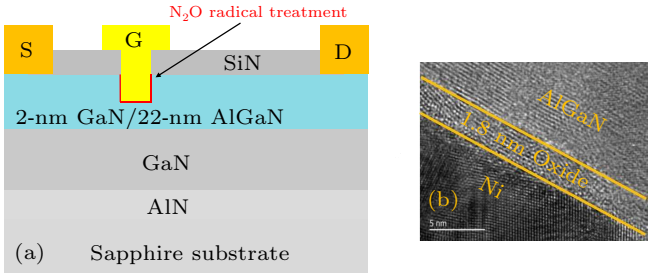



**Fig. 1.** (a) Schematic cross section of the proposed AlGaN/GaN HEMTs and (b) Scanning transmission electron microscopy image on a cross-section from the IST sample in the gate interface region.

The process flow started with a Ti/Al/Ni/Au ohmic contact deposited by electron beam evaporation, followed by annealing at 840 °C for 30 s in nitrogen ambient. Then the device isolation was achieved by $BCl_3/Cl_2$ based etching with the etching depth of 140 nm. The measured ohmic contact resistance was 0.42 Ω·mm using transmission line model (TLM). A 60-nm SiN passivation layer was deposited with PECVD, and the gate foot was defined by photolithography. After the SiN layer under the gate electron was removed by $CF_4$-based plasma, gate recess was performed by $BCl_3/Cl_2$-based plasma with ICP, of which total etching depth is 74.5 nm by atomic force microscope (AFM). Two control groups were set. The sample A without IST process served as a control group after gate recess etching, and the sample B was treated by $N_2O$ radical to react with the AlGaN surface in high vacuum reaction chamber of ICP for 20 minutes. The ICP source power and the bias power were applied by 200 W and 0 W, respectively. The chamber pressure was 15 mTorr (1 Torr = $1.33322 \times 10^2$ Pa) with the $N_2O$ flow rate of 60 sccm. And the temperature of chuck was 40 °C. There was no DC-bias voltage in the entire IST process. In the gate region of sample B, a 1.8-nm oxide layer was obtained as shown in Fig. 1(b). An Ni/Au (45 nm/120 nm) gate metal was deposited by electron beam evaporation after gate head lithography. In the whole processes, the two samples have the same process conditions except the IST time. The two types of HEMTs have a gate width of 50 μm, gate–source spacing of 1.4 μm, gate length of 0.6 μm, and gate–drain spacing of 2.8 μm. In addition, a circular shape Schottky barrier diode (SBD) with an anode radius of 65.0 μm were used for the capacitance–voltage measurements.

## 3. Results and discussion

The surface morphology of two samples in gate region scanned by AFM is shown in the Fig. 2(a) (sample A) and 2(b) (sample B). After IST, the surface roughness in terms of root mean square (RMS) changes from 0.336 nm to 0.286 nm, which shows IST process does not deteriorate the surface morphology of AlGaN layer.

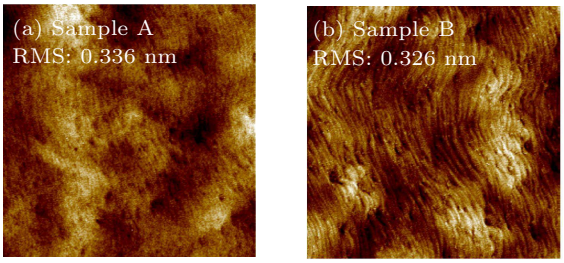



**Fig. 2.** The morphology of recess gate with (a) no IST (sample A) and (b) IST (sample B) by AFM scanning (5 μm × 5 μm).

The transfer *I*–*V* and output characteristics of the two devices at $V_d = 10$ V are compared as illustrated in Figs. 3(a) and 3(b). Table 1 shows the threshold voltages ($V_{th}$), peak transconductance ($G_{mmax}$) and $I_{ON}/I_{OFF}$ of the two kinds of HEMTs. The $V_{th}$ is defined as the gate-bias intercept of the linear extrapolation of drain current at the peak transconductance. It is found that the $V_{th}$ of sample A is −1.6 V and that of sample B is −1.3 V which is floating forward by 0.3 V. This is because that the effective thickness of the barrier layer decreases due to the oxidation of 1.8-nm AlGaN on the surface of the barrier layer by IST (as shown in Fig. 1(b)).[21] At $V_g$ of −6 V, the drain leakage currents for two types of HEMTs are $5.3 \times 10^{-9}$ and $1.7 \times 10^{-7}$ A/mm with and without IST respectively. The corresponding $I_{ON}/I_{OFF}$ ratio increases by more than one order of magnitude. Figure 3(b) compares the output characteristics of two types of HEMTs, at a gate voltage of −6 V ∼ 2 V and step of 1 V. It is found that the on-resistance of the devices are the same as 2.8 Ω·mm and 2.7 Ω·mm

for samples A and B respectively. And the saturation output currents of two kind of HEMTs were 905 mA/mm and 875 mA/mm. After IST, the on-resistance decreases slightly. The on-resistance of HEMT can be expressed by the following expression:

$$R_{\text{on-total}} = 2R_{\text{con}} + R_{\text{gs}} + R_{\text{recess}} + R_{\text{gd}}, \tag{1}$$

where $R_{\text{on-total}}$ is the total on-resistance, $R_{\text{con}}$ is the ohmic contact resistance determined by transfer line method, $R_{\text{gs}}$ is the channel resistance between gate and source, $R_{\text{gd}}$ is the channel resistance between gate and drain, and $R_{\text{recess}}$ refers to the channel resistance under the gate. Judging from the TLM analysis, the contact resistance ($R_{\text{con}}$) and block resistance ($R_{\square}$) for the HEMTs without IST are the same as the ones for the HEMTs with IST. Thus, $R_{\text{con}}$, $R_{\text{gs}}$, and $R_{\text{gd}}$ remain unchanged during IST because of the constant $R_{\text{con}}$ and $R_{\square}$. And the variation of $R_{\text{on-total}}$ depends on $R_{\text{recess}}$. This means that the gate resistance of the HEMTs does not degenerate after IST. Figure 3(c) shows the gate Schottky characteristics of the two devices. When $V_{\text{g}} = -10$ V, the gate leakage current decreases from $1.8 \times 10^{-7}$ A/mm before IST to $2.4 \times 10^{-9}$ A/mm, which reduces by more than one order of magnitude. The Schottky barrier height can be extracted by the CV ring on the same sheet.[22] And the barrier height are 1.02 eV and 0.86 eV, respectively, for the HEMTs with IST and without IST. The increase of Schottky barrier height not only suppresses the gate reverse leakage current,[23,24] but also promotes the positive drift of device threshold voltage.[21] Figure 3(d) shows the curve of channel electron field effect mobility ($\mu_{\text{FE}}$) with gate bias in the linear region. The $\mu_{\text{FE}}$ of the all HEMTs channel was extracted by fat field-effect transistors (FATFETs) with $L_{sg}$, $L_{\text{g}}$, $L_{\text{gd}}$, and $W_{\text{G}}$ of 3 μm, 50 μm, 3 μm, and 100 μm to reduce the influence of source and drain resistances. The peak $\mu_{\text{FE}}$ of HEMT with IST is 1409 $\text{cm}^2/\text{V}\cdot\text{s}$, however, ones of HEMT without IST is 1349 $\text{cm}^2/\text{V}\cdot\text{s}$. It was probably due to the fact that $N_2O$ radicals repaired the etching damage of gate region to a certain extent and reduced the surface trap density of states.[25]

**Table 1.** Comparison of $V_{\text{th}}$, $G_{\text{mmax}}$, $I_{\text{on}}/I_{\text{off}}$, and $I_{\text{dmax}}$ of HEMTs without and with IST.

| | Sample A | Sample B |
|---|---|---|
| $V_{\text{th}}$ (V) | −1.6 | −1.3 |
| $G_{\text{mmax}}$ (mS/mm) | 332 | 337 |
| $I_{\text{ON}}/I_{\text{OFF}}$ | $1.0 \times 10^7$ | $3.6 \times 10^8$ |
| $I_{\text{dmax}}$ (mA/mm) | 905 | 875 |

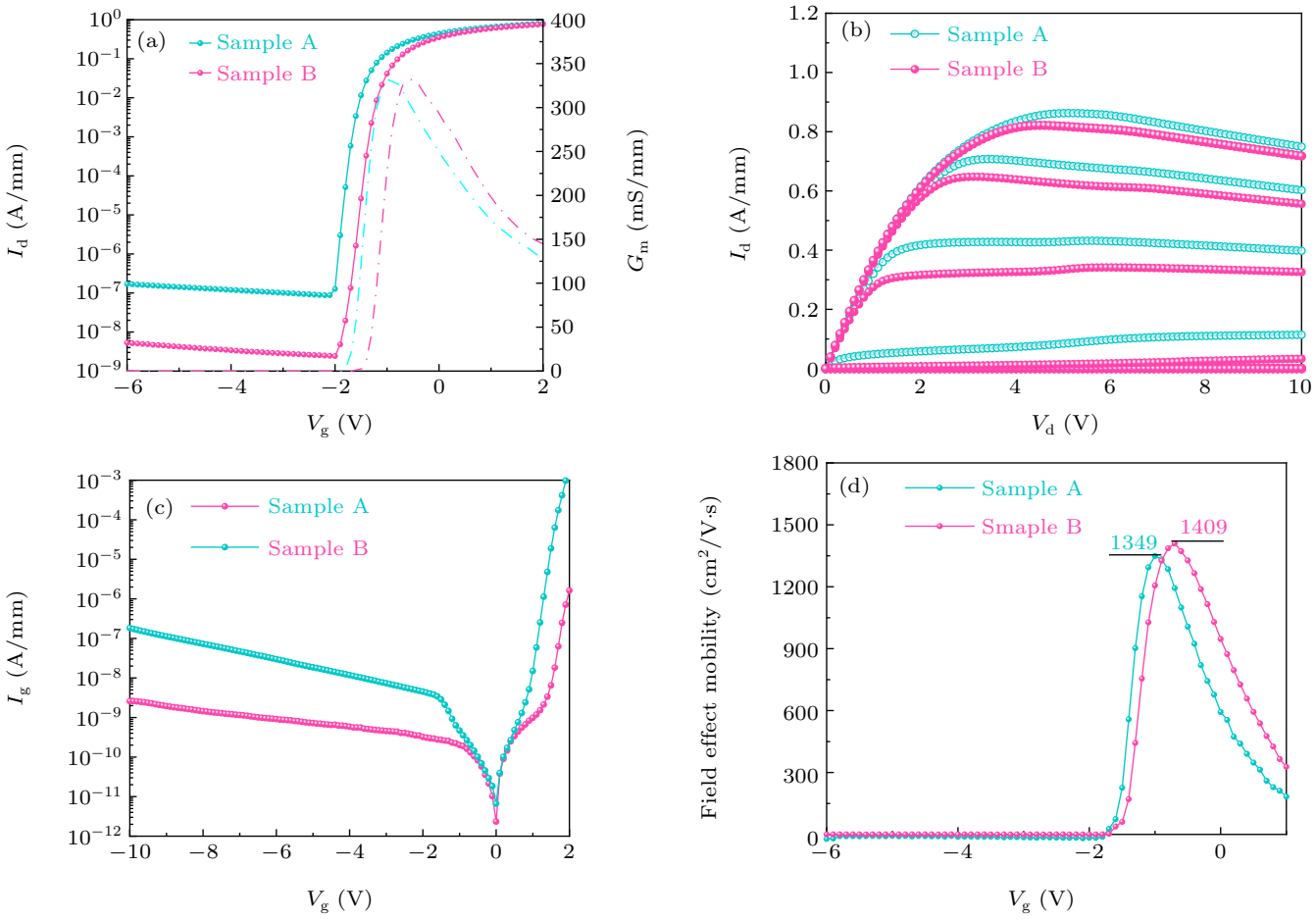



**Fig. 3.** (a) Transfer characteristics, (b) output characteristics, (c) gate Schottky characteristics, and (d) $\mu_{\text{FE}}$ as a function of $V_{\text{g}}$ for HEMTs with and without IST.

Figure 4 illustrates the capacitance–voltage characteristics of the two types of Schottky diodes with different treatment processes at 100 kHz. Compared with sample A, the turn-on voltage of sample B is floating by 0.3 V, which is consistent with the transfer characteristics shown in Fig. 3(a). The depth profile calculated by the *C*–*V* measurement shows that the peak concentrations of electrons for two samples are in the position of 9.5 nm, as shown in the inset of Fig. 4. This shows that the chemical reaction between $N_2O$ radicals and AlGaN layer does not change the distance between gate electrode and two-dimensional electron gas (2DEG) channel. However, the 2DEG concentration ($n_s$) of the channel after IST is reduced to 55% of that of the channel without IST, which may be because the IST process oxidizes the AlGaN surface layer and reduces the thickness of the remaining barrier layer.[26] The decrease of $n_s$ leads to a slight decrease in the saturated output current of the device with IST, as shown in Fig. 3(b). What is more, the smaller the $n_s$, the more positive bias voltage is required to clamp off the channel, that is, the more positive the corresponding threshold voltage. Therefore, in this study, sample B (with IST) has a more positive threshold voltage.

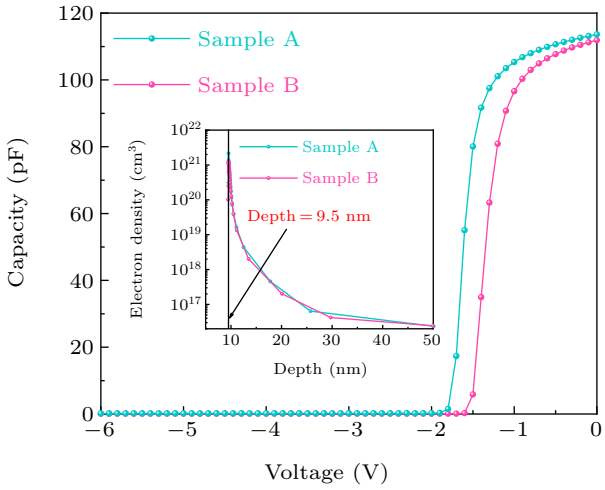



**Fig. 4.** The *C*–*V* characteristics of sample A and sample B.

The XPS method is also adopted to investigate the surface chemical composition of two samples. The Al 2p and the O 1s core level spectra are illustrated in Figs. 5(a) and 5(b), respectively. As shown in Fig. 5(a), the Al 2p core–level spectrum is a coupling of two components corresponding to Al–O and Al–N bonds. After IST, the intensity of Al–O bond was elevated, indicating that some Al–N bonds on the surface are broken and meanwhile some Al–O bonds are formed. Figure 5(b) demonstrates that the O 1s core–level spectrum is a coupling of two components corresponding to the Al–O and the Ga–O bonds. After IST, both intensity of Al–O and Ga–O bonds were elevated as well, illustrating that Al–N and Ga–N bonds on the surface are broken while some Al–O and Ga–O bonds are formed. Compared sample A, the significant enhancement of Al–O peak makes the core–level spectra of O 1s drift towards the Al–O peak with lower bond energy for sample B. These results are consistent with the corresponding spectral peaks of $Al_2O_3$ prepared by physical vapor deposition method.[27] The IST process generates corresponding oxides, so as to improve the Schottky barrier height.[28,29] Therefore, the barrier height of the device with IST is higher than that of the device without IST. Moreover, it is found that the decrease of gate leakage current is related to the oxidation of the barrier layer, as figure 3(c) shows.

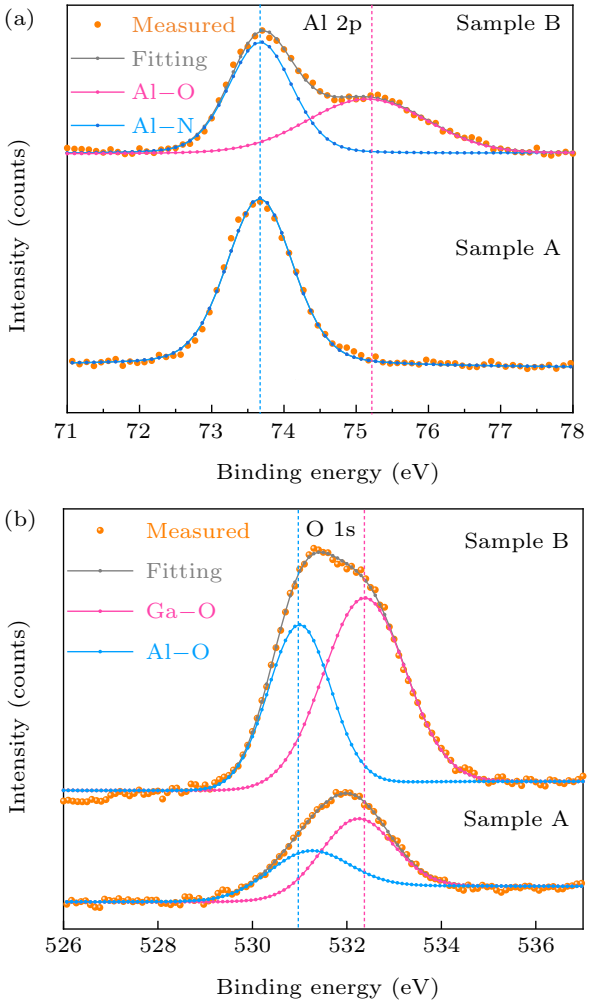



**Fig. 5.** XPS spectra from (a) Al 2p and (b) O 1s core levels of AlGaN surface with and without IST.

Figure 6 shows the pulse transfer characteristics of two types of HEMTs at a gate voltage of $-6$ V $\sim$ 2 V and the current collapse ratio can be expressed by the following expression:

$$\Delta I = \Delta I_{ds}/I_{ds0}, \tag{2}$$

where $\Delta I_{ds}$ is the variation of pulse drain current at $V_g = 2$ V before and after electrical stress, and $I_{ds0}$ is the pulse drain current at $V_g = 2$ V before applying electric stress.

**Table 2.** Comparison of pulse current collapse ratio of HEMTs with and without IST at ($V_{GSQ}$, $V_{DSQ}$ = −4 V, 0 V) and ($V_{GSQ}$, $V_{DSQ}$ = −8 V, 0 V).

| | Sample A | Sample B |
|---|---|---|
| ($V_{GSQ}$, $V_{DSQ}$ = −4 V, 0 V) | 1.9% | 0.4% |
| ($V_{GSQ}$, $V_{DSQ}$ = −8 V, 0 V) | 4.9% | 1.8% |

As the Table 2 shows, sample A shows current collapse ratios of 1.9% and 4.9% at gate quiescent voltages of −4 V and −8 V, respectively. Sample B shows current collapse ratios of 0.4% and 1.8%. This indicates that IST has a certain inhibition effect on current collapse. What is more, the HEMTs without IST exhibited a forward floating of $V_{th}$ by 0.18 V, while that for the ones with IST is only 0.06 V. The drift of $V_{th}$ may be due to the damage induced trap introduced in the process of recess gate etching, which has the ability to capture electrons.[30]

As demonstrated in Fig. 7, the current–gain cutoff frequency $f_T$ and maximum oscillation frequency $f_{max}$ of the two types of HEMTs were measured using network analyzer in a frequency ranging from 100 MHz to 40 GHz. The HEMTs with IST process deliver an $f_T$ of 22.4 GHz and an $f_{max}$ of 47.5 GHz (as shown in Fig. 7(b)), resulting in a high $f_T \times L_g$ of 13.4 GHz·μm. While the HEMTs without IST show an $f_T$ of 18.0 GHz and an $f_{max}$ of 38.8 GHz (as shown in Fig. 7(a)). As shown in Fig. 6, the IST process reduces the drift of threshold voltage, which shows its advantage in reducing the interface charge induced by trap. Because IST process could effectively reduce the interface charge, reduced the parasitic effect of the device, and then reduced the effective gate length of the device.[31] Therefore, the small signal characteristics of the device are improved.

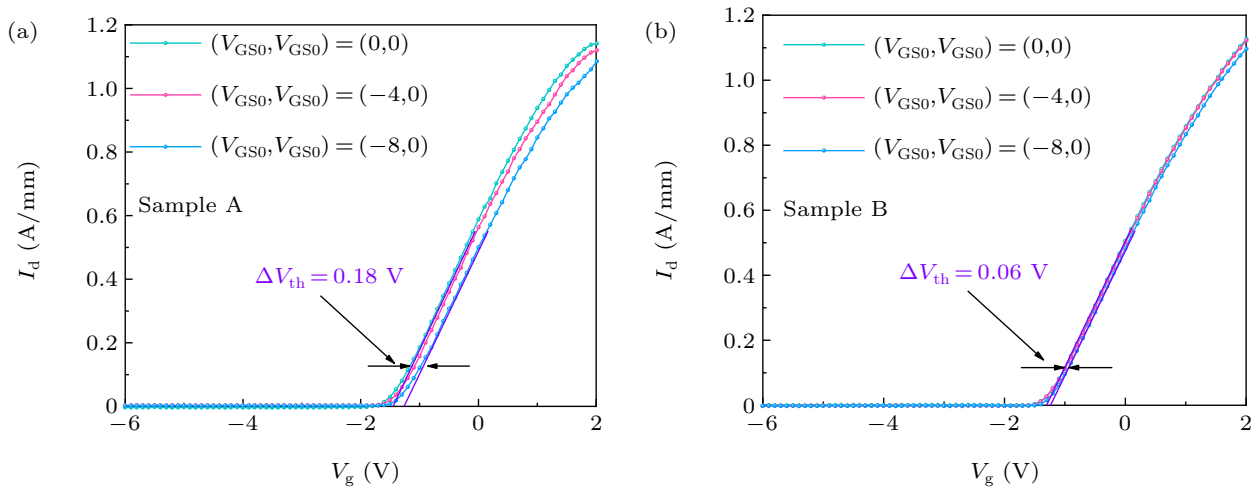



**Fig. 6.** Pulsed *I*–*V* characteristics of HEMTs with (a) no IST and (b) IST at a drain voltage of 10 V for ($V_{GSQ}$, $V_{DSQ}$ = 0 V, 0 V), ($V_{GSQ}$, $V_{DSQ}$ = −4 V, 0 V), and ($V_{GSQ}$, $V_{DSQ}$ = −8 V, 0 V).

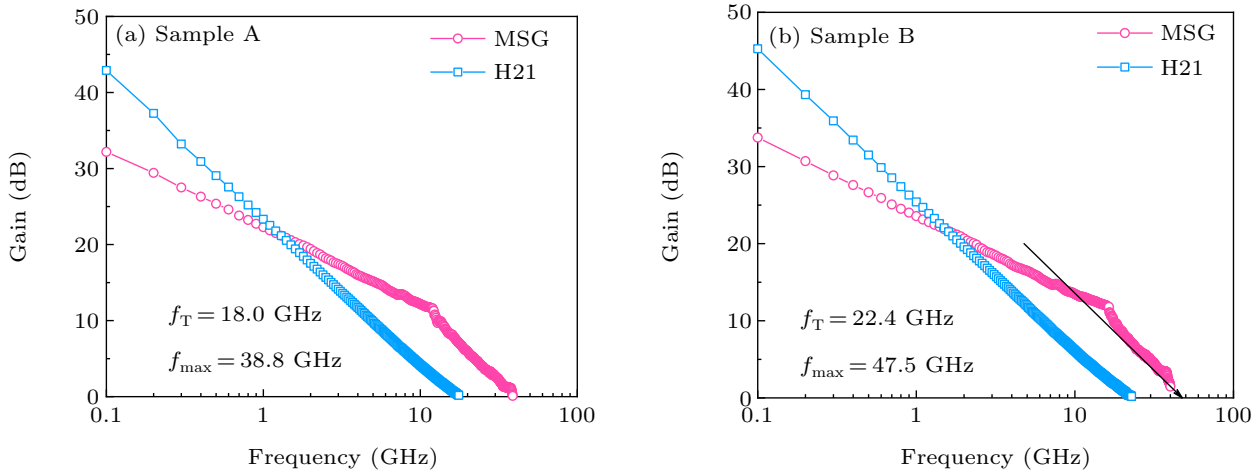



**Fig. 7.** Small-signal characteristics of the fabricated HEMTs at $V_{DS}$ = 10 V for the HEMTs (a) without and (b) with IST.

## 4. Conclusion

In conclusion, we proposed a method to reduce gate leakage of devices and investigated the effect of different processing time of IST on the surface of barrier layer under gate metal. The fabricated HEMTs with the IST process show a low reverse gate current of $10^{-9}$ A/mm, high on/off current ratio of $3.6 \times 10^8$, and high $f_T \times L_g$ of 13.44 GHz · μm. Energy

spectrum analysis of XPS shows the surface of AlGaN barrier layer is transformed into gallium oxide and alumina oxide, which proved by the cross-sectional TEM. These excellent results depict the great potential of the IST process applied for high frequency and high power operation. Especially, for RF devices with small gate length used in millimeter wave band, IST process can reduce the gate length extension of the device and significantly improve the high-frequency characteristics of the device and promote the development of RF devices.

## Acknowledgments

Project supported by the National Key Research and Development Program of China (Grant No. 2018YFB1802100), the National Natural Science Foundation of China (Grant Nos. 62104184, 62090014, 62104178, and 62104179), the Fundamental Research Funds for the Central Universities of China (Grant Nos. XJS201102, XJS211101, XJS211106, and ZDRC2002), and the Natural Science Foundation of Shaanxi Province, China (Grant Nos. 2020JM-191 and 2018HJCG-20).

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