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Citation: Chin. Phys. B, 2022, 31 (**5**): 058502. DOI: 10.1088/1674-1056/ac464f
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Impact of gate offset in gate recess on DC and RF performance of InAlAs/InGaAs InP-based HEMTs

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(Received 8 November 2021; revised manuscript received 8 November 2021; accepted manuscript online 24 December 2021)

A set of 100-nm gate-length InP-based high electron mobility transistors (HEMTs) were designed and fabricated with different gate offsets in gate recess. A novel technology was proposed for independent definition of gate recess and T-shaped gate by electron beam lithography. DC and RF measurement was conducted. With the gate offset varying from drain side to source side, the maximum drain current ($I_{ds,max}$) and transconductance ($g_{m,max}$) increased. In the meantime, f_T decreased while f_{max} increased, and the highest f_{max} of 1096 GHz was obtained. It can be explained by the increase of gate–source capacitance and the decrease of gate–drain capacitance and source resistance. Output conductance was also suppressed by gate offset toward source side. This provides simple and flexible device parameter selection for HEMTs of different usages.

Keywords: InP HEMT, InGaAs/InAlAs, cut-off frequency (f_T), maximum oscillation frequency (f_{max}), asymmetric gate recess

PACS: 85.30.Tv, 73.40.Qv, 85.30.–z **DOI:** 10.1088/1674-1056/ac464f

1. Introduction

Due to high frequency, high gain, low power consumption, and low noise performance, InP-based high electron mobility transistors (HEMTs) are one of the most promising semiconductor devices for millimeter-wave and terahertz monolithic integrated circuits.[1–5] The excellent performance is attributed to high carrier density, high electron velocity, and low gate leakage current. A cutoff frequency (f_T) of over 700 GHz using 25-nm gate was reported in InP-based HEMTs[6]. A maximum oscillation frequency (f_{max}) of 1.5 THz and a terahertz IC operating at 1 THz using 25-nm gate InP-based HEMTs were demonstrated.[7] The f_T and f_{max} of HEMTs were mainly improved by scaling down the gate length of devices.[8] On the other hand, it is of great significance to optimize parasitic effects in order to further improve performance.[9] By reducing the source-to-drain space, parasitic resistance was suppressed and RF performance was improved.[10,11] Modifying the gate recess is another effective way to improve high-frequency characteristics of InP-based HEMTs. The adoption of asymmetric gate recess was proved helpful to improve f_{max}.[12,13] On this basis, we would like to further investigate the impacts of asymmetric gate recess by varying the gate location in the recess.

In this paper, we will report on how the gate offset in gate recess impacts the DC and RF characteristics of InP-based HEMTs instead of a gate scaling down that is often used to obtain high performance. We designed and fabricated a set of devices, of which the gate location was varying in the recess. Therefore, various forms of asymmetric gate recess were realized. A fixed source-to-drain space was maintained at 2.4 μm for the same periphery conditions. The gate was located at the recess center, with an offset toward source or drain side to form the whole gate structure. The gate recess length L_{recess} is expressed as $L_{rs}+L_g+L_{rd}$, where L_{rs} is the source-side recess length, L_g is the gate length, and L_{rd} is the drain-side recess length. It is easy to adjust the gate location through one step EBL after the recess is defined and form the asymmetry of gate recess. To draw a general conclusion, gate recesses were defined with three lengths, which were 0.4 μm, 0.6 μm, and 0.8 μm respectively. It was found that the gate away from drain side was effective in decreasing parasitic source resistance, output conductance and gate-to-drain capacitance, and hence improved transconductance and f_{max} even though an increase of C_{gs} is not ideal for a high f_T.

2. Device fabrication

Figure 1 shows the cross-section schematic diagram of the device with a gate offset toward source side. Epitaxial layer structures of InP-based HEMTs were grown on a 3-inch (1 inch = 2.54 cm) semi-insulating InP (100) substrate by gas source molecular beam epitaxy (GSMBE). The layers, from bottom to top, were composed of a 500-nm $In_{0.52}Al_{0.48}As$

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buffer layer, a 15-nm lattice matched $In_{0.52}Ga_{0.48}As$ channel layer, a 3-nm $In_{0.52}Al_{0.48}As$ spacer layer, an Si planar doping with a sheet carrier density of 5×10^{12} cm^{-2}, an 8-nm $In_{0.52}Al_{0.48}As$ Schottky barrier layer, a 4-nm InP etch-stop layer, and a 15-nm/15-nm/10-nm heavily Si-doped $In_{0.52}Ga_{0.48}As/In_{0.53}Ga_{0.48}As/In_{0.65}Ga_{0.35}As$ composite cap layer with a concentration of 1×10^{19} cm^{-3}/1×10^{19} cm^{-3}/3×10^{19} cm^{-3}. Hall measurement was carried out at room temperature. The two-dimensional electron gas (2DEG) carrier mobility was 12000 cm^2/(V·s).

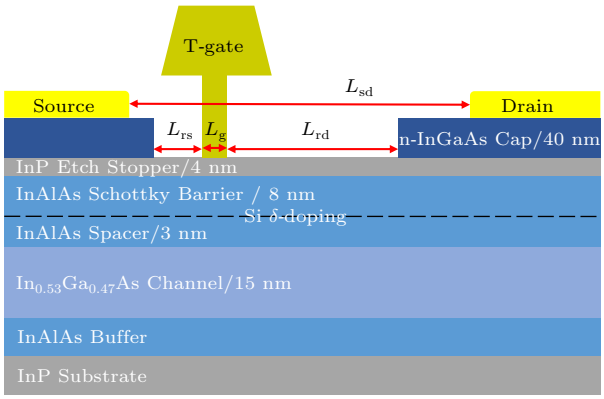


Fig. 1. Cross-section schematic diagram of the InP-based HEMT with a gate offset toward source.

The fabrication process of InP-based HEMTs consisted of four main steps, namely mesa isolation, Ohmic contact formation, gate recess, and T-shaped gate process, which was similar to our previously reported devices.[14] At first isolated mesa was formed to define the area of a device by means of phosphorus acid based wet chemical etching down to buffer layer. Then source and drain were defined by lithography with a 2.4-μm space in between. Ohmic contacts were formed using electron beam evaporated Ti/Pt/Au (15 nm/15 nm/50 nm) without annealing. The ohmic contact resistivity was measured to be 0.023 Ω·mm and the specific contact resistivity to be 8.75×10^{-8} Ω·cm^2 by transmission line method (TLM).[15] Afterward, SiO_2 was deposited by PECVD, which served as a hard mask for gate recess and improved adherence of photoresist. A novel gate recess process was proposed, where the gate recess was defined by electron beam lithography with a ZEP520A e-beam resist independently of the gate electrode. SiO_2 mask was etched by reactive ion etching (RIE). For extending investigation, the gate recesses were designed with three different lengths, which were 0.4 μm, 0.6 μm, and 0.8 μm respectively. The gate recess, as a whole, was closer to the source side in order to achieve a higher breakdown voltage. This was followed by T-shaped gate lithography. The gate was defined by EBL with a ZEP/PMGI/ZEP (200 nm/500 nm/200 nm) tri-layer e-beam resist. Here the gate could be located at the recess center, or with an offset toward source/drain, which corresponded to the variation of L_{rs} and L_{rd}. After pattern definition, wet chemical etching was used to form the gate recess and Ti/Pt/Au (3 nm/15 nm/300 nm) stack layers were evaporated and lifted off to form the T-shaped gate in sequence. Finally the SiO_2 hard mask was removed, the devices were passivated by a 20-nm SiN_x layer, and Ti/Au (15 nm/30 nm) connection pads were evaporated for on-wafer characterization. The SEM images of the devices are shown in Fig. 2.

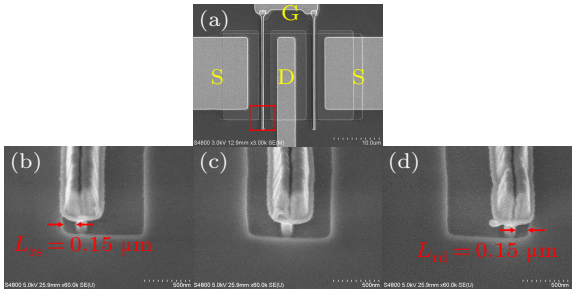


Fig. 2. SEM images of InP HEMTs with gate offsets in gate recess: (a) top view of InP HEMT; (b) gate offset toward source; (c) gate in the middle of recess; (d) gate offset toward drain.

3. Result and discussion

In a narrow recess the absolute value of gate offset was relatively small while in a wider recess the offset was larger. The offsets from recess center were ±0.05 μm, ±0.15 μm, and ±0.25 μm for recess lengths of 0.4 μm, 0.6 μm, and 0.8 μm, respectively. In this case, L_{rs} was kept at 0.15 μm for gate offset toward source and L_{rd} was kept at 0.15 μm for gate offset toward drain. The values of gate offsets were normalized as −1, 0, and 1 to represent the offset toward source, in the middle, and toward drain, respectively.

3.1. DC characteristics

On-wafer DC measurement was carried out by a HP4155A semiconductor parameter analyzer at room temperature. The gate–source voltage (V_{gs}) was swept from −1.0 V to 0.2 V at a step of +0.1 V, and the drain–source voltage (V_{ds}) was from 0 V to 1.5 V. The threshold voltage was about −0.6 V. These devices exhibited a maximum saturated drain current $I_{ds,max}$ of 763.9 mA/mm at $V_{GS} = 0.2$ V and $V_{gs} = 1.5$ V, which was achieved in a device of 0.4-μm recess length. The maximum extrinsic transconductance, $g_{m,max}$, was high up to 1120 mS/mm at $V_{GS} = -0.25$ V.

Devices with a wider gate recess, where the absolute gate offset was larger, indicated clear changes of I_{ds} and g_m. When L_{rs} decreased, namely gate location shifted from drain side to source side, both $I_{ds,max}$ and $g_{m,max}$ increased. Figure 3 plots the I_{ds}–V_{ds} curves of 0.8-μm-recess devices with different gate offsets, and the $I_{ds,max}$ increased by over 15% from 541 mA/mm to 621 mA/mm. Another benefit could be found that a longer L_{rd} lead to effective suppression of impact ionization when a large V_{ds} was applied. For $V_{gs} = -0.4$ V, the drain current of positive-offset device exceeded that of zero-offset device at V_{ds} over 1.2 V, illustrating a weaker impact

ionization in longer distance between gate and drain. Besides, $g_{m,max}$ increased by 17% from 864 mA/mm to 1016 mA/mm, as is shown in Fig. 4. Extrinsic transconductance g_m can be expressed as

$$g_m = \frac{g_{mi}}{1 + g_{mi}R_s}, \tag{1}$$

where g_{mi} is the intrinsic transconductance removing the influence of parasitic parameters, and R_s is the parasitic source resistance. Since recess resistance R_{recess} is 2.3 times larger than that of cap layer R_{cap},[12] a smaller L_{rs} in the access region between gate and source led to a smaller R_s that improved extrinsic transconductance. The voltage drop on R_s was reduced, and consequently more proportion of V_{gs} dropped on the Schottky barrier capacitor for gate control.

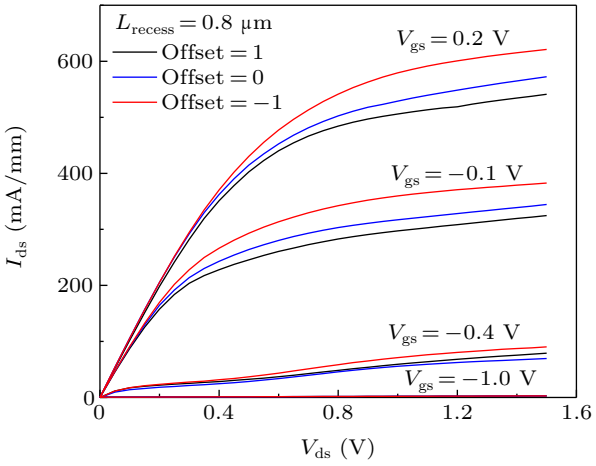


Fig. 3. Output characteristics of 0.8-μm-recess HEMTs.

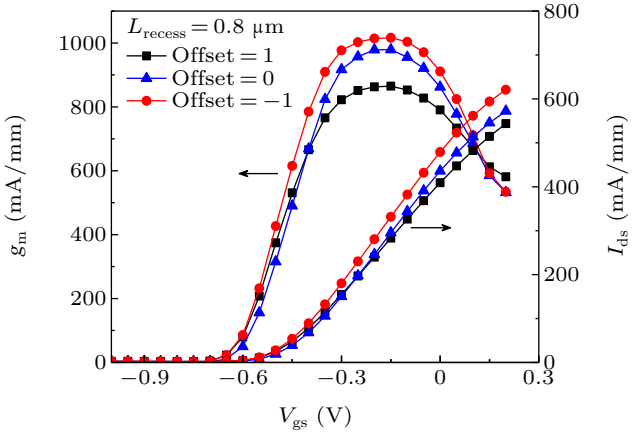


Fig. 4. Transfer characteristics of 0.8-μm-recess HEMTs.

Moreover, for all devices of different gate recess lengths, g_m showed a maximum value when gate was located with an offset toward source. And the corresponding I_{ds} tend to be a larger value due to better gate control.

3.2. RF characteristics

RF characteristics were measured on wafer by Agilent E8363B PNA vector network analyzer from 0.1 GHz to 40 GHz at a step of 0.1 GHz. Open-short patterns were fabricated on the same wafer for S parameter deembedding of connection pads. f_T was obtained by extrapolating H_{21} curve to unit gain by a slope of −20 dB/decade. Moreover, due to the noisy characteristics of unilateral gain (U) which indicated insufficient estimation of f_{max} variation, MAG/MSG was used to extrapolate f_{max},[13–16] as is shown in Fig. 5. Since f_T and f_{max} had a positive correlation with g_{mi}, V_{ds} and V_{gs} were biased at 1.5 V and −0.2 V, respectively, which were associated with the maximum g_{mi} in our devices. As can be seen in Fig. 6, f_{max} ranged from 374 GHz to 584 GHz while f_T ranged from 167 GHz to 225 GHz, and there was a trade-off between the two parameters. The highest f_T was obtained from the positive gate-offset device with 0.4-μm gate recess while the highest f_{max} was obtained from the negative gate-offset device with 0.8-μm gate recess.

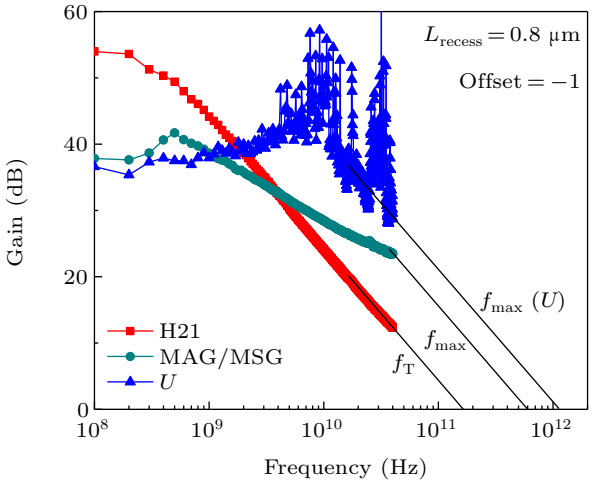


Fig. 5. Extrapolation of f_T and f_{max} from measured data.

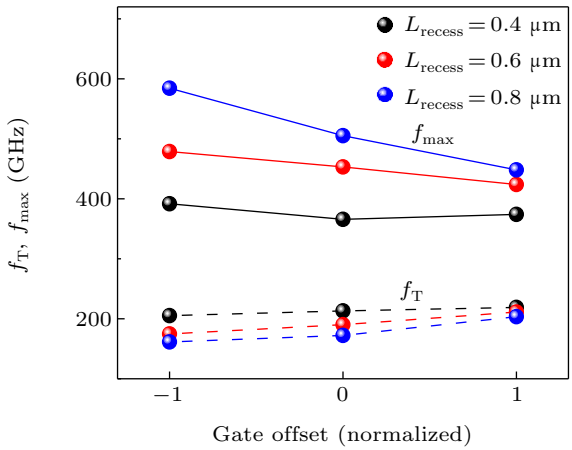


Fig. 6. f_T and f_{max} of HEMTs with gate offsets in gate recess (solid: f_{max}, dashed: f_T).

The results were similar for devices with three different gate recess lengths. When the normalized gate offset varied from 1 to −1, which literally meant that the gate location moved from drain side to source side, f_T decreased, and f_{max} increased. It can be seen from Fig. 6 that in wide recesses, the ratio of f_T and f_{max} change became more obvious. f_T and f_{max} can be expressed as

$$f_{\mathrm{T,int}} = \frac{g_{\mathrm{mi}}}{2\pi\left(C_{\mathrm{gs}}+C_{\mathrm{gd}}\right)}, \tag{2}$$

$$f_{\mathrm{T}} = \frac{g_{\mathrm{mi}}}{2\pi\left(C_{\mathrm{gs}}+C_{\mathrm{gd}}\right)\left[1+g_{\mathrm{ds}}\left(R_{\mathrm{s}}+R_{\mathrm{d}}\right)\right]+C_{\mathrm{gd}}\cdot g_{\mathrm{mi}}\left(R_{\mathrm{s}}+R_{\mathrm{d}}\right)}, \tag{3}$$

$$f_{\mathrm{max}} = \frac{f_{\mathrm{T,int}}}{\sqrt{4g_{\mathrm{ds}}\left(R_{\mathrm{g}}+R_{\mathrm{s}}+R_{\mathrm{i}}\right)+\dfrac{2C_{\mathrm{gd}}}{C_{\mathrm{gs}}}\left(\dfrac{2C_{\mathrm{gd}}}{C_{\mathrm{gs}}}+g_{\mathrm{mi}}\left(R_{\mathrm{s}}+R_{\mathrm{i}}\right)\right)}}, \tag{4}$$

where g_{mi} is the intrinsic transconductance, C_{gs} is the gate–source capacitance, C_{gd} is the gate–drain capacitance, g_{ds} is the output conductance, R_{s} is the source resistance, R_{d} is the drain resistance, R_{g} is the gate resistance, and R_{i} is the intrinsic resistance in the channel region.[16] $f_{\mathrm{T,int}}$ represents the cut-off frequency of the intrinsic part of HEMTs without parasitic resistance and capacitance. Parameters of the small-signal equivalent circuit model were extracted and compared based on Rorsman's method[17] and our previous research.[18–20] Figure 7 illustrates the changes in key parameters, and Table 1 lists some related small-signal model parameters of 0.8-μm-recess devices. The small-signal model was then simulated with extracted parameter values. Figure 8 shows a good fitting result of our small-signal model compared with the measured data after de-embedding, which indicated effectiveness and accuracy of our extracted parameters.

Table 1. Parameters of small-signal model for InP HEMTs of 0.8-μm gate recess.

Gate offset (μm)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	g_{ds} (mS)	R_{s} (Ω)	R_{d} (Ω)	R_{g} (Ω)	g_{mi} (mS)	f_{T} (GHz)	f_{max} (GHz)	f_{max} (U) (GHz)
+0.25	76.70	4.448	16.68	4	1.98	4	5.78	116	213	392	642
0	99.52	2.664	16.19	2	1.75	5.2	5.78	116	181	479	825
−0.25	114.80	1.901	16.48	1	1.6	6	5.78	118	167	584	1096

Table 2. Benchmarks of f_{max} in InGaAs/InAlAs HEMTs.

Ref.	L_{g} (nm)	Channel/substrate	$g_{\mathrm{m,max}}$ (mS/mm) (V_{ds} (V))	f_{T} (GHz) (V_{ds} (V))	f_{max} (GHz) (V_{ds} (V))
[13]	75	$In_{0.7}Ga_{0.3}As/InP$	1950 (1.0)	270 (1.0)	910 (1.0)
[21]	50	$In_{0.7}Ga_{0.3}As/InP$	1700 (0.5)	470 (0.75)	1080 (0.75)
[22]	35	InAs/InP	2300 (1.0)	385 (0.8)	1200 (0.8)
[23]	25	InAs/InP	3050 (1.0)	610 (1.2)	1500 (1.2)
[24]	20	InAs/GaAs	2850 (1.0)	320 (1.0)	1130 (1.0)
This work	100	$In_{0.52}Ga_{0.48}As/InP$	1120 (1.5)	167 (1.5)	1096 (1.5)

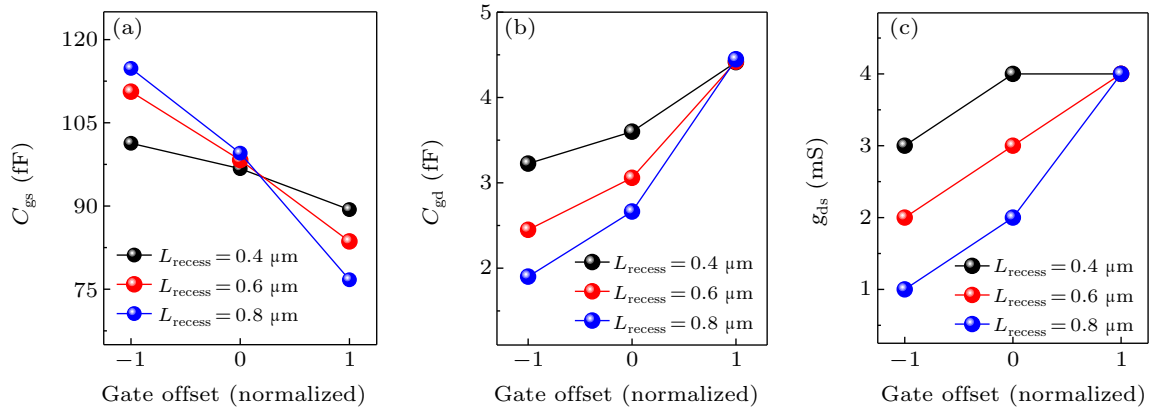


Fig. 7. Extracted small-signal parameters of HEMTs with different gate offsets: (a) gate–source capacitance; (b) gate–drain capacitance; (c) output conductance.

For a given gate recess, where $L_{\mathrm{rs}}+L_{\mathrm{rd}}$ was a constant, the variation of gate offset from drain side to source side meant a smaller L_{rs} and a larger L_{rd}. C_{gs} and C_{gd} which were related to the corresponding space consequently changed, resulting in C_{gs} increase and C_{gd} decrease. The g_{ds} decrease was also attributed to the extension of L_{rd}.[13] Here the electric field between gate and drain was smoothed, and thus impact ionization in the channel was suppressed. This was consistent with the phenomenon observed in DC measurement.

Although C_{gs} and C_{gd} changed in a contrary way, the absolute value of C_{gs} was still much larger than that of C_{gd}. As a result, $C_{\mathrm{gs}}+C_{\mathrm{gd}}$ in total increased, contributing to the decrease of f_{T}. As for f_{max}, although it was proportional to f_{T}, $C_{\mathrm{gd}}/C_{\mathrm{gs}}$ further decreased due to the contrary change, leading

to the reduction in the denominator of the f_{max} formula by a greater ratio. Moreover, according to Eq. (4), the reduction of g_{ds} and R_s was helpful in increasing f_{max} as well. As is plotted in Fig. 5, a high f_{max} of approximately 1.1 THz was achieved from extrapolation of Mason's unilateral gain, U, to 0 dB when a V_{gs} of −0.2 V and a V_{ds} of 1.5 V were applied to the HEMT.

Table 2 shows the benchmarks of f_{max} in published papers.[13,21–24] In some cases, f_{max} exceeding 1 THz was obtained by scaling L_g to less than 50 nm. Meanwhile, the InP-based HEMT reported in this paper reached a f_{max} of approximately 1.1 THz although L_g was relatively large at 100 nm.

In a multi-function MMIC, devices of various performance are needed. For instance, an analog module requires high f_T while a power amplifier requires high f_{max}. Thus, the device requirements can be satisfied by simply adjusting the gate location in gate recess. Furthermore, by adding the modification of gate recess length, various transistor performances are available over a larger range.

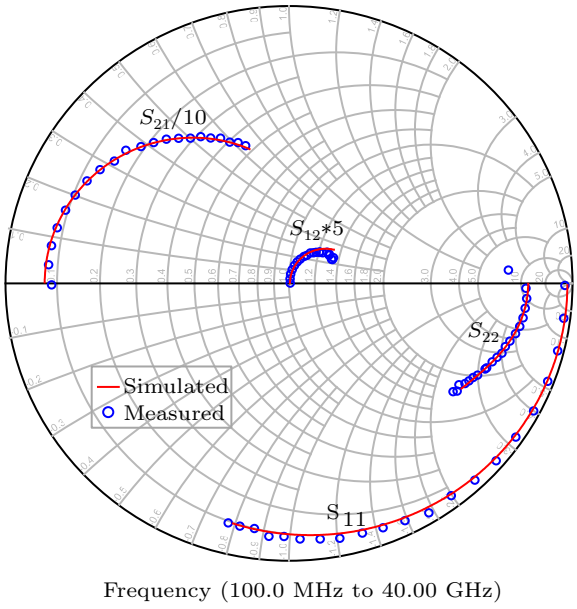


Fig. 8. Small-signal model *versus* de-embedded *S* parameters of InP-based HEMTs (red line: small-signal model; blue dot: de-embedded measured *S* parameters).

4. Conclusion

In this paper, we investigated a set of 100-nm InP-based HEMTs with gate offsets in the gate recess. A novel technology was proposed for independent definition of gate recess and T-shaped gate. As a result, a maximum I_{ds} of 769 mA/mm and g_m of 1120 mS/mm were obtained. When the gate offset varied from toward drain side to toward source side, I_{ds} and g_m increased. The reduction of R_s improved extrinsic transconductance and decreased the voltage drop split from V_{gs}. In the meantime, f_T decreased while f_{max} increased. A f_{max} of 1096 GHz was obtained in a 0.8-μm-recess HEMT with a gate offset toward source side. This was attributed to the increase of C_{gs}, along with the reduction of C_{gd}, g_{ds}, and R_s. This work provides simple and flexible device parameter selection for HEMTs of different usage over a large frequency range.

Acknowledgment

Project supported by the National Nature Science Foundation of China (Grant No. 61434006).

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