


# DC and analog/RF performance of C-shaped pocket TFET (CSP-TFET) with fully overlapping gate

Zi-Xin Chen(陈子馨), Wei-Jing Liu(刘伟景), Jiang-Nan Liu(刘江南), Qiu-Hui Wang(王秋蕙), Xu-Guo Zhang(章徐国), Jie Xu(许洁), Qing-Hua Li(李清华), Wei Bai(白伟), and Xiao-Dong Tang(唐晓东)

**Citation:**Chin. Phys. B, 2022, 31 (**5**): 058501. DOI: 10.1088/1674-1056/ac43a6
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

**What follows is a list of articles you may be interested in**

---

## Impact of oxygen in electrical properties and hot-carrier stress-induced degradation of GaN high electron mobility transistors

Lixiang Chen(陈丽香), Min Ma(马敏), Jiecheng Cao(曹杰程), Jiawei Sun(孙佳惟), Miaoling Que(阙妙玲), and Yunfei Sun(孙云飞)

Chin. Phys. B, 2021, 30 (**10**): 108502. DOI: 10.1088/1674-1056/ac1efd

## Design and investigation of dopingless double-gate line tunneling transistor: Analog performance, linearity, and harmonic distortion analysis

Hui-Fang Xu(许会芳)†, Xin-Feng Han(韩新风), and Wen Sun(孙雯)

Chin. Phys. B, 2020, 29 (**10**): 108502. DOI: 10.1088/1674-1056/ab9c06

## Double-gate-all-around tunnel field-effect transistor

Wen-Hao Zhang(张文豪), Zun-Chao Li(李尊朝), Yun-He Guan(关云鹤), Ye-Fei Zhang(张也非)

Chin. Phys. B, 2017, 26 (**7**): 078502. DOI: 10.1088/1674-1056/26/7/078502

## Heteromaterial-gate line tunnel field-effect transistor based on Si/Ge heterojunction

Shuqin Zhang(张书琴), Renrong Liang(梁仁荣), Jing Wang(王敬), Zhen Tan(谭桢), Jun Xu(许军)

Chin. Phys. B, 2017, 26 (**1**): 018504. DOI: 10.1088/1674-1056/26/1/018504

## Analytical threshold voltage model for strained silicon GAA-TFET

Hai-Yan Kang(康海燕), Hui-Yong Hu(胡辉勇), Bin Wang(王斌)

Chin. Phys. B, 2016, 25 (**11**): 118501. DOI: 10.1088/1674-1056/25/11/118501

---

# DC and analog/RF performance of C-shaped pocket TFET (CSP-TFET) with fully overlapping gate

Zi-Xin Chen(陈子馨)[1], Wei-Jing Liu(刘伟景)[1,†], Jiang-Nan Liu(刘江南)[1], Qiu-Hui Wang(王秋蕙)[1], Xu-Guo Zhang(章徐国)[1], Jie Xu(许洁)[1], Qing-Hua Li(李清华)[2], Wei Bai(白伟)[3], and Xiao-Dong Tang(唐晓东)[3]

[1] *College of Electronics and Information Engineering, Shanghai University of Electric Power, Shanghai* 200090, *China*
[2] *GTA Semiconductor Corporation Limited, Shanghai* 200123, *China*
[3] *Key Laboratory of Polar Materials and Devices, East China Normal University, Shanghai* 200041, *China*

(Received 1 November 2021; revised manuscript received 27 November 2021; accepted manuscript online 16 December 2021)

A C-shaped pocket tunnel field effect transistor (CSP-TFET) has been designed and optimized based on the traditional double-gate TFETs by introducing a C-shaped pocket region between the source and channel to improve the device performance. A gate-to-pocket overlapping structure is also examined in the proposed CSP-TFET to enhance the gate controllability. The effects of the pocket length, pocket doping concentration and gate-to-pocket overlapping structure on the DC and analog/RF characteristics of the CSP-TFET are estimated after calibrating the tunneling model in double-gate TFETs. The DC and analog/RF performance such as on-state current ($I_{on}$), on/off current ratio ($I_{on}/I_{off}$), subthreshold swing (*SS*) transconductance ($g_m$), cut-off frequency ($f_T$) and gain–bandwidth product (GBP) are investigated. The optimized CSPTFET device exhibits excellent performance with high $I_{on}$ ($9.98\times10^{-4}$ A/μm), high $I_{on}/I_{off}$ ($\sim 10^{11}$), as well as low *SS* ($\sim$ 12 mV/dec). The results reveal that the CSP-TFET device could be a potential alternative for the next generation of semiconductor devices.

**Keywords:** tunnel field effect transistor, double gate, pocket

**PACS:** 85.30.Mn, 85.30.Tv, 81.05.Cy **DOI:** 10.1088/1674-1056/ac43a6

## 1. Introduction

As the feature size of metal oxide semiconductor field effect transistors (MOSFETs) continues to decrease, the supply voltage ($V_{DD}$) scaling of MOSFETs will be quite slow. With the increasing reduction of technology nodes, the lack of $V_{DD}$ scaling has recently led to power consumption problems because MOSFETs are approaching to their minimum $V_{DD}$ determined by the operating mechanism. Thus, higher device power consumption will become a major constraint on the transistor performance. To meet the demand for low-power circuits in the era of big data, many researchers have proposed a variety of ultra-steep subthreshold swing devices based on novel operating mechanisms, including piezoelectric field-effect transistors (piezo-FETs), negative capacitance field-effect transistors (NC-FETs), and tunneling field-effect transistors (TFETs). TFETs are emerging as a promising candidate for ultra-low power applications due to their advantages of low leakage currents, low temperature dependence, and low sub-threshold swings, which can be achieved beyond the 60 mV/dec limit of MOSFETs at room temperature.[2–9] However, the drawbacks of TFETs are low on-state current and the occurrence of ambipolar current. Many researchers addressed these problems by means of modifying the device structure, such as the use of dual-gate TFETs,[2,10] gate-all-around TFETs,[11,12] L-shaped gate TFETs[13,14] and gate–source/drain overlapping,[15,16] or adopting different kinds of materials such as hetero-gate dielectric,[17–19] III–IV materials[20–22] and hetero-material gate.[23,24] The low on-current of the silicon-based TFETs are an inherent difficulty in Si due to the indirect bandgap and low tunneling effective mass.[25] In order to achieve a higher on-state current of the silicon-based TFETs, the source-pocket TFET (PNPN-TFET)[26–30] has recently been proposed, which features a heavily doped N pocket added on the source side, leading to enhanced on-state currents,[26] improved on/off current ratios and steep subthreshold swings compared with the conventional PIN-TFETs. Different structures and materials of pocket in PNPN-TFETs have been explored: (1) vertical pocket inserted between the source and channel based on the fully depleted pocket region, which results in reducing the tunneling width and then enhancing the lateral electric field at the tunneling junction;[26,27,30] (2) horizontal pocket added on the source side based on the line tunneling-based structures;[29,31] (3) the use of SiGe pocket materials[32,35] due to its VLSI compatibility and tunable bandgap. In addition, a gate-to-pocket overlapping structure has been demonstrated as a new way to enhance the BTBT generation rate and thus to improve the tunneling current.[33] However, the silicon-based TFETs still require further improvements in terms of $I_{on}$ and subthreshold swing (*SS*) for ultra-low power applications.

In this work, the silicon-based double-gate PNPN-TFET with symmetrical horizontal pocket and gate-to-pocket overlapping structure — silicon-based C-shaped pocket TFET (CSP-TFET) has been proposed to further improve the on-

†Corresponding author. E-mail: liuwj5500@163.com

© 2022 Chinese Physical Society and IOP Publishing Ltd 

state current and subthreshold swing. The effect of the physical dimensional parameters and the doping concentration of the pocket on the DC and analog/RF performance of the CSP-TFET device are analyzed in detail. The experimental details will be explored in the following sections. Section 2 describes the basic structure, parameters, simulation models, and calibration experiments of the proposed device. Section 3 discusses the characteristics of the structure and the optimization process, and then Section 4 summarizes the article with relevant notes.

## 2. Device structures, parameters, simulation details and calibration

The simulated CSP-TFET is schematically presented in Fig. 1, and the specific parameters of the device are shown in Table 1. The doping concentrations of the source, channel, and drain are $1\times10^{20}$ cm$^{-3}$ (for p-type), $1\times10^{17}$ cm$^{-3}$ (for p-type), and $5\times10^{18}$ cm$^{-3}$ (for n-type), respectively. All regions are assumed to be uniformly doped. The PNPN-TFETs are characteristically based on the conventional structure of silicon-based double-gate TFETs with a heavily N-doped pocket incorporated between the source and channel. The principle of the PNPN-TFET is to make the pocket region fully depleted under the applied voltage, increasing the electric field and thus enhancing the band-to-band tunneling rate between the source and channel, which leads to an increase in the on-state current. The proposed CSP-TFET device is based on the N-doped pocket region (region name: pocket 2) between the source and channel, with another pocket region (region name: pocket 1) added to the source. The pocket 1 is connected to the pocket 2. The N-doped pocket 1 and pocket 2 are collectively called the "pocket", and the entire pocket (including pocket 1 and pocket 2) looks like a "C" shape, as shown in Fig. 1. It is assumed that pocket 1 and pocket 2 are consistent in doping concentration. $SiO_2$ is used as the gate oxide layer with a thickness of 2 nm. The simulation parameters, such as the length of pocket 1 ($L_{p1}$), the length of pocket 2 ($L_{p2}$) and the pocket doping concentration ($N_p$), will be used as variables. Assuming that the pocket is fully covered by the gate. The work function $\varphi$ (of the gate) is set to be 4.5 eV. In addition to studying the effect of pocket length and doping concentration on the DC and analog/RF properties of the CSP-TFET device, the influence of the gate position of the CSP-TFET device is also investigated.

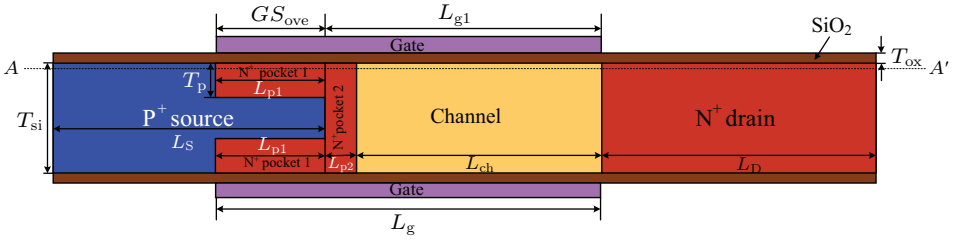



**Fig. 1.** The 2-D schematic view of CSP-TFET.

**Table 1.** Device parameters.

| Variable | Parameter | Simulation value |
|---|---|---|
| $T_{si}$ | silicon body thickness | 20 nm |
| $T_p$ | pocket 1 thickness | 2 nm |
| $L_{p1}$ | pocket 1 length | 2–30 nm |
| $L_{p2}$ | pocket 2 length | 1–10 nm |
| $L_S$ | source length | 50 nm |
| $L_D$ | drain length | 50 nm |
| $L_{ch}$ | channel length | 40–49 nm |
| $L_{g1}$ | gate 1 length | 50 nm |
| $N_{ch}$ | channel doping (n-type) | $1\times10^{17}$ cm$^{-3}$ |
| $N_s$ | source doping (p-type) | $1\times10^{20}$ cm$^{-3}$ |
| $N_d$ | drain doping (n-type) | $5\times10^{18}$ cm$^{-3}$ |
| $N_p$ | pocket doping (n-type) | $2\times10^{19}$–$1\times10^{20}$ cm$^{-3}$ |
| $\varphi$ | gate work function | 4.5 eV |
| $GS_{ove}$ | gate–pocket overlap | $L\times L_{p1}$ nm |
| $T_{ox}$ | gate oxide thickness | 2 nm |

The CSP-TFET is investigated by using Synopsys Sentaurus TCAD. The meshes need to be carefully defined to accurately extract data, especially for the interface between source and pocket and the interface between pocket and gate oxide layer. Since the source and drain of TFET are heavily doped, the Fermi–Dirac model and the bandgap narrowing model are employed. The doping-dependent mobility model, the carrier Shockley–Read–Hall (SRH) model, and the Auger model are also adopted. Since the silicon thickness ($T_{si}$) is 20 nm (larger than 7 nm), quantum effects are not considered in this simulation. The common band-to-band tunneling models include Schenk, Hurkx, the simple band-to-band tunneling model and the dynamic nonlocal path band-to-band tunneling (BTBT) model. The electric field and the carrier distribution at each point of the actual tunneling path are not constant. This paper employs the dynamic non-local BTBT model, which is the most versatile model and becomes a more flexible and convenient way to deal with arbitrarily shaped potential barriers. When using a nonlocal dynamic band-to-band tunneling model, the default values of the model parameters are inaccurate and need to be calibrated based on experimental results. The nonlocal BTBT model used in this paper is calibrated by using the work by Boucart and Ionescu.[1] The phonon-assisted factors ($A_{path1}=4.0\times10^{16}$ cm$^{-3}\cdot$s$^{-1}$ and $B_{path1}=1.9\times10^{7}$ MV$\cdot$cm$^{-1}$) are chosen for silicon materials

to achieve the best fitting results. The tunneling model used has been calibrated with the reported results.[1] The calibration of transfer characteristics is depicted in Fig. 2.

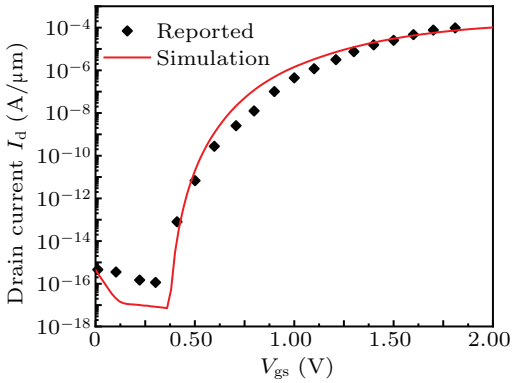



**Fig. 2.** Calibration of the TCAD model parameters obtained by comparing the simulated and experimental $I_{ds}$–$V_{gs}$ characteristics of Ref. [1].

## 3. Results and discussion

Pocket length, pocket doping concentration and gate position are discussed for better DC and analog/RF performance. The $I_{on}$, $I_{off}$, $I_{on}/I_{off}$, and $SS_{avg}$ are used as important indicators of the DC characteristics, and subsequently, the $g_m$, $f_T$, and GBP are used as those of the analog/RF characteristics. The drain voltage $V_d$ is set to be 1 V. The gate voltage $V_g$ varies from 0 to 2 V. The on-state current ($I_{on}$) and the off-state current ($I_{off}$) are defined by the drain currents ($I_d$) under $V_d = 1$ V with $V_g = 2$ V and $V_g = 0$ V.

### 3.1. Effect of $L_{p2}$ and $N_p$

Figure 3(a) shows the transfer characteristics with different value of $L_{p2}$ of the proposed CSP-TFET at a fixed pocket1 length ($L_{p1}$) of 2 nm and a pocket doping concentration ($N_p$) of $1\times10^{20}$ cm$^{-3}$. Note that in this work, the energy band diagrams are obtained at the location of 1 nm below the interface of silicon and gate oxide layer along the channel direction. As shown in Fig. 3(b) along the line $A$–$A'$ in Fig. 1, there is a local minimum in the conduction band $E_c$ of this device depicted in the locally enlarged picture due to the addition of pocket 2 between the source and channel, where the pocket 2 is either fully or partially depleted under the gate voltage.[17] It is observed from Fig. 3(a) that the drain currents of the device increase sharply and approach saturation at $L_{p2} > 2$ nm, and the on-state currents at $L_{p2} > 2$ nm are approximately 1.5 times higher than those at $L_{p2} \leq 2$ nm. This may be because the local minimum of the conduction band ($E_c$) in pocket 2 at $L_{p2} > 2$ nm has more energy band overlapping region with the valence band ($E_v$) in the source, resulting in more electron tunneling from the source into the channel as seen in Fig. 3(b). Moreover, Fig. 3(a) shows, without the gate voltage applied, the significant leakage currents were observed in the off state, which degrades severely to about $10^{-6}$ A/μm at $L_{p2} > 2$ nm, while the drain current at $L_{p2} \leq 2$ nm is less than $10^{-15}$ A/μm. The behavior of the drain currents of the CSP-TFET device in the off-state condition is illustrated by Fig. 3(c), where the conduction band in pocket 2 at $L_{p2} \leq 2$ nm lies above the valence band in the source in the absence of the gate voltage. The BTBT is suppressed, resulting in the device being in the off state. When $L_{p2}$ is greater than 2 nm, the conduction band of pocket 2 region is below the valence band of the source.

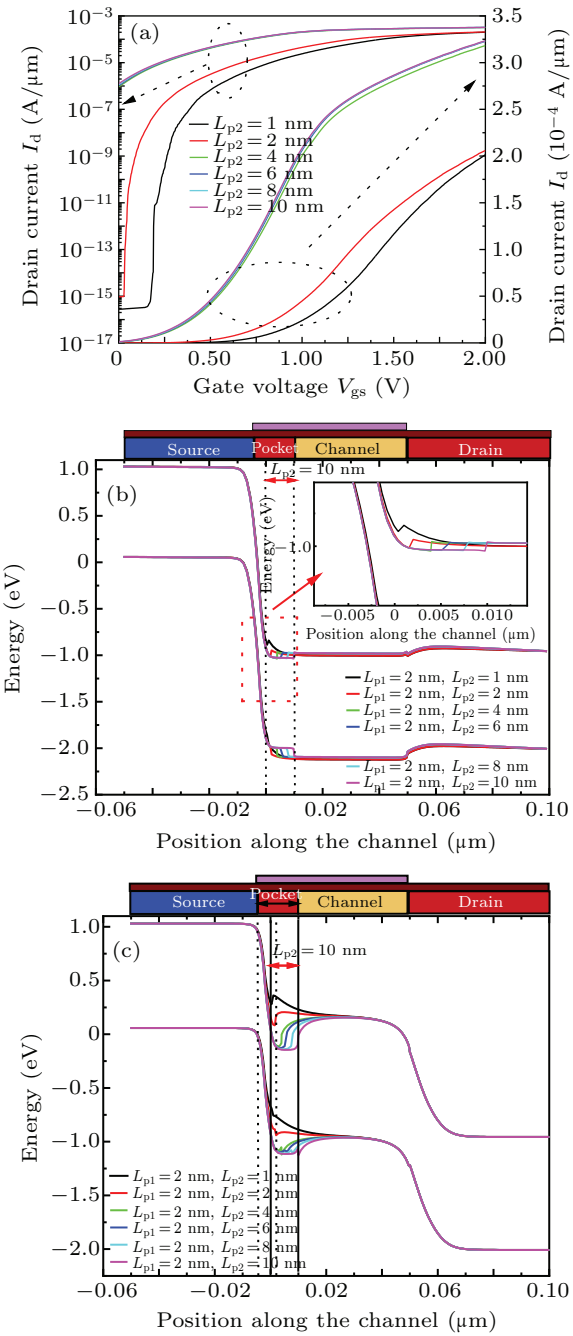



**Fig. 3.** (a) Effect of $L_{p2}$ on the transfer characteristics of the CSPTFET device at $L_{p1} = 2$ nm and $N_p = 1\times10^{20}$ cm$^{-3}$ (@$V_d = 1$ V, @$V_g = 2$ V), where the left $Y$-axis is the logarithmic curve and the right $Y$-axis is the linear curve. (b) Energy band diagram for $L_{p2}$ varying from 1 nm to 10 nm in the on-state at $L_{p1} = 2$ nm and $N_p = 1\times10^{20}$ cm$^{-3}$ (@$V_d = 1$ V, @$V_g = 2$ V), where the box checked by the red dashed line is an enlarged picture between the source and the channel. (c) Energy band diagram for $L_{p2}$ varying from 1 nm to 10 nm in the off-state at $L_{p1} = 2$ nm and $N_p = 1\times10^{20}$ cm$^{-3}$ (@$V_d = 1$ V, @$V_g = 0$ V).

Therefore, the conduction band in the pocket 2 and the valence band in the source overlap, and electrons from the source can enter the channel with no gate voltage applied, and thus band-to-band tunneling occurs, as shown in Fig. 3(c) along the line $A$–$A'$ in Fig. 1. Therefore, for a fixed $L_{p1}$ of 2 nm and a pocket doping concentration of $1\times10^{20}$ cm$^{-3}$, the device has an on-state current $> 10^{-4}$ A/μm, an off-state current $< 10^{-15}$ A/μm, and $I_{on}/I_{off}$ of approximately $10^{11}$ at $L_{p2} \leq 2$ nm. To further optimize $L_{p2}$, the DC and analog characteristics of the device for both $L_{p2}$ of 1 nm and 2 nm are compared and analyzed.

The calculated DC characteristics (e.g., $I_{on}$, $I_{off}$, $SS_{avg}$, $I_{on}/I_{off}$) are shown in Table 2. $SS$ is defined as the change in gate voltage which must be applied in order to create a one decade increase in the output current,[1] defined by $(\mathrm{d}\log I_d/\mathrm{d}V_{gs})^{-1}$ in units of mV/decade.[25] In this work, the average subthreshold swing and point subthreshold swing performance metrics are adopted. $SS_{point}$ is measured around the voltage corresponding to a drain current of $10^{-7}$ A/μm. Several methods of defining subthreshold swing have been proposed for TFETs.[1,34] Bhuwalka[34] and Boucart and Ionescu[1] have proposed definitions for calculating the $SS_{avg}$,[25] defined as

$$SS_{avg} = \frac{V_{TH} - V_{OFF}}{\log\left(\dfrac{I_{TH}}{I_{OFF}}\right)}, \tag{1}$$

where $V_{TH}$ is the threshold voltage whose value is the voltage corresponding to a drain current $I_{TH}$ of $10^{-7}$ A/μm. Since the minimum tunneling current varies in different cases, the $V_{OFF}$ in this work is the voltage corresponding to a drain current $I_{off}$ of $10^{-14}$ A/μm.

**Table 2.** Simulated results ($I_{on}$, $I_{off}$, $SS_{avg}$, $I_{on}/I_{off}$ and $g_m$) extracted from the transfer characteristics at $L_{p2} = 1$ nm and 2 nm.

| $L_{p2}$ (nm) | $I_{on}$ (A/μm) | $I_{off}$ (A/μm) | $SS_{avg}$ (mV/dec) | $I_{on}/I_{off}$ | $g_m$ (S) |
|---|---|---|---|---|---|
| 1 | $2.014\times10^{-4}$ | $2.779\times10^{-16}$ | 28.437 | $7.247\times10^{11}$ | $3.39\times10^{-4}$ |
| 2 | $2.060\times10^{-4}$ | $9.509\times10^{-16}$ | 26.723 | $2.166\times10^{11}$ | $2.68\times10^{-4}$ |

Table 2 shows different DC and analog parameters extracted from the transfer characteristics between $L_{p2} = 1$ nm and 2 nm. It is obvious that the numerical results for $I_{on}$ and $SS_{avg}$ at $L_{p2} = 1$ nm are similar to those at $L_{p2} = 2$ nm, while the latter ($I_{off} = 9.509\times10^{-16}$ A/μm for $L_{p2} = 2$ nm) has an off-state current approximately 3.42 times higher than the former ($I_{off} = 2.779\times10^{-16}$ A/μm for $L_{p2} = 1$ nm). Hence, the $I_{on}/I_{off}$ of the former ($I_{on}/I_{off} = 7.247\times10^{11}$ for $L_{p2} = 1$ nm) is three times more than that of the latter ($I_{on}/I_{off} = 2.166\times10^{11}$ for $L_{p2} = 2$ nm). It is important to add that a critical indicator of the analog characteristics of the device is the $g_m$, which represents the gate controllability over the drain current, i.e., the relative change in drain current with the change in gate voltage, as shown below:

$$g_m = \frac{\mathrm{d}I_d}{\mathrm{d}V_{gs}}. \tag{2}$$

It can also be found that $g_m$ at $L_{p2} = 1$ nm ($3.39\times10^{-4}$ S) is slightly higher than that at $L_{p2} = 2$ nm ($2.68\times10^{-4}$ S) from Eq. (2) and Table 2. Based on the factors mentioned above, the optimum $L_{p2}$ is found to be 1 nm for $L_{p1} = 2$ nm and $N_p = 1\times10^{20}$ cm$^{-3}$.

The pocket doping concentration ($N_p$) also has an impact on the electrical properties of the CSP-TFET device fixing $L_{p1}$ and $L_{p2}$. From Figs. 4 and 5(a), it can be seen that the on-state current of the device increases by 30.8% when the pocket doping concentration increases from $2\times10^{19}$ cm$^{-3}$ to $1\times10^{20}$ cm$^{-3}$, and reaches a peak value of $2.01\times10^{-4}$ A/μm when the pocket doping concentration reaches $1\times10^{20}$ cm$^{-3}$ at $L_{p1} = 2$ nm and $L_{p2} = 1$ nm. This is possibly because in pocket 2, the pocket doping concentration becomes higher, making the pocket region fully depleted, thus leading to an increase in the electric field between the source and channel, and therefore increasing the BTBT current. It is observed from Figs. 4, 5(a) and 5(b) that the off-state currents of the CSP-TFET devices increase with the pocket doping concentration but $I_{off} < 10^{-14}$ A/μm, and $I_{on}/I_{off} > 10^{10}$. The $SS_{avg}$ of the device in Fig. 5(b) continue to decrease with increasing $N_p$, decreasing by $\sim 18$ mV/dec, which can be reflected in the transfer characteristics in Fig. 4. It can be clearly seen that the higher the $N_p$ is, the steeper the slope of the curve in the subthreshold region becomes, which leads to the faster switching speed of the CSP-TFET device. Thus, there exists an optimum pocket doping concentration ($N_p$) of $1\times10^{20}$ cm$^{-3}$ at $L_{p1} = 2$ nm and $L_{p2} = 1$ nm for better DC characteristics.

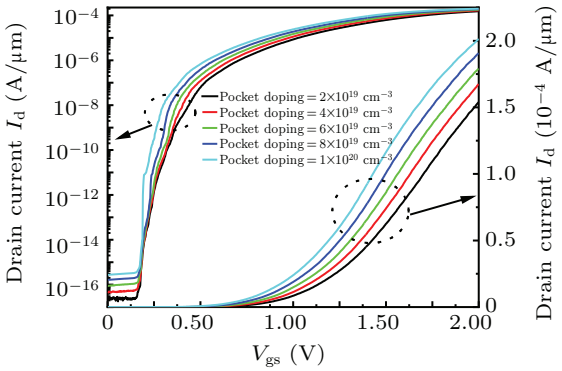



**Fig. 4.** Effect of pocket doping concentration variation on transfer characteristics at $L_{p1} = 2$ nm and $L_{p2} = 1$ nm (@$V_d = 1$ V, @$V_g = 2$ V), where the left $Y$-axis is the logarithmic curve and the right $Y$-axis is the linear curve.

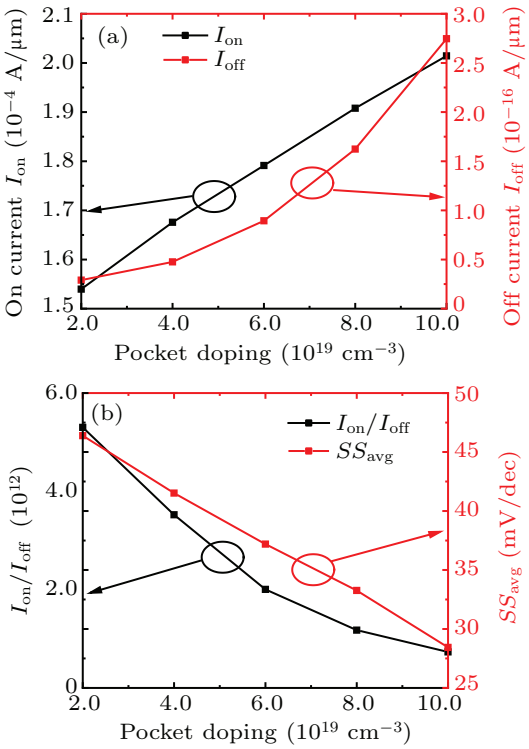



**Fig. 5.** Impact of pocket doping concentration variation on (a) $I_{on}$ and $I_{off}$; (b) $I_{on}/I_{off}$ and $SS_{avg}$ at $L_{p1} = 2$ nm and $L_{p2} = 1$ nm.

### 3.2. Effect of $L_{p1}$

The effect of $L_{p1}$ on the DC and analog/RF characteristics of the CSP-TFET device is investigated for a fixed optimum value of $N_p = 1 \times 10^{20}$ cm$^{-3}$ and $L_{p2} = 1$ nm.

#### 3.2.1. DC characteristics

The effect of $L_{p1}$ on the transfer characteristics of the device is shown in Fig. 6. The linear curves in Figs. 6 and 8 reveal that as $L_{p1}$ increases from 2 nm to 30 nm, the curve in the subthreshold region of the transfer characteristics becomes steeper. The $SS_{avg}$ decreases by approximately 16 mV/dec, while the on-state current increases by about $8.0\times10^{-4}$ A/μm. The off-state current also becomes larger with an increase of $L_{p1}$, with an upper limitation of $10^{-14}$ A/μm. Hence, $I_{on}/I_{off}$ is still greater than $10^7$.

The experiment begins with a default gate position that completely covers the pocket and the channel. The effect of the gate position on the CSP-TFET device will be discussed later in Subsection 3.2. Figure 7 shows the comparison of the physical electric field diagrams and electron BTBT tunneling rate diagrams with $L_{p1}$ of 2 nm and 30 nm, respectively, for a given gate bias. Figures 7(b) and 7(d) show that the longer the $L_{p1}$ is, the more the gate and pocket regions overlap, which leads to in the electric field extending towards the source, i.e., tunneling electrons are generated vertically and horizontally along pocket 2, which leads to more electrons being collected by the drain. Thus, the optimized DC characteristics of the device is found at $L_{p1} = 30$ nm. In this case, the average subthreshold swing is 12.19 mV/dec, the transconductance is $1.268\times10^{-3}$ S, the on-state current is $9.98\times10^{-4}$ A/μm, the off-state current is $3.681 \times 10^{-15}$ A/μm, and the $I_{on}/I_{off}$ is $2.71 \times 10^{11}$.

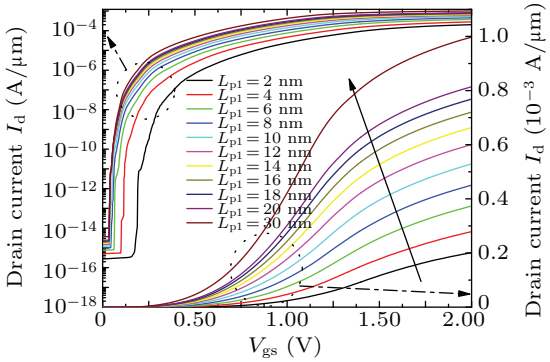



**Fig. 6.** Effect of $L_{p1}$ variation on transfer characteristics of the device at $L_{p2} = 1$ nm and $N_p = 1 \times 10^{20}$ cm$^{-3}$ (@$V_d = 1$ V, @$V_g = 2$ V), where the left $Y$-axis is the logarithmic curve and the right $Y$-axis is the linear curve.

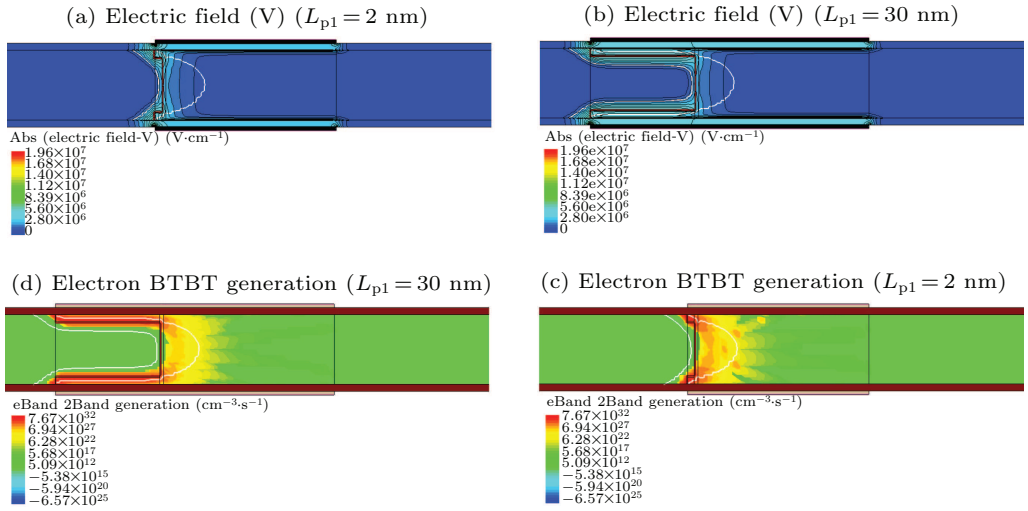



**Fig. 7.** Contour plots of electric field and electron BTBT generation distribution at (a), (c) $L_{p1} = 2$ nm (b), (d) $L_{p1} = 30$ nm at $L_{p2} = 1$ nm and $N_p = 1 \times 10^{20}$ cm$^{-3}$.

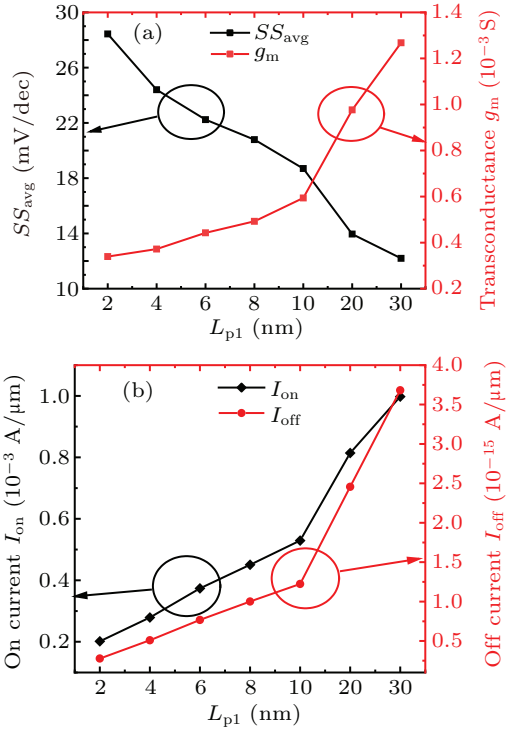



**Fig. 8.** Impact of $L_{p1}$ variation on (a) $SS_{avg}$ and $g_m$; (b) $I_{on}$ and $I_{off}$ at $L_{p2} = 1$ nm and $N_p = 1 \times 10^{20}$ cm$^{-3}$.

### 3.2.2. Analog/RF characteristics

Having investigated the DC characteristics, this section evaluates the analog/RF characteristics of the CSP-TFET device. The simulated performance parameters are analyzed by using an AC analytical method, and the capacitance parameters are extracted at an operating frequency of 1 MHz frequency conditions. The $g_m$ is an important indicator to measure the analog characteristics of devices,[35] and a higher $g_m$ makes the device beneficial for analog applications. Analysis of the analog parameter $g_m$ plays a critical role in obtaining higher $f_T$ and GBP.[36] The transconductance is defined as Eq. (2). Figure 9(a) shows the transconductance of the CSP-TFET device with different $L_{p1}$ and it is shown that the maximum $g_m$ ($g_{m,max}$) of the CSP-TFET device is $1.268 \times 10^{-3}$ S at $L_{p1} = 30$ nm. Furthermore, $g_m$ is increased with $V_{gs}$, for $V_{gs}$ below 1 V, beyond which $g_m$ starts to decrease at $L_{p1} = 30$ nm.The decrease in $g_m$ after $g_m$ reaches the $g_{m,max}$ is probably caused by carrier velocity saturation at high electric fields, leading to the degradation of the carrier mobility. Figures 9(b)–9(d) show the variation of the gate-to-source capacitance ($C_{gs}$), the gate-to-drain capacitance ($C_{gd}$) and the gate capacitance ($C_{gg} = C_{gs} + C_{gd}$) with $V_{gs}$ for $L_{p1}$ ranging from 2 nm to 30 nm. The capacitance parameters also have influence on the $f_T$ and GBP, which will be discussed later. The cut-off frequency, which is the frequency at which the current gain becomes unity, plays a significant role in deciding the device performance at high frequency,[37] as shown below:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2\left(\frac{C_{gd}}{C_{gs}}\right)}} \cong \frac{g_m}{2\pi(C_{gs}+C_{gd})} \cong \frac{g_m}{2\pi C_{gg}}. \tag{3}$$

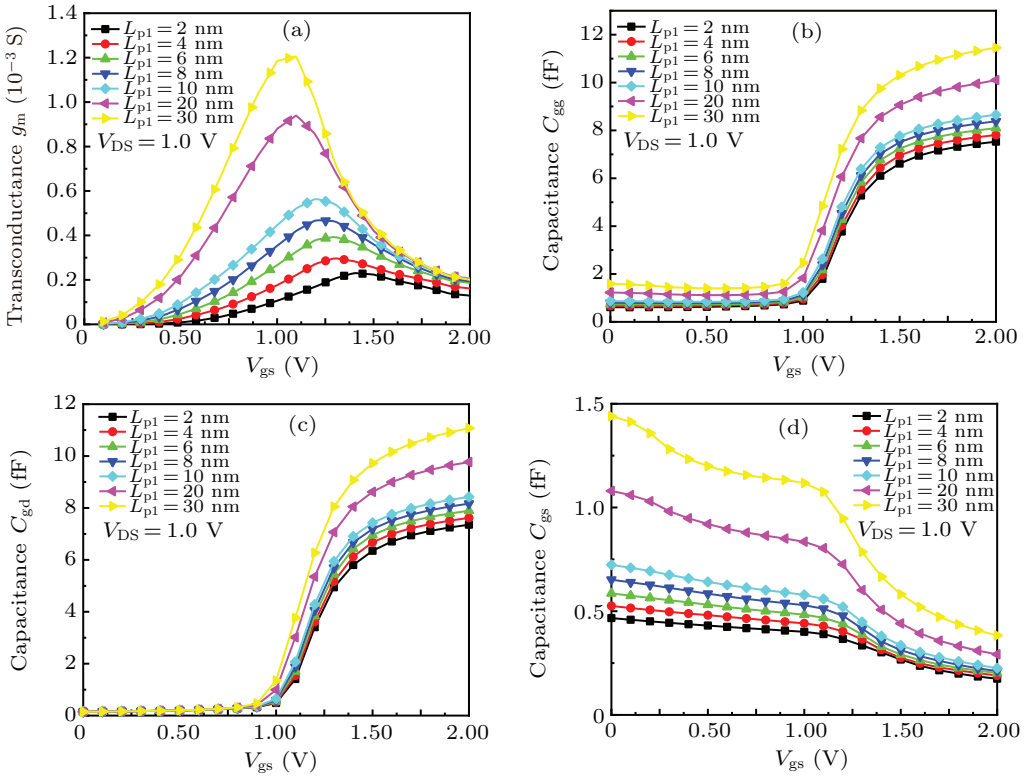



**Fig. 9.** Variation of (a) $g_m$, (b) $C_{gg}$, (c) $C_{gd}$, (d) $C_{gs}$ with different $L_{p1}$ from 2 nm to 30 nm.

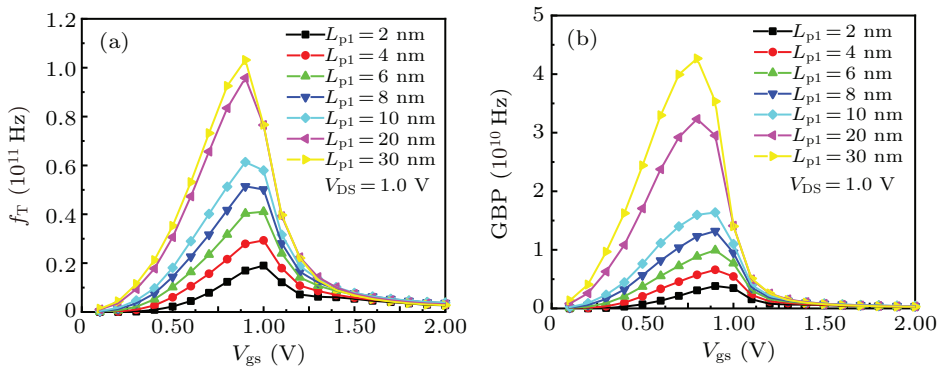



**Fig. 10.** Variation of (a) $f_T$ and (b) GBP with different $L_{p1}$ from 2 nm to 30 nm.

Figure 10(a) shows the variation of $f_T$ with $V_{gs}$ as $L_{p1}$ ranges from 2 nm to 30 nm. It is observed from Eq. (3) that $f_T$ is proportional to $g_m$ and inversely proportional to $C_{gg}$. Note that $C_{gg}$ remains at a small value for all curves when $V_{gs} < 0.9$ V and then increases rapidly with $V_{gs}$, when $V_{gs} > 0.9$ V in Fig. 9(b). The cut-off frequency variation with $V_{gs}$ when $V_{gs} > 0.9$ V, as shown in Fig. 10(a), decreases sharply after reaching the maximum cut-off frequency ($f_{Tmax}$) because $g_m$ decreases with $V_{gs}$ and $C_{gg}$ increases with $V_{gs}$, which leads to a faster rate of $f_T$ decline. Figure 10(a) shows that as $L_{p1}$ increases to 30 nm, the CSP-TFET device shows the highest cut-off frequency of $1.0316\times10^{11}$ Hz when $V_{gs} = 0.9$ V. GBP is another significant parameter, which represents the product of gain and bandwidth of the active device or circuit. The value of GBP is expressed as follows:

$$\mathrm{GBP} = \frac{g_m}{2\pi 10 C_{gd}}. \tag{4}$$

From Eq. (4), GBP is still proportional to $g_m$ and inversely proportional to $C_{gd}$. Figure 10(b) shows the variation of GBP with $V_{gs}$ as $L_{p1}$ ranges from 2 nm to 30 nm and the trend of GBP is basically the same as Fig. 10(a). Thus, the GBP achieves a maximum value of $4.266\times10^{10}$ Hz when $L_{p1} = 30$ nm.

### 3.3. Effect of the location of the gate

Based on the discussion above, the optimal $L_{p1}$, $L_{p2}$ and $N_p$ of the proposed CSP-TFET device are selected as 30 nm, 1 nm and $1\times10^{20}$ cm$^{-3}$, respectively. In order to investigate the effect of gate-to-pocket overlapping structures on the electrical properties of the device, we simulate 6$GS_{ove}$s: 3 nm, 6 nm, 12 nm, 18 nm, 24 nm, and 30 nm (in this work, we define $GS_{ove}$ as $L\times L_{p1}$ and simulate 6$L_s$: 0.1, 0.2, 0.4, 0.6, 0.8, and 1.0 for a fixed optimum $L_{p1}$ value of 30 nm), which represent the length of the overlapping region between the gate and pocket 1. $L$ is the gate-to-pocket overlapping factor.

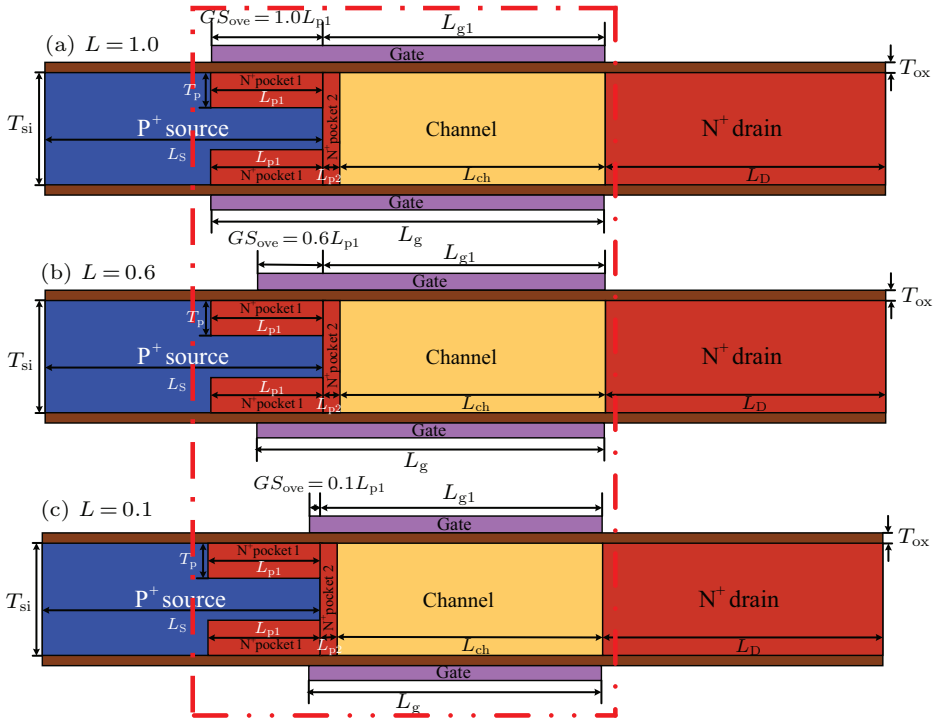



**Fig. 11.** Structure diagrams of the variation of $L$ ranging from 0.1 to 1.0.

Figure 11 shows the structure diagram of the CSP-TFETs with the change of $L$ (1.0, 0.6, and 0.1). For $0 < L \leq 1$, $L = 1$ represents the gate fully overlapping the pocket region (including pocket 1 and pocket 2) and $0 < L < 1$ denotes the gate partially overlapping of the pocket region.

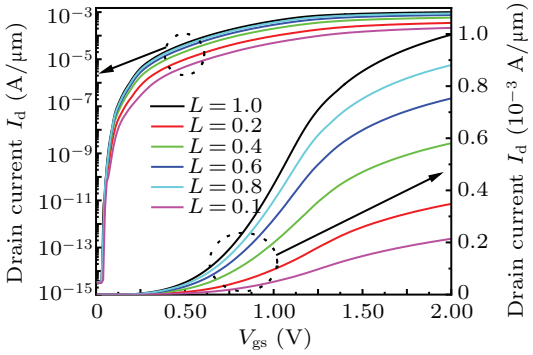



**Fig. 12.** Effect of $L$ (the change in position of the gate) on the transfer characteristics of the CSP-TFET at $L_{p1} = 30$ nm, $L_{p2} = 1$ nm, $N_p = 1 \times 10^{20}$ cm$^{-3}$ (@$V_d = 1$ V, @$V_g = 2$ V), where the sitting $Y$-axis is a logarithmic curve and the right $Y$-axis is a linear curve.

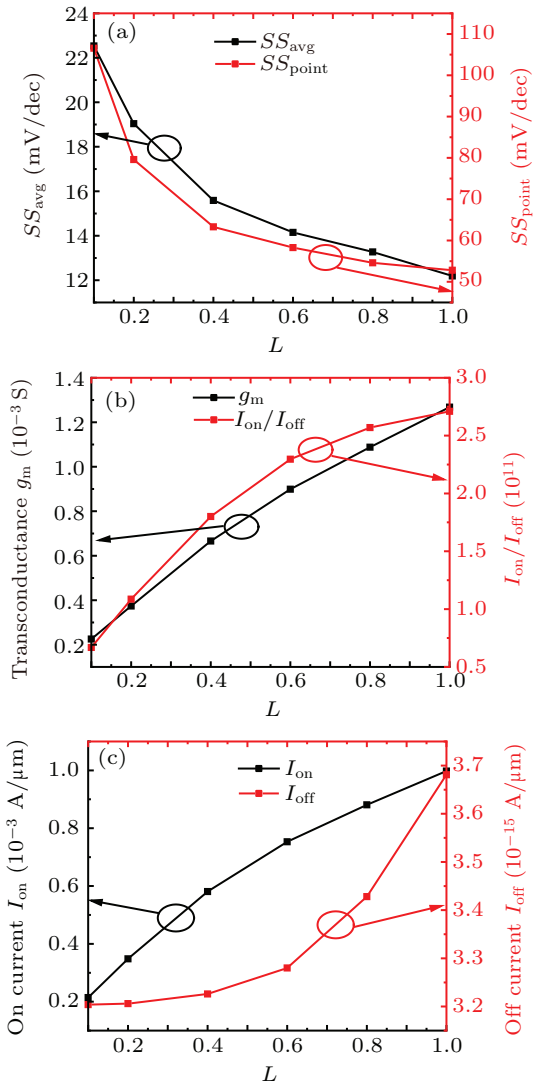



**Fig. 13.** Impact of $L$ variation on (a) $SS_{avg}$ and $SS_{point}$; (b) $g_m$ and $I_{on}/I_{off}$; (c) $I_{on}$ and $I_{off}$.

Figure 12 shows the effect of $L$ on the transfer characteristics of the CSP-TFET device. Figures 13(a)–13(c) illustrate the DC and transconductance parameters extracted from Fig. 12. Figure 13(a) shows $SS_{avg}$ and $SS_{point}$ as a function of $L$. It can be seen that both $SS_{avg}$ and $SS_{point}$ decrease as $L$ increases, with $SS_{avg}$ improving by 10.342 mV/dec and $SS_{point}$ decreasing by 53.7 mV/dec. Figure 13(b) shows the variation of $g_m$ and $I_{on}/I_{off}$ as $L$ ranges from 0.1 to 1.0. For $L = 1.0$, the device has the maximum value in terms of $g_m$ and $I_{on}/I_{off}$ and shows better gate controllability and switching capability. Moreover, Fig. 13(c) shows $I_{on}$ and $I_{off}$ vary with $L$. It is clear that the on-state current improves by $7.834 \times 10^{-4}$ A/μm when $L$ increases from 0.1 to 1.0. According to Figs. 12 and 13, for $L = 1.0$, i.e., fully gate-to-pocket overlapping structure, the CSP-TFET device has the smallest $SS_{avg}$ and $SS_{point}$, the largest $I_{on}$, $I_{on}/I_{off}$, and $g_m$, which has the optimized DC and analog characteristics.

## 4. Conclusion and perspectives

In this paper, a C-shaped pocket TFET with the gate covering the pocket based on the double-gate TFET is proposed and analyzed. The pocket is C-shaped which is incorporated between source and channel to enhance device performance. The pocket length and pocket doping concentration affect the DC and analog/RF performance of the C-shaped pocket TFET. The use of fully gate-to-pocket overlapping structure results in the improvements of gate controllability and current driving capability. Our results demonstrate that high pocket doping concentration ($N_p$) and narrow pocket 2 length ($L_{p2}$) can achieve better electrical properties. The increase in pocket 1 length ($L_{p1}$) results in a larger overlapping region between the gate and pocket, which increases the electric field, and then increases the BTBT rate of the electrons. The silicon-based double-gate CSP-TFET demonstrated superior DC and analog/RF performance with $I_{on} = 9.98 \times 10^{-4}$ A/μm, $SS_{avg} = 12.19$ mV/dec, $SS_{point} = 52.81$ mV/dec, $g_m = 1.268 \times 10^{-3}$ S, $I_{on}/I_{off} = 2.71 \times 10^{11}$, $f_T = 1.0316 \times 10^{11}$ Hz and GBP $= 4.266 \times 10^{10}$ Hz at $L_{p1} = 30$ nm, $L_{p2} = 1$ nm and $N_p = 1 \times 10^{20}$ cm$^{-3}$. The results of this work indicates that the CSP-TFET device is suitable for high speed and low power applications.

## Acknowledgements

Project supported by the National Natural Science Foundation of China (Grant Nos. 52177185 and 62174055) and Open Fund of Shanghai Key Laboratory of Multidimensional Information Processing, East China Normal University (Grant No. 2019MIP002).

## References

[1] Boucart K and Ionescu A M 2007 *IEEE Trans. Electron. Devices* **54** 1725

[2] Chen Z X, Yu H Y, Singh N, Shen N S, Sayanthan R D, Lo G Q and Kwong D L 2009 *IEEE Electron. Device Lett.* **30** 754

[3] Hu C M, Patel P, Bowonder A, Jeon K, Kim S H, Wei Y L, Chang Y K, Jungwoo O, Majhi P, Javey A, Liu T J K and Jammy R 2010 *International Electron Devices Meeting*, December 6–8, 2010, San Francisco, CA, USA, p. 16.1.1

[4] Omura Y, Mallik A and Matsuo N 2017 *MOS Devices for Low-Voltage and Low-Energy Applications* (Singapore: John Wiley & Sons) pp. 53–80

[5] Avci U E, Morris D H and Young I A 2015 *IEEE J. Electron. Devices Soc.* **3** 88

[6] Saurabh S and Kumar M J 2011 *IEEE Trans. Electron. Devices* **58** 404

[7] Lu H and Seabaugh A 2014 *IEEE J. Electron. Devices Soc.* **2** 44

[8] Rajoriya A, Shrivastava M, Gossner H, Schulz T and Rao V R 2013 *IEEE Trans. Electron. Devices* **60** 2626

[9] Ionescu A M and Riel H 2011 *Nature* **479** 329

[10] Yoon Y J, Woo S Y, Seo J H, Lee J S, Park Y S, Lee J H and Kang I M 2012 *J. Korean Phys. Soc.* **61** 1679

[11] Chatterjee N, Gupta A and Pandey S 2016 *International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT)*, March 11–13, 2016, New Delhi, India, p. 118

[12] Kumar N and Raman A 2020 *Silicon* **12** 2627

[13] Kim S W, Kim J H, Liu T J K, Choi W Y and Park B G 2016 *IEEE Trans. Electron. Devices* **63** 1774

[14] Li C, Zhao X L, Zhuang Y Q, Yan Z R, Guo J M and Han R 2018 *Superlattices Microstruct.* **115** 154

[15] Liu K M and Cheng C P 2020 *IEEE Trans. Nanotechnol* **19** 382

[16] Dubey P K, Kaushik B K 2017 *IEEE Trans. Electron. Devices* **64** 3120

[17] Choi W Y and Lee W 2010 *IEEE Trans. Electron. Devices* **57** 2317

[18] Li C, Yan Z R, Zhuang Y Q, Zhao X L and Guo J M 2018 *Chin. Phys. B* **27** 078502

[19] Lee J W and Choi W Y 2020 *IEEE Access* **8** 67617

[20] Avci U E and Young I A 2013 *IEEE International Electron Devices Meeting*, December 9–11, 2013, Washington, DC, USA, p. 4.3.1

[21] Lu Y Q, Zhou G L, Li R, Liu Q M, Zhang Q, Vasen T, Chae S D, Kosel T, Wistey M, Xing H L, Seabaugh A and Fay P 2012 *IEEE Electron. Device Lett.* **33** 655

[22] Tomioka K, Yoshimura M and Fukui T 2012 *Symposium on VLSI Technology (VLSIT)*, June 12–14 2012, Honolulu, HI, USA, p. 47

[23] Cui N, Liang R R and Xu J 2011 *Appl. Phys. Lett.* **98** 142105

[24] Beneventi G B, Gnani E, Gnudi A, Reggiani S and Baccarani G 2015 *IEEE Trans. Electron. Devices* **62** 44

[25] Seabaugh A C and Zhang Q 2010 *Proc. IEEE Inst. Electr. Electron. Eng.* **98** 2095

[26] Nagavarapu V, Jhaveri R and Woo J C S 2008 *IEEE Trans. Electron. Devices* **55** 1013

[27] Jhaveri R, Nagavarapu V and Woo J C S 2011 *IEEE Trans. Electron. Devices* **58** 80

[28] Li W C and Woo J C S 2018 *IEEE Trans. Electron. Devices* **65** 5289

[29] Kao K H, Verhulst A S, Vandenberghe W G, Soree B, Magnus W, Leonelli D, Groeseneken G and Meyer K De 2012 *IEEE Trans. Electron. Devices* **59** 2070

[30] Abdi D B and Kumar M J 2014 *IEEE Electron. Device Lett.* **35** 1170

[31] Sahoo S, Dash S, Routray S R and Mishra G P 2021 *Int. J. Numer. Model. El.* **34** e2808

[32] Li W C and Woo J C S 2020 *IEEE Trans. Electron. Devices* **67** 1480

[33] Yang Z N 2016 *IEEE Electron. Device Lett.* **37** 839

[34] Bhuwalka K K, Schulze J and Eisele I 2005 *IEEE Trans. Electron. Devices* **52** 1541

[35] Xie H W and Liu H X 2020 *AIP Adv.* **10** 055125

[36] Dharmender and Nigam K 2020 *Silicon* **13** 2347

[37] Singh A K, Tripathy M R, Baral K, Singh P K and Jit S 2020 *Microelectron. J.* **102** 104775