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Citation: Chin. Phys. B, 2022, 31 (**5**): 058503. DOI: 10.1088/1674-1056/ac3819
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MOS-based model of four-transistor CMOS image sensor pixels for photoelectric simulation

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(Received 9 September 2021; revised manuscript received 4 November 2021; accepted manuscript online 10 November 2021)

By using the MOS-based model established in this paper, the physical process of photoelectron generation, transfer, and storage in the four-transistor active pixel sensor (4T-APS) pixels can be simulated in SPICE environment. The variable capacitance characteristics of double junctions in pinned photodiodes (PPDs) and the threshold voltage difference formed by channel nonuniform doping in transfer gates (TGs) are considered with this model. The charge transfer process of photogenerated electrons from PPDs to the floating diffusion (FD) is analyzed, and the function of nonuniform doping of TGs in suppressing charge injection back to PPDs is represented with the model. The optical and electrical characteristics of all devices in the pixel are effectively combined with the model. Moreover, the charge transfer efficiency and the voltage variation in PPD can be described with the model. Compared with the hybrid simulation in TCAD and the Verilog-A simulation in SPICE, this model has higher simulation efficiency and accuracy, respectively. The effectiveness of the MOS-based model is experimentally verified in a 3 μm test pixel designed in 0.11 μm CIS process.

Keywords: four-transistor active pixel sensor (4T-APS), nonuniform doping, SPICE model, transfer gate, variable capacitance

PACS: 85.30.–z **DOI:** 10.1088/1674-1056/ac3819

1. Introduction

The excellent performance of CMOS image sensors (CISs) has led to the widespread use of pinned photodiode (PPD) based four-transistor active pixel sensors (4T-APSs) in various commercial and scientific areas. PPDs and transfer gates (TGs) are the two main components of 4T-APS. The heavily doped pinned layer isolates the charge storage region from the surface defects and traps that exist at the Si/SiO_2 interface, resulting in a low current leakage rate.[1–3] The nonuniform doping of TGs helps to stop the photogenerated electrons from being injected back to the photodiode, and thus eliminating the image lag.[4] Various key parameters such as the pinned voltage (V_{pin}), full well capacity (FWC), and PPD capacitance (C_{PPD}) have been used to quantify the charge storage capacity and evaluate the features of the pixels.[5] As the core components of 4T-APS [i.e., TG, PPD, and floating diffusion (FD)] directly affect the FWC, transfer efficiency, noise, conversion gain, and quantum efficiency of CIS, they have been widely discussed in the academia and industry.[6–9]

To determine the transfer characteristics of TGs, thermionic emission theory is applied in the qualitative explanation of image lag caused by the potential barrier.[10] Subthreshold current characteristics are used to analyze the charge transfer and image lag in TGs.[11] A second-order response system model based on the above theory has been established,[12–14] providing a more accurate physical model to explain the microscopic phenomena. As a result, several refined device designs have been developed.[15,16] For the PPD structure and its characterization, the relationship between the channel barrier height and FWC of the PPD during TG shutdown has been established.[12] The FWC qualitative analysis model of PPD uses the abstract pinned voltage model to fit the temperature and the concept of PPD capacitance.[10–17] The FWC model assumes a positive bias state and the equivalent theory of the depletion zone.[18,19] However, the test results are not in good agreement with the constant PPD capacitance model.[20] A variable capacitance model has been established based on mathematical analysis,[21] and a qualitative model based on the Fermi level equilibrium hypothesis has been reported.[10–22] Few studies, however, have attempted to identify how the TG functions together with the PPD influence the entire charge transfer process, and directly impact the charge transfer speed and the charge transfer efficiency. Additionally, there is no compact model that combines key parameters to reflect the entire operation process of PPD.[23] Furthermore, the above-mentioned models cannot be integrated into the SPICE framework. Thus, it is hard to effectively evaluate the compatibility between devices and system indicators.

Therefore, in this paper, we propose a matching approach

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with the MOS-based model to describe and simulate the working process of the 4T-APS pixels. The charge transfer process of the pixels is analyzed, and the role of nonuniform doping of TGs is investigated by using the resulting model. Finally, the effectiveness of the model is verified by the consistency between the simulation output and measurement results of a prototype PPD-based 4T-APS pixel.

2. MOS-based model in TGs

As shown in Fig. 1(a), there are two key design points in PPDs. (1) The photoelectric part: the width of the body depletion region and the pinned voltage are determined by the matching design of the epitaxial layer, pinned clamp layer, and the N-well implant concentration and depth. Thus, we can optimize the quantum efficiency (QE) of a specific spectral range and the PPD side potential during the photoelectric process. (2) The charge transfer part: to ensure the monotonicity of the potential distribution when the process of charge transfer from PPD to FD by the ON-state of TG, the size of the threshold voltage adjustment layer covering all PPDs and half parts of the TG channels. In TCAD simulation, the length of PPD and TG is 3 μm and 0.6 μm, respectively. In addition, the doping of TGs and threshold voltage adjustment layer is 4.5×10^{15} cm^{-3} and 2.2×10^{12} cm^{-3}, respectively. The potential distributions corresponding to the ON and OFF states of TG are respectively shown in Figs. 1(b) and 1(c). Therefore, TG+PPD cannot be regarded as an ordinary surface type four-terminal MOS device.

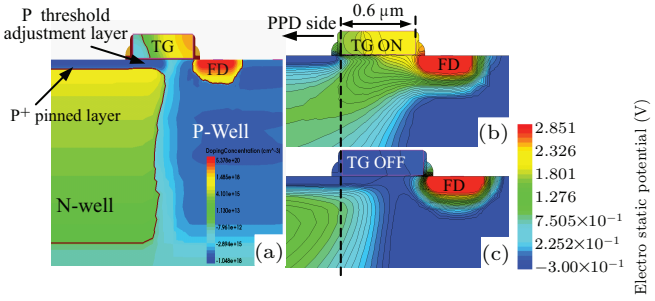


Fig. 1. Typical TG and PPD structures. (a) doping diagram, (b) and (c) potential distributions corresponding to the ON and OFF states of TG, respectively.

The schematic of a 4T-APS built by a general SPICE model is shown in Fig. 2(a) (spectre circuit simulation environment). The PPD and TG are equivalent to an ideal current source in parallel with a constant capacitance and a symmetrical MOS transistor, respectively. The working principle is illustrated in Fig. 2(b), where RESET MOS is used to reset the voltages of the FD and PPD capacitors, and the PPD capacitor is integrated by the current source (I_{photo}). To change the FD potential, a TG MOS is used to redistribute the integrated charges in the FD and PPD capacitors. The simulation results of this 4T-APS circuit provide an input reference signal for a readout circuit, which may match the system timing but have no physical significance, as shown in Fig. 2(b). The problems with this general SPICE model are as follows. (1) The photoelectric conversion characteristics of the PPD are expressed by a constant current source, which have no physical meaning. Because the equivalent of this method cannot represent the true current value that changes with the input light intensity and wavelength under the specific quantum efficiency of the device. (2) C_{PPD} should not be a constant capacitor, as a constant capacitance that can be reset to any voltage value cannot represent the clamping voltage characteristic of the PPD. The difference in V_{PPD} after switching off the TG twice in Fig. 2(b) illustrates this problem. (3) A regular single threshold voltage of TG MOSFET model is not consistent with the characteristics of a nonuniform doping channel transfer gate. As shown in Fig. 2(b), the V_{FD} does not change under different V_{TG} at 25 μs, and it is inconsistent with the physical process that different gate voltages will lead to different transfer efficiency. Thus, it is necessary to build a SPICE environment electrical model that reflects the whole physical process of 4T-APS pixel. Therefore, we propose a MOS-based combined model, including a photoelectric model and a transfer model to solve the above problems. The proposed approach is illustrated in Fig. 3 and can be described as following.

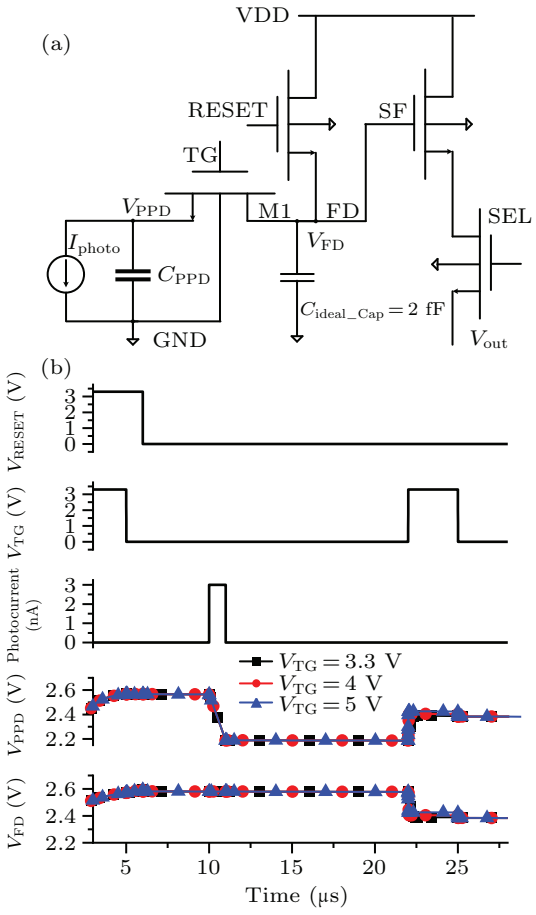


Fig. 2. (a) Schematic of 4T pixel with a general SPICE model. (b) Simulation results of V_{PPD} and V_{FD} under different V_{TG} are not consistent with the actual switching characteristics of TG.

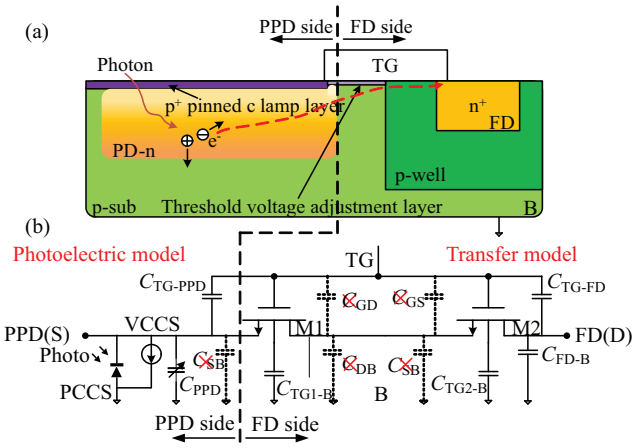


Fig. 3. (a) Structure of PPD and TG. (b) Corresponding schematic of MOS-based equivalent model. The dashed line capacitors represent that need to be removed compared to the regular MOS source and drain junction capacitance. The specific description is shown in Table 1.

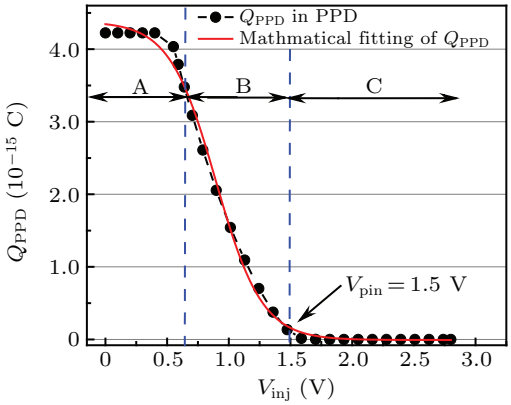


Fig. 4. Charge of injection in PPD ($Q_{\rm PPD}$) for varying injection voltage $V_{\rm inj}$.

2.1. Photoeectric model

In this paper, a photoelectric model is setup to simulate the process of photoelectric conversion in the PPD, as shown on the PPD side of Fig. 3. The equivalence method is described in detail as follows.

Step 1 As shown in Fig. 3, the PPD side of the TG is replaced by a pinned photodiode, where a variable PPD capacitance, $C_{\rm PPD}$, is substituted for the capacitance of the source end of the TG, $C_{\rm SB}$. To obtain the charge in the PPD ($Q_{\rm PPD}$) versus voltage of PPD ($V_{\rm PPD}$) equation for capacitance model, a standard CMOS 4T-pixel with 3 μm pixel designed in 0.11 μm CIS process. These Q–V models of PPD capacitances are also reported.[21–24] In the measurement setup, electrical injection of charges instead of optical integration is adopted to prevent measurement variations due to light. The drain voltage of reset transistor (VDD_RST) is externally controllable and the source of reset transistor is connected to the FD node. VDD_RST is the injected voltage ($V_{\rm inj}$), which is varied to inject electrons via the floating diffuse node (FD) into photodiode well. The test curve of $Q_{\rm PPD}$ and the corresponding injected voltage ($V_{\rm inj}$) is shown in Fig. 4. The estimation of $V_{\rm pin}$ is done as[22] shown in Fig. 4. In region B, PPD is in a valid reset state, so $V_{\rm PPD} = V_{\rm inj}$. The starting portion (region A) is dominated by the feed-forward effect[17] (the read-out chain is not saturation). The tail portion (region C) is dominated by the pinning process and thermal emission. Only the middle portion can define $V_{\rm PPD}$ normally. The quantitative $Q_{\rm PPD}$–$V_{\rm inj}$ relationship that is accurately mathematical fitted according to the test data is as follows:

$$Q_{\rm PPD} = -8.08568 \times 10^{-18} + \frac{4.29732 \times 10^{-15}}{1+{\rm e}^{\frac{V_{\rm inj}-0.89516}{0.18734}}}. \tag{1}$$

Step 2 Under this model, the input light is equivalent to a source terminal voltage at TG. The photodiode well is powered by light energy through a photoelectric conversion process. The photocurrent model is set up and the photon control current source (PCCS) originating from the photoelectric process is incorporated into the charge process of the PPD. In this work, in order to simplify the charging model of current source, only the photocurrent ($I_{\rm ph}$) is considered. Then, the photocurrent can be expressed as[25]

$$I_{\rm ph} = \frac{\eta \lambda P_{\rm opt}}{1.24}, \tag{2}$$

where η is the quantum efficiency, λ is the wavelength of light, and $P_{\rm opt}$ represents the incident optical power. In this paper, η of test device is 32%@905 nm through measurement. This innovative specific conversion process is as follows. Firstly, the relationship between the photocurrent $I_{\rm ph}$ of the PPD versus optical power and wavelength is obtained through Eq. (2). Secondly, the behavioral model of VCCS is constructed by the Verilog-A syntax. Thirdly, the charge generated by the photocurrent $I_{\rm ph}$ in the PPD, $Q_{\rm PPD}$, is determined by the integral time $t_{\rm int}$. Fourthly, Eq. (1) is used to determine $V_{\rm inj}$ and $Q_{\rm PPD}$ at the corresponding $t_{\rm int}$ in PPD. Finally, the simplified photoelectric part of generation and collection have been established. This modeling method realizes the state that the internal voltage of the PPD changes with the generation of the photoelectric signal, and the voltage change will affect the PPD junction capacitance characteristics, so this feedback mechanism will affect the timely efficiency of the photoelectric collection. For integral optoelectronic devices, as the integrated charge of PPD increases, the PPD junction voltage decreases, and the photoelectric absorption efficiency tends to zero. The voltage value of the PPD side and the amount of transferable charge in the ON-state of the TG cannot be characterized by the traditional current source model.

2.2. Transfer model

The transfer model simulates the process of charge entering the FD from different doping regions of the TG. For the normal operation of a TG-based PPD structure, the inversion layer of the TG is created by the TG bias and the signal electrons are transferred into the FD region, as shown on the FD side of Fig. 3. The model equivalence method can be described as follows.

Step 1 The PN junction model of the FD region needs some minor revisions to function as the drain terminal of the TG. We use the PN junction model of FD in a p-well provided by the CIS foundry. At the same time, the leakage current characteristics of the FD and PPD with respect to temperature can be obtained from the test results. These junction capacitances and leakage current parameters can be placed into the corresponding nodes.

Step 2 To model the nonuniform doping behavior of the TG under different threshold voltages. The purpose of this equivalence is to simulate the noise and charge injection effects of the TG switching process. Due to the nonuniform doping behavior of the TG, the channel electrons will monotonically transfer to the low-potential FD node during the TG turn-off process. We revise the Berkeley single channel IGFET model (BSIM; IGFET is an insulated-gate field-effect transistor) of a normal MOSFET to connect the modified MOSFET with different $V_{\rm TH}$ in series to act as the nonuniform TG, as shown in Fig. 3. Note that different values of $V_{\rm TH}$ are used to simulate the nonuniform doping of the TG channel in this model. This equivalence is based on the $V_{\rm TH}$ model given by

$$V_{\rm TH} = \phi_{\rm MS} + 2\phi_{\rm F} + \frac{\sqrt{4q\varepsilon_{\rm si}\,|\phi_{\rm F}|\,N_{\rm sub}}}{C_{\rm ox}}, \tag{3}$$

where $\phi_{\rm MS}$ is the work function difference between the gate and the substrate, $\phi_{\rm F} = (kT/q) \times \ln(N_{\rm sub}/n_{\rm i})$, $N_{\rm sub}$ is the doping concentration of the substrate, $C_{\rm ox}$ is the gate oxide capacitance per unit area, and $\varepsilon_{\rm si}$ is the dielectric constant of silicon. As shown in Fig. 3, the substrate under the TG channel is doped under different conditions, so it is reasonable to use a low threshold voltage $V_{\rm TH-L}$ to characterize light p doping and a high threshold voltage $V_{\rm TH-H}$ to characterize heavy p doping in the TG channel. Therefore, W/L for each MOSFET is determined under two different $V_{\rm TH}$ conditions according to the actual injection size of the TG channel.

Step 3 Adjust the capacitance and current density parameters in the BSIM of the series MOSFETs described in step 2. Parameters such asjunction capacitance of source or drain end per unit area (CJ), sidewall junction capacitance per unit periphery (CJSW), gate drain overlap capacitance per unit width (CGDO), gate source overlap capacitance per unit width (CGSO), bottom source junction reverse saturation current density (JSS), isolation edge sidewall source junction reverse saturation current density (JSWS), gate edge source junction reverse saturation current density (JSWGS), bottom drain junction reverse saturation current density (JSD), isolation edge sidewall drain junction reverse saturation current density (JSWD), and gate edge drain junction reverse saturation current density (JSWGD) are considered. Because the actual nonuniform doping TG is a source–drain asymmetrical two-terminal device, part of the node devices will be deleted in the dual MOS structure model, as shown in Fig. 3(b). The BSIM capacitances and current density parameters are presented in Table 1, where $L_{\rm D}$ is the drain/source diffusion length, $W_{\rm eff}$ is the effective width, L the channel length, M_J is the exponent in the CJ formula, $V_{\rm BS}$ is the voltage between body and source end, $V_{\rm BD}$ is the voltage between body and drain end, $C_{\rm F}$ is the full well capacitance, $C_{\rm GS}$ is the capacitance between gate and source end, $C_{\rm GB}$ is the capacitance between gate and bulk, $C_{\rm BD}$ is the capacitance between bulk and drain end, and $C_{\rm SB}$ is the capacitance between bulk and source end.

Table 1. BSIM parameters of MOS-based model.

	M1			M2	
$C_{\rm GS}$	$C_{\rm TG-PPD}$	$C_{\rm GS}$[a]@cutoff region; $C_{\rm GS}$[b]@saturation region; $C_{\rm GS}$[c]@active region;	$C_{\rm GS}$	CGSO = 0;	
$C_{\rm GD}$	$C_{\rm GD}$	CGDO = 0;	$C_{\rm TG-FD}$	$C_{\rm GD}$[f]@cutoff/saturation region; $C_{\rm GD}$[g]@active region;	
$C_{\rm GB}$	$C_{\rm TG1-B}$	$C_{\rm GB}$[d]@cutoff region; $C_{\rm GB}$[e]@saturation/active region;	$C_{\rm TG2-B}$	$C_{\rm GB}$[h]@cutoff region; $C_{\rm GB}$[i]@saturation/active region;	
$C_{\rm SB}$	$C_{\rm SB}$	replaced by (1);	$C_{\rm SB}$	CJSW = 0; CJ = 0; (JSWGS = 0; JSS = 0; JSWS = 0; MJSW = 0;)	
$C_{\rm DB}$	$C_{\rm DB}$	CJSW = 0; CJ = 0; (JSWGD = 0; JSD = 0; JSWD = 0; MJSW = 0;)	$C_{\rm FD-B}$	$C_{\rm BD}$[j]@$V_{\rm BD} \le (FC)(PB)$; $C_{\rm BD}$[k]@$V_{\rm BD} > (FC)(PB)$;	

[a] $C_{\rm GS} = L_{\rm D} \times W_{\rm eff} \times {\rm CGSO}$; [b] $C_{\rm GS} = L_{\rm D} \times W_{\rm eff} \times {\rm CGSO} + \frac{2}{3} \times (L - L_{\rm D}) \times W_{\rm eff} \times {\rm CGSO}$;
[c] $C_{\rm GS} = L_{\rm D} \times W_{\rm eff} \times {\rm CGSO} + \frac{1}{2} \times (L - L_{\rm D}) \times W_{\rm eff} \times {\rm CGSO}$;
[d] $C_{\rm GB} = (L - 2L_{\rm D}) \times W_{\rm eff} \times {\rm CGBO} + 2{\rm CGBO}\,(L - 2L_{\rm D})$; [e] $C_{\rm GB} = 2{\rm CGBO}\,(L - 2L_{\rm D})$;
[f] $C_{\rm GD} = L_{\rm D} \times W_{\rm eff} \times {\rm CGDO}$; [g] $C_{\rm GD} = L_{\rm D} \times W_{\rm eff} \times {\rm CGDO} + 1/2\,(L - 2L_{\rm D}) \times W_{\rm eff} \times {\rm CGDO}$;
[h] $C_{\rm GB} = (L - 2L_{\rm D}) \times W_{\rm eff} \times {\rm CGBO} + 2{\rm CGBO}\,(L - 2L_{\rm D})$; [i] $C_{\rm GB} = 2{\rm CGBO}\,(L - 2L_{\rm D})$;
[j] $C_{\rm BD} = (CJ)\,(AD)/[1 - (V_{\rm BS}/PB)]^{M_J} + (CJDW)\,(PS)/[1 - (V_{\rm BD}/PB)]^{M_J DW}$;
[k] $C_{\rm BD} = (CJ)\,(AD)/\,(1 - FC)^{(M_J+1)\times[1-(1+M_J)FC+M_J(V_{\rm BD}/PB)]} + (CJDW)\,(PD)\,/\,(1 - FC)^{(M_J DW+1)\times[1-(1+M_J DW)FC+M_J DW(V_{\rm BD}/PB)]}$.

3. MOS-based model in 4T pixels

Combining the above two models gives the whole MOS-based model. The photoelectron generation and charge transport behaviors of signal electrons from PPD to FD and the role of the TG in the charge transfer process are investigated. The leakage current model is not considered in this simulation. A schematic of the 4T pixel with the proposed MOS-based model is shown in Fig. 5, where the threshold voltages of M1 and M2 are set to 0.8 V and 0.4 V, respectively, as an example. The quantum efficiency ($\eta = 30\%$) and wavelength of light ($\lambda = 905$ nm) are chosen in this work. The simulation timing include reset, integration, correlated double sampling (CDS) reset and readout phase.

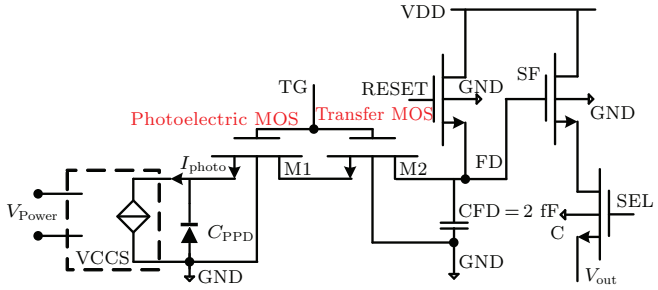


Fig. 5. Schematic of 4T pixel with MOS-based model.

As shown in Fig. 6, we can observe that the TG switches off during the reset phase, and the V_{PPD} decreases from 2.8 V to 1.45 V under illumination. Due to the charge injection effect of the TG, some electrons are injected into the C_{PPD}, that is, the V_{PPD} can quickly decreases to the V_{pin} like region C in Fig. 4. The value of V_{FD} remains almost constant because it is still connected to the VDD terminal through the RESET transistor, the clock feedthrough effect introduced by the RESET switching cannot affect the voltage of the FD node before the TG is turned on, so the injected electrons are also pumped away by this process. However, V_{FD} suffers from the charge injection and the kTC noise of the RESET transistor when it is off.

Then, the light is on after reset phase, and the photogenerated electrons are integrated in the PPD capacitance by a 905 nm light with a power density of 0.05 W/cm^2 for 7 μs, which leads to the V_{PPD} nonlinear decrease from 1.45 V to 0.72 V. Therefore, it is proved that the variable capacitance can accurately simulate the current and voltage characteristics of the PPD in the photoelectric simulation than the conventional current source.

The TG then switches on and the signal electrons start to flow from PPD to FD after CDS reset phase, causing a decrease in V_{FD} and a increase in V_{PPD}. When the TG switches off again, the coupling effect from the TG causes V_{FD} to decrease again. This process implies that when the TG switches on, some of the photo generated electrons are absorbed by the inversion layer of the TG, and other electrons transfer to FD. The inversion electrons will be kicked back to both FD and PPD when the TG switches off. The charge injection from the TG causes some of the photo generated electrons to flow back to PPD, and the potential barrier/pocket under along the electron path is the main reason that affects the electron lag. After using the MOS-based model to be equivalent, these potential effects are replaced by the channel on-resistance and the switching charge sharing effect. Therefore, the photoelectron generation and charge transport behaviors of V_{PPD} and V_{FD} can be expressed correctly by using the above two models to give the whole MOS-based model.

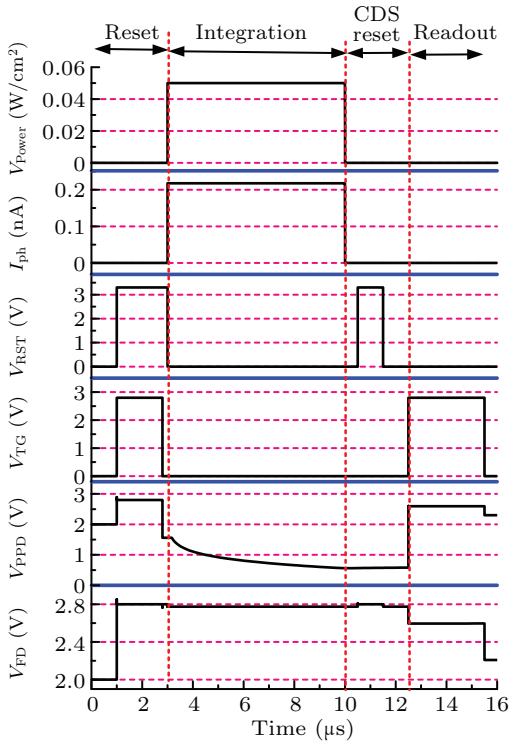


Fig. 6. Simulation results of 4T pixel with MOS-based model.

4. Model validation

4.1. Modeling the charge injection effect by different threshold voltages

To investigate how nonuniform doping could suppress the charge injection effect of the TG, the MOS-based model was executed with three different threshold voltage combinations according to the conditions in Fig. 5. The simulation results are summarized in Table 2. The charge injection from TG to PPD in case A ($V_{TH-M1} = 0.8$ V and $V_{TH-M2} = 0.4$ V) is only 0.0016%, much lower than the 6.49% in case B ($V_{TH-M1} = 0.4$ V and $V_{TH-M2} = 0.4$ V) and 9.12% in case C ($V_{TH-M1} = 0.4$ V and $V_{TH-M2} = 0.8$ V). Case B characterizes the switching characteristics and charge injection effects of a conventional symmetric MOSFET. The simulation results in cases B and C do not match the switching characteristics of TGs. These results confirm the effectiveness of nonuniform TG doping with different threshold voltages MOS-based

model in suppressing the charge injection effect and improving the device performance of charge transfer efficiency. This paper focuses on the use of MOS-based models to characterize the integration and transfer characteristics of optoelectronic devices, so discussion on device optimization is ignored.

Table 2. Charge number under different V_{TH} and reset conditions ($V_{TG} = 2.8$ V, $V_{RST} = 3.3$ V).

Case	(V_{TH_M1}, V_{TH_M2}) (V)	V_{FD} after reset (V)	No. of photo electron	No. electron transfer to FD
A	(0.8, 0.4)	2.75	4783.5	4734.2
B	(0.4, 0.4)	2.75	4783.5	4473.0
C	(0.4, 0.8)	2.75	4783.5	4347.3

4.2. Modeling charge transfer efficiency by TG voltage

We further studied how the gate voltage of the TG influences charge transfer efficiency (CTE) of the pixel both in MOS-based model and TCAD simulations. The condition of case A (in Table 2) and timing process like Fig. 6 are used in MOS-based model simulation. All the simulations are performed at a temperature of 300 K. By comparing the results from these two channel length conditions, the working mechanism of nonuniform TG doping can be determined. It is important to note that only the trend of relationship between V_{TG} and CTE is considered in this work. As shown in Fig. 8, the model potential can not match the actual potential perfectly. The actual potential from PPD to FD change gradually, which is not as same as the stepped potential distribution in MOS-based model. And some second-order effects like both the thermal emission and drain induced barrier lowering (DIBL) can lead to differences in the model and TCAD simulation. As shown in Fig. 7, when the V_{TG} drops from 2.8 V to 1.5 V, the CET decreases approximately linearly from about 100% to 72%. However, the CTE drops from 53% to 21% when V_{TG} changes to 1.5 V. This is mainly due to the M1 transistor enters the sub-threshold region, which leads to the sharp deterioration of CTE. Similar trend can be observed in TCAD simulation, and the knee point of CTE changes sharply at $V_{TG} = 2$ V. The thermal emission effect will help the electrons overcome the barrier to transfer to FD at lower the barrier. Although the

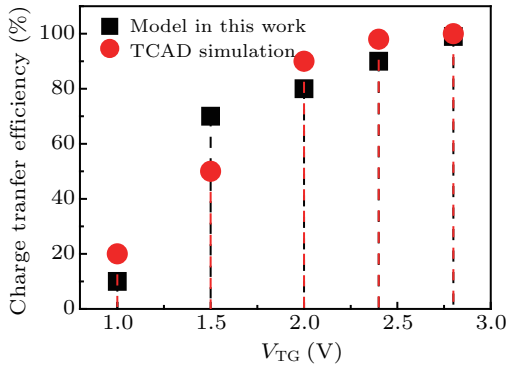


Fig. 7. The trend of charge transfer efficiency versus V_{TG}.

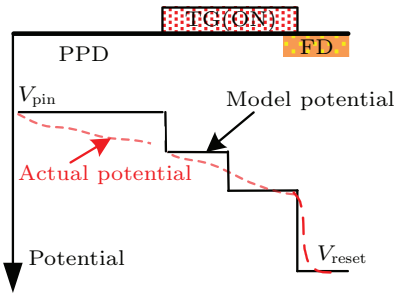


Fig. 8. Equivalent potential distribution condition of MOS-based model and TCAD simulation.

specific value and knee point are not well matched, this model can reflect the trend of changing.

4.3. Modeling the transient variation of V_{PPD} by different light power

The V_{PPD} is a physical parameter inside the device, which cannot be directly characterized by real-time testing, therefore, it is necessary to do the transient photoelectric simulation by TCAD to directly characterize the variation of V_{PPD}, which can also well verify the correctness of model. The TCAD simulations adopt the same timing as Fig. 6 to compare with MOS-based model results. The voltage variation of V_{PPD} in integration time interval (2.8 μs to 12.5 μs) is shown in Fig. 9. Three typical cases of light power were selected to compare the fitting between TCAD and model simulation data. The best fitting has been obtained with small light power ($V_{Power} = 0.005$ W/cm^2) as shown in red line and circle makers in Fig. 9. In the photocurrent model,[21] the total current (I_{total}) contribution at PPD node is given as

$$I_{total} = I_{ph} - I_{sub_TG} - I_f. \tag{4}$$

The I_{total} will decrease as V_{PPD} decreases, and this mainly due to the PPD gets forward biased and forward current (I_f) and subthreshold current (I_{sub_TG}) will increase. In this work, the influence of V_{PPD} on the total current is temporarily ignored to simplify the photocurrent model, so, the total current contribution is only made up of I_{ph}. Therefore, when the light is off (time = 10 μs), the model will show a greater variation in VPPD than TCAD simulations as shown in black and blue lines ($V_{Power} = 0.02$ W/cm^2, 0.08 W/cm^2) in Fig. 9. And the reverse trend of V_{PPD} increase can be observed in blue lines ($V_{Power} = 0.08$ W/cm^2) mainly because of I_{sub_TG}. More specifically, when the light intensity increases, the number of integrated electrons in PPD increases, which will reduce the potential barrier from PPD to TG. So, the thermionic emission will become more significant. Additionally, I_{sub_TG} will also include the current due to the feed forward effect when V_{PPD} is smaller. As a result, the variation trend of V_{PPD} in the model can match better with TCAD simulation even there will be some deviations occur due to the subthreshold current. And future work will consider the total current more detailed.

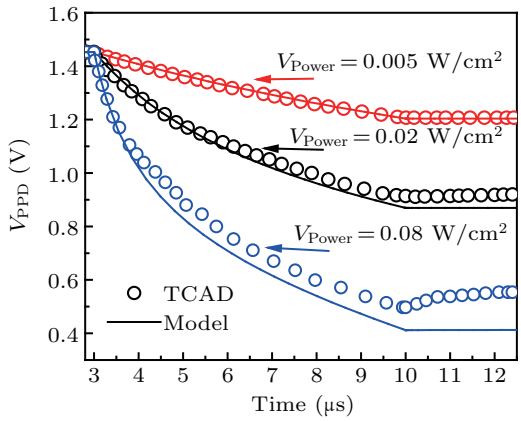


Fig. 9. The V_{PPD} as function of integration time for three different light power. Circle markers represent TCAD simulation data and solid lines represent model simulation data.

4.4. Modeling the variation of V_{FD} by test verification

As shown in Fig. 10, the effectiveness of the MOS-based model is verified by the testbench. The light source is an integrating sphere with a 905 nm laser diode, and the measurement-control system is based on Xilinx's Kintex-7. The test circuitry consists of a standard 4T-APS with a PPD with 3 μm pixel, and the W/L of the TG is 1.0 μm/0.6 μm. VDD_RST is fixed to 2.8 V, which is used to reset the FD and PPD regions to a higher potential level. The global analog buffer circuit is used to read out the signals under the test environment temperature of 300 K. The test timing is as same as Fig. 6 and the results of the FD voltage are shown in Fig. 11. Without any light after reset, the FD voltage rises to a high level. Both in the model and TCAD, the FD node is reset to 2.8 V, and the V_{FD} of test pixel is 1.82 V due to the source follower (SF). The threshold voltage of SF is adjusted to be 0.4 V in this work. The FD voltage decreases when the reset signal is off because of the charge injection effect, however, lager V_{FD} variation was observed in measurement. This mainly caused by the parasitic coupling of wire. FD node is very sensitive as read-out node in 4T structure, and moreover, the capacitance of FD is only 2 fF in this work. Therefore, the clock feed through effect of parasitic capacitance will cause V_{FD} to decrease greatly after reset in the measurement data curve. In the meantime, the same phenomenon and trend were observed during CDS reset period. When PPD is integrated by a 905 nm laser diode for 7 μs, there is a slight drop of V_{FD} in measurement and TCAD curve due to the subthreshold leakage and direct photogenic effect of FD node. When the TG is on again after integration, one part of electrons will transfer directly from PPD to FD, resulting in the drop of V_{FD}, and the other part of electrons will be stored under the TG gate as inversion layer electrons. This part of electrons will be released again to FD node when TG is turned off. The two parts of the signal electrons constitute the signal change of V_{FD}. As shown in Fig. 9, the variation of V_{FD} in measurement is smaller than TCAD and the model, it is understandable because the light power intensity can not be calibrated and match with the model well. All these behaviors trend can be obtained by using the circuit simulation based on the proposed model, TCAD and measurement, demonstrating the effectiveness of our approach.

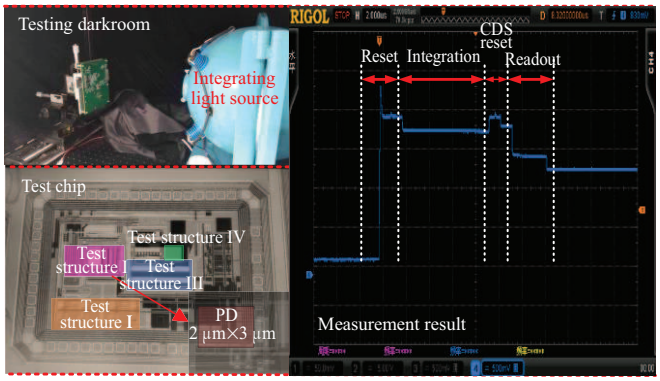


Fig. 10. Test platform and test structure of test chip diagram.

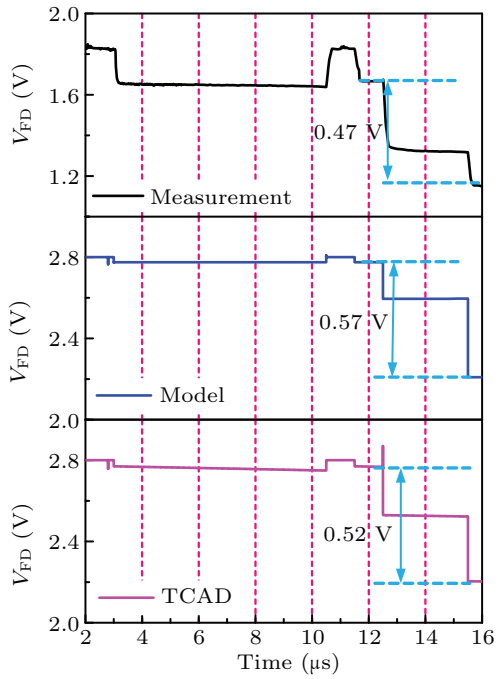


Fig. 11. Test curves of V_{FD} as function of integration time. TCAD and the proposed model simulations are compared together.

During the process simulation, the Monte Carlo implantation model is used. The doping-dependent mobility models, Shockley–Read–Hall model, Auger recombination model, Fermi–Dirac statistics optical generation model and compact SPICE model are activated in Sdevice simulation. The mesh number (about 100000) and minimum mesh size (2 nm) are optimized for simulations. The hybrid simulation of 4T-APS in TCAD usually takes about one day in this work. However, the MOS-based model can characteristics the function of nonuniform doping of TGs in suppressing charge injection back to PPDs like TCAD simulation with a few minutes. So, compared with the hybrid simulation in TCAD and the

Verilog-A simulation in SPICE, this model has higher simulation efficiency and accuracy, respectively.

5. Conclusions

A combined MOS-based model has been developed by considering the variable capacitance characteristics of PPD and the nonuniform doping in the TG channel. The SPICE simulation conclusion of this model was verified by TCAD simulations and test results. The charge transfer process of photogenerated electrons from PPD to FD was analyzed and the function of nonuniform TG doping in suppressing charge injection back to PPD was studied. The proposed model characterizes current and capacitance characteristics of the TG source terminal correctly. As a result, SPICE simulations can be successfully performed by combining all the physical characteristics of the PPD and TG, giving an effective evaluation mechanism for hybrid optoelectronic processes. In addition, with the help of the model, pixel design can be rapidly iterated to match the system design. This model introduces the possibility of system-level simulation in the design of low-illumination and low-noise-response CIS and high-speed modulation of the time of flight (TOF) pixels. Future work will consider the quantitative analysis of the overlapping potential barrier, total current, gate voltage, and threshold voltage for TGs more detailed.

Acknowledgements

Project supported by the National Natural Science Foundation of China (Grant No. 61874085) and the Postdoctoral Research Funding Project of Shaanxi Province, China (Grant No. 2018BSHEDZZ41).

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