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Impact of symmetric gate-recess length on the DC and RF characteristics of InP HEMTs

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We fabricated a set of symmetric gate-recess devices with gate length of 70 nm. We kept the source-to-drain spacing (L_{SD}) unchanged, and obtained a group of devices with gate-recess length (L_{recess}) from 0.4 μm to 0.8 μm through process improvement. In order to suppress the influence of the kink effect, we have done SiN_X passivation treatment. The maximum saturation current density (I_{D_max}) and maximum transconductance ($g_{m,max}$) increase as L_{recess} decreases to 0.4 μm. At this time, the device shows $I_{D_max} = 749.6$ mA/mm at $V_{GS} = 0.2$ V, $V_{DS} = 1.5$ V, and $g_{m_max} = 1111$ mS/mm at $V_{GS} = -0.35$ V, $V_{DS} = 1.5$ V. Meanwhile, as L_{recess} increases, it causes parasitic capacitance C_{gd} and g_d to decrease, making f_{max} drastically increases. When $L_{recess} = 0.8$ μm, the device shows $f_T = 188$ GHz and $f_{max} = 1112$ GHz.

Keywords: InP HEMT, InGaAs/InAlAs, current gain cut-off frequency (f_T), maximum oscillation frequency (f_{max}), gate-recess length (L_{recess})

PACS: 85.30.Tv, 73.40.Qv, 85.30.–z **DOI:** 10.1088/1674-1056/ac364d

1. Introduction

InP-based high electron mobility transistors (HEMTs) are considered as one of the most competitive semiconductor devices for millimeter and terahertz monolithic integrated circuits because of their low noise, low power consumption, and high gain performance.[1–5] In InP-based HEMTs, a source-to-drain spacing (L_{SD}) plays a critical role in both DC and RF performance. Changing L_{SD} will affect the source–drain resistance of the devices, as well as the parasitic capacitance of the gate–source–gate–drain, thereby affecting the DC and RF performance of the devices. Cha *et al.*[6] reported that the smaller L_{SD} resulted in a worse maximum drain current density (I_{D_max}). Recently, Yun *et al.*[7] reported that both the DC and RF responses of these devices were improved as the L_{SD} scaled down to 0.8 μm.

The L_{SD} is composed of the cap layer length (L_{capped}) and the gate-recess length (L_{recess}). Therefore, the change of L_{SD} is essentially a compromise between the cap layer length and the gate-recess length (L_{recess}). Takahashi *et al.*[8] reported that the f_{max} improved significantly by extending the drain-side gate-recess length (L_{RD}) to 250 nm; meanwhile, the source-side gate-recess length (L_{RS}) was kept to 70 nm; Shinohara *et al.*[9] reported that the asymmetric recess technique is one of the effective solutions to achieve a higher f_{max} since a longer L_{RD} results in much reduced g_d and C_{gd}/C_{gs}. Kim *et al.*[10] reported that they improved short-channel effects through widening of the side-recess spacing (L_{side}) to 150 nm, as well as reducing parasitic source and drain resistances. Shinohara *et al.*[11] reported that the f_T decreases with increasing L_{RS}. This variation can be explained by the increase in the source resistance (R_S) due to the spread of the highly resistive recessed region. In these reports, it is confirmed that the variation of the gate-recess length (L_{recess}) has a significant impact on the characteristics of the devices. On this basis, we want to further study the impact of changing the gate-recess length (L_{recess}) on the performance of the devices when the L_{SD} remains unchanged.

In this work, we fabricated a set of symmetric gate-recess devices with gate length of 70 nm while maintaining the length of source–drain metal and gate length (L_g) constant. By controlling the L_{SD} unchanged, we study the impact of different symmetric gate-recess length (L_{recess}) on the DC and RF performance of the devices.

2. Experiment

The schematic illustration of the cross-section of the InP-based HEMTs is shown in the following Fig. 1. The epitaxial layers of the devices were grown by gas source molecular beam epitaxy (GSMBE) on 3-inch (1 inch = 2.54 cm) semi-insulating InP (100) substrates. From bottom to top, the layers consist of a 500-nm $In_{0.52}Al_{0.48}As$ buffer layer, 10-nm $In_{0.53}Ga_{0.47}As$ channel layer, 3-nm unstrained $In_{0.52}Al_{0.48}As$ spacer layer, Si delta doping layer with 5×10^{12} cm^{-2} doping concentration, 8-nm unstrained $In_{0.52}Al_{0.48}As$ Schot-

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tky barrier layer, 4-nm InP etch-stop layer and Si-doped $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ (10/15/15 nm) composite capping layers. Hall measurements were made at room temperature, showing a carrier mobility of over 12000 $cm^2/(V{\cdot}s)$.

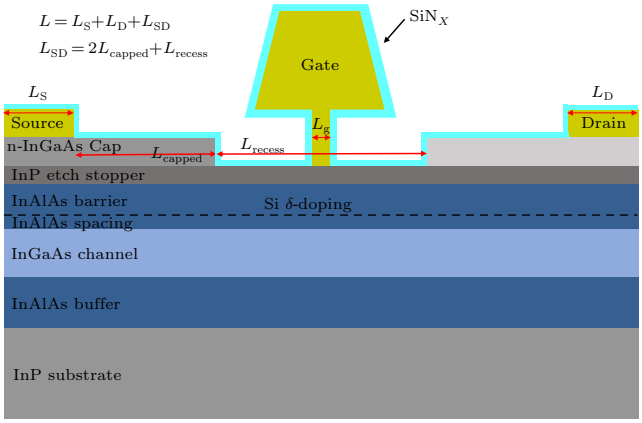


Fig. 1. Schematic diagram of cross-section of InP-based HEMTs.

The fabrication process of InP HEMTs mainly contains six steps, including mesa isolation, Ohmic contact formation, gate-recess, T-gates, passivation, and connection pads, which is similar to our previous reported devices.[12,13]

Firstly, isolating mesa was formed by means of phosphorus acid-based wet chemical etching. Next, source and drain were spaced 2.4 μm through a lithography process, followed by Ti/Pt/Au (15/15/50 nm) evaporated to satisfy the requirement of Ohmic contact by electron beam evaporation without annealing, with contact resistance measured to be 0.023 Ω·mm and the specific contact resistivity 8.75×10^{-8} Ω·cm^2 by TLM method.[14,15]

Afterward, gate-recesses with various width were formed by a novel technology, as shown in Fig. 2. A SiO_2 layer which was used as hard mask was deposited by PECVD. Then the gate-recesses were defined by electronic beam lithography (EBL) with a ZEP520A e-beam resist layer, and SiO_2 layer was etched by RIE, as shown in Fig. 2(a). And then the T-gates were defined by EBL with a ZEP/PMGI/ZEP (200/500/200 nm) e-beam resist stack. The top ZEP was exposed by a small dose and wide line and developed by a methyl isobutyl ketone (MIBK): 2-butanone (MEK) solution to determine the gate cap, the PMGI was etched by TMAH, and the bottom ZEP was exposed by a big dose and narrow line, then developed by N, N-dimethylacetamide to define the gate foot. And then the cap layers were etched by a phosphate-based solution to form the gate-recesses. As the adhesiveness of the InGaAs surface to ZEP is rather weaker than that to SiO_2, the cap layer beyond the SiO_2 hard mask could be etched absolutely, as a result, the width of the gate-recess could be controlled by the opening size of the SiO_2 layer. After the formation of the gate-recess, a Ti/Pt/Au (3/25/300 nm) metal stack was evaporated and lifted off, as shown in Fig. 2(b).

Finally, the SiO_2 hard mask was removed by HF solution and the devices were passivated by a 20-nm SiN_x layer, and then the Ti/Au (15/300 nm) connection pads were evaporated for on-wafer DC and RF characteristics measurements, as shown in Fig. 2(c). The scanning electron microscope (SEM) images of the present InP HEMT devices with various L_{recess} are shown in Fig. 3.

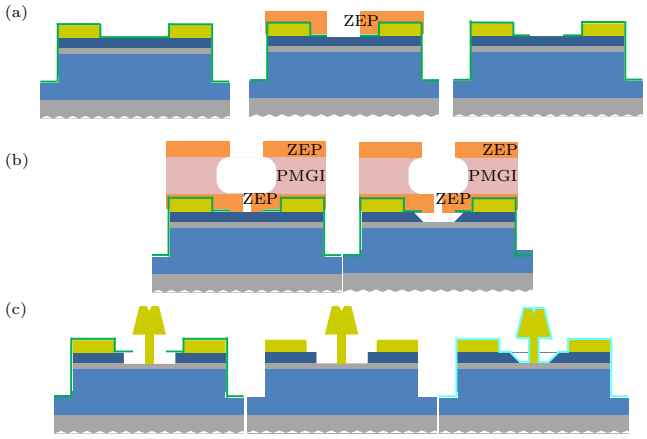


Fig. 2. A novel gate-recess technology of InP HEMTs.

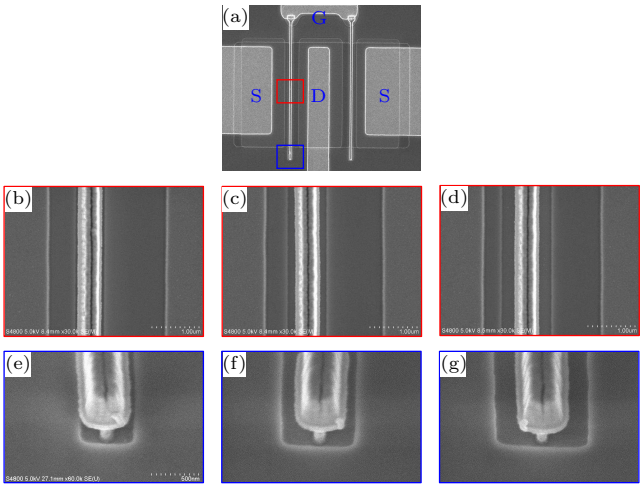


Fig. 3. SEM images of the present InP HEMT devices with various L_{recess}. (a) InP HEMT device, [(b) and (e)] $L_{recess} = 0.4$ μm, [(c) and (f)] $L_{recess} = 0.6$ μm, [(d) and (g)] $L_{recess} = 0.8$ μm.

3. Results and discussion

To study the impact of symmetric gate-recess length (L_{recess}), the DC and RF characteristics of InGaAs/InAlAs HEMTs were characterized by HP4142 semiconducter parameter analyzer and Agilent E8363B PNA vector network analyzer from 0.1 GHz to 40 GHz at room temperature. After the measurement, the *S*-parameters were extracted and studied.

3.1. DC characteristics

Figure 4 shows three sets of current–voltage (I_D–V_{DS}) curves of InGaAs/InAlAs HEMTs. The devices have various L_{recess} of 0.4 μm, 0.6 μm, 0.8 μm and a T-shaped W_g of 2×50 μm. The devices exhibited excellent pinch-off and current saturation characteristics up to $V_{DS} = 1.5$ V. Kink effect is

well suppressed due to the SiN_X passivation and InP etch stopper of devices. And it gets a maximum drain current density (I_{D_max}) of 749.6 mA/mm which is achieved at $V_{GS} = 0.2$ V and $V_{DS} = 1.5$ V. As L_{recess} down to 0.4 μm, there is an increase in the maximum drain current density. And the device with a shorter L_{recess} has a lower value of the on-resistance (R_{ON}). According to Ref. [16], R_{recess} is 2.3 times larger than R_{capped}. In this work, we keep an invariant L_{SD}. When L_{recess} increases from 0.4 μm to 0.8 μm, it is believed that both R_S and R_D increase, which is also confirmed in the parameter extraction results of R_S and R_D in Table 1. So the lower R_{ON} is mostly due to reduction of R_S and R_D with an invariant L_{SD}.

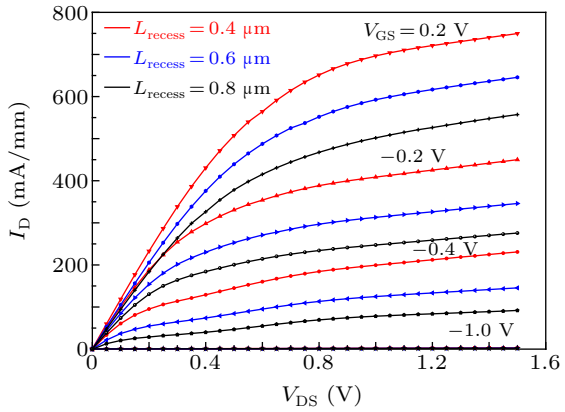


Fig. 4. Output characteristics of InP HEMTs with various L_{recess} (L_{recess} = 0.4, 0.6, and 0.8 μm).

Figure 5 plots the extrinsic transconductance (g_m) characteristics at $V_{DS} = 1.5$ V. The devices exhibit a continuously increasing g_m with L_{recess} down to 0.4 μm. According to Eq. (1), it can be explained by the decrease of R_S. The maximum transconductance ($g_{m,max}$) increases from 941.4 mS/mm at $V_{GS} = -0.25$ V to 1111 mS/mm at $V_{GS} = -0.35$ V.

$$g_m = \frac{g_{m,int}}{1 + R_S \cdot g_{m,int}}, \tag{1}$$

where $g_{m,int}$ is the value of g_m for the core part of HEMTs without any parasitic resistances and capacitances. And R_S is the parasitic resistances of source respectively.

Figure 6 plots the transfer characteristics. The drain–source voltage (V_{DS}) is increased from 1.0 V to 1.5 V with step of +0.1 V. A positive threshold voltage (V_{th}) shift is observed as L_{recess} increases. It can be explained the electron density in the channel of the side-etched region is reduced by surface depletion caused by surface states.[17] Generally, the electron density in side-etched region becomes smaller as the threshold voltage (V_{th}) of the HEMT's increases.

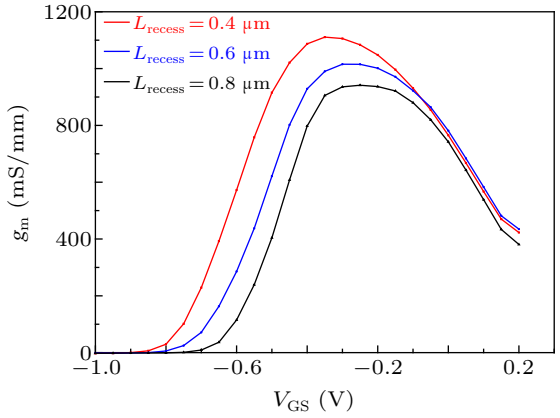


Fig. 5. The extrinsic transconductance (g_m) characteristics for InP HEMTs with various L_{recess} at $V_{DS} = 1.5$ V (L_{recess} = 0.4, 0.6, and 0.8 μm).

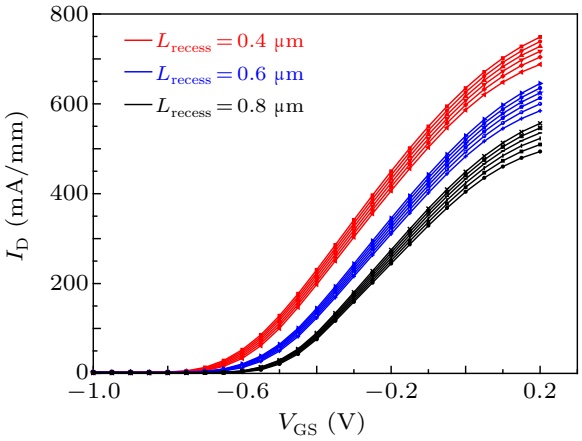


Fig. 6. The transfer characteristics for InP HEMTs with various L_{recess} (L_{recess} = 0.4, 0.6, and 0.8 μm).

3.2. RF characteristics

The devices were measured using on-wafer open and short patterns to subtract pad capacitances and inductances from the measured device S parameters, as shown in Ref. [18]. Figure 7 shows a measured current gain (H_{21}), maximum available gain, and maximum stable gain (MAG/MSG), and Mason's unilateral gain (U) against frequency for all devices with L_{recess} = 0.4, 0.6, and 0.8 μm. The bias condition was at $V_{DS} = 1.5$ V, $V_{GS} = -0.2$ V. The cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) were obtained by extrapolating the curve of H_{21} followed by a slope of −20 dB/dec and U followed by a slope of −20 dB/dec. The extrapolated f_T and f_{max} are 188 GHz and 1112 GHz at $L_{recess} = 0.8$ μm, 207 GHz, and 723 GHz at $L_{recess} = 0.6$ μm, 230 GHz, and 555 GHz at $L_{recess} = 0.4$ μm.

The f_T and f_{max} are expressed as follows:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)\left[1 + g_{ds}\left(R_s + R_d\right)\right] + C_{gd} \cdot g_m\left(R_s + R_d\right)}, \tag{2}$$

$$f_{max} = \frac{f_T}{\sqrt{4g_{ds}\left(R_g + R_i + R_s\right) + \dfrac{2C_{gd}}{C_{gs}}\left(\dfrac{C_{gd}}{C_{gs}} + g_m\left(R_i + R_s\right)\right)}}, \tag{3}$$

where C_{gs} is the parasitic capacitance from gate to source, C_{gd} is the parasitic capacitance from gate to drain, and R_g, R_D, and R_S are the parasitic resistances of gate, drain, and source respectively. The g_m is the extrinsic transconductance and the g_d is conductance between the drain and the source.

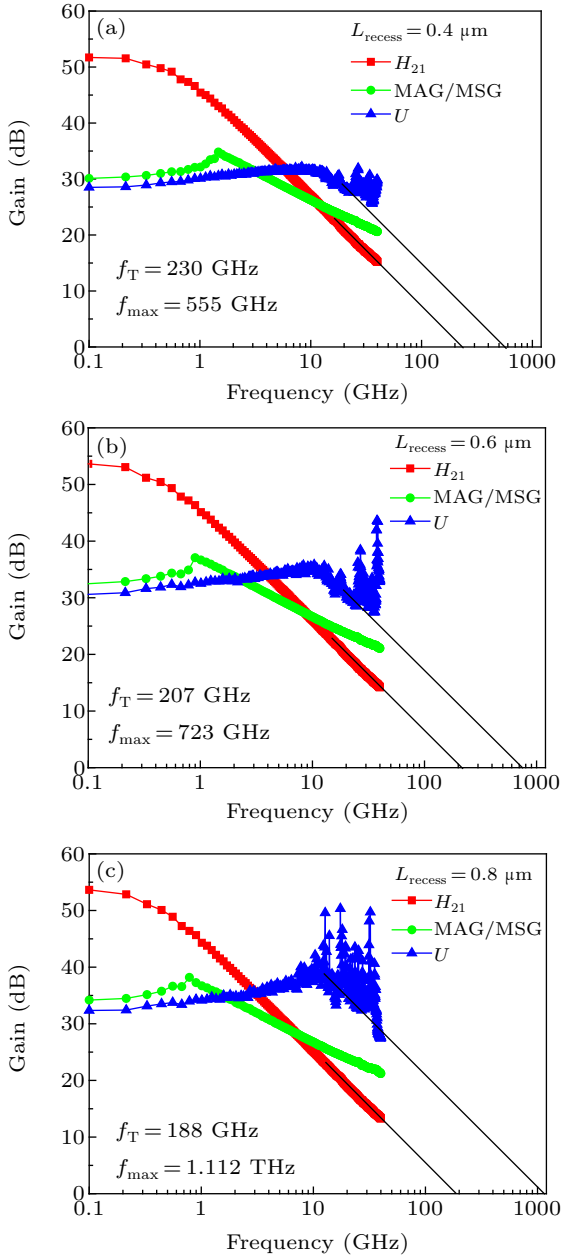


Fig. 7. The measured H_{21}, MAG/MSG, and U gain *versus* frequency of the HEMT with various values of L_{recess} (0.4 μm, 0.6 μm, 0.8 μm) at $V_{GS} = -0.2$ V and $V_{DS} = 1.5$ V.

As shown in Fig. 8(a), f_T decreases with the increase of L_{recess}. Equation (2) shows that f_T has a positive correlation with g_m. And the f_T would be good because of the high g_m. According to the results of C_{gd} parameter extraction in Table 1 and Fig. 8(b), as L_{recess} increases, C_{gd} gradually decreases. This is because L_{recess} increases, leading to a decrease in L_{capped}. Therefore, the spacing between the cap layer and the gate increases, C_{gd} gradually decreases. At the same time, Table 1 also shows that R_S and R_D increase with the increase of L_{recess}. So we believe that in this work, changing the value of L_{recess} makes the change of R_S and R_D having a greater impact on f_T than the change of parasitic capacitance C_{gd}.

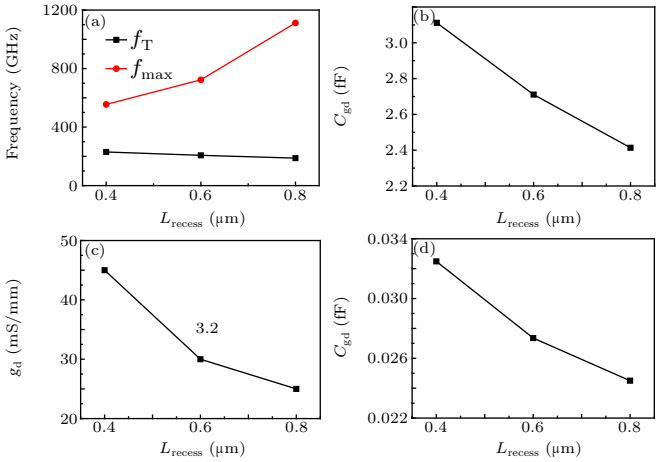


Fig. 8. Dependence of f_T, C_{gd}, g_d, and C_{gd}/C_{gs} on L_{recess} for InP HEMTs.

Although the smaller L_{recess} increases f_T, figures 8(b)–8(d) show that C_{gd}, g_d, and C_{gs}/C_{gd} decrease with the increase of L_{recess}, which is why the larger L_{recess} obtains the highest f_{max}. Since a large L_{recess} leads to a decrease in g_d and C_{gs}/C_{gd}, increasing L_{recess} can achieve an increase in f_{max}. This is because the increase in L_{recess} makes the gate–drain electric field weaker, thereby suppressing impact ionization.[9] Table 1 summarizes the small-signal modeling parameters for the devices with different L_{recess}, such as C_{gs}, C_{gd}, g_m, and g_d, based on our previous research.[19–21]

Table 1. The parameters of small signal equivalent circuit of devices.

L_{recess} (μm)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_S (Ω)	R_D (Ω)	R_g (Ω)	g_{ds} (mS)	g_m (mS)	f_T (GHz)	f_{max} (GHz)
0.4	95.8	3.1	25.3	1.72	4.02	5.78	45	1465	230	555
0.6	99.0	2.7	21.9	2.06	4.18	5.82	30	1330	207	723
0.8	98.5	2.4	19.8	2.49	4.35	5.79	25	1175	188	1112

Figure 9 shows the bias-dependent f_T and f_{max} for the devices with $L_{recess} = 0.8$ μm at $V_{DS} = 1.5$ V as a function of V_{GS}. It can be seen that f_T and f_{max} increase first and then decrease with the change of voltage V_{GS}. When $V_{GS} = -0.2$ V, f_T and f_{max} reach the maximum value, at this time f_{T_max} =188 GHz and $f_{max_max} = 1112$ GHz. Table 2 shows the reported InGaAs/InAlAs HEMT devices with f_{max} over 1.0 THz. By comparing these results, we need to further increase g_m and f_T while maintaining f_{max}.

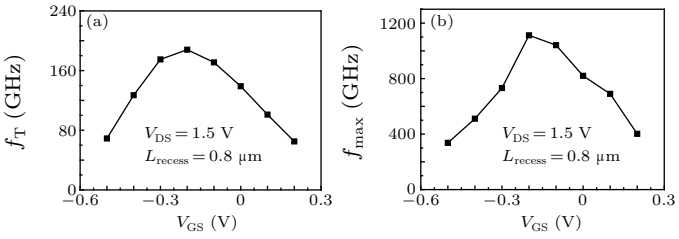


Fig. 9. The f_T and f_{max} for InP HEMTs with various V_{GS} at $V_{DS} = 1.5$ V.

Table 2. Comparison with published InGaAs(InAs)/InAlAs HEMTs with $f_{max} > 1.0$ THz.

Ref.	L_g (nm)	Channel/substrate	$g_{m.max}$ (mS/mm) (V_{DS} (V))	f_T (GHz) (V_{DS} (V))	f_{max} (GHz) (V_{DS} (V))
[22]	50	$In_{0.7}Ga_{0.3}As$/InP	1700 (0.5)	470 (0.75)	1080 (0.75)
[23]	20	InAs/GaAs	2850 (1.0)	320 (1.0)	1130 (1.0)
[24]	25	InAs/InP	3050 (1.0)	610 (1.2)	1500 (1.2)
[25]	75	$In_{0.7}Ga_{0.3}As$/InP	1900 (1.0)	250 (1.0)	1300 (1.0)
This work	70	$In_{0.53}Ga_{0.47}As$/InP	941.4 (1.5)	188 (1.5)	1112 (1.5)

4. Conclusion

In summary, a set of symmetric gate-recess InP HEMT devices with various L_{recess} were fabricated by a novel gate-recess technology. With the increase of L_{recess}, f_T decreases and f_{max} increases. When L_{recess} is 0.4 μm, the device has the maximum $f_T = 230$ GHz, as well as the maximum drain current density and transconductance. When L_{recess} is 0.8 μm, the device has a maximum $f_{max} = 1112$ GHz.

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