

A high rectification efficiency $Si_{0.14}Ge_{0.72}Sn_{0.14}$-$Ge_{0.82}Sn_{0.18}$-Ge quantum structure n-MOSFET for 2.45 GHz weak energy microwave wireless energy transmission

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A high rectification efficiency $Si_{0.14}Ge_{0.72}Sn_{0.14}$–$Ge_{0.82}Sn_{0.18}$–Ge quantum structure n-MOSFET for 2.45 GHz weak energy microwave wireless energy transmission

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The design strategy and efficiency optimization of a Ge-based n-type metal–oxide–semiconductor field-effect transistor (n-MOSFET) with a $Si_{0.14}Ge_{0.72}Sn_{0.14}$–$Ge_{0.82}Sn_{0.18}$–Ge quantum structure used for 2.45 GHz weak energy microwave wireless energy transmission is reported. The quantum structure combined with δ-doping technology is used to reduce the scattering of the device and improve its electron mobility; at the same time, the generation of surface channels is suppressed by the $Si_{0.14}Ge_{0.72}Sn_{0.14}$ cap layer. By adjusting the threshold voltage of the device to 91 mV, setting the device aspect ratio to 1 μm/0.4 μm and adopting a novel diode connection method, the rectification efficiency of the device is improved. With simulation by Silvaco TCAD software, good performance is displayed in the transfer and output characteristics. For a simple half-wave rectifier circuit with a load of 1 pf and 20 kΩ, the rectification efficiency of the device can reach 7.14% at an input power of −10 dBm, which is 4.2 times that of a Si MOSFET (with a threshold voltage of 80 mV) under the same conditions; this device shows a better rectification effect than a Si MOSFET in the range of −30 dBm to 6.9 dBm.

Keywords: microwave wireless energy transmission, quantum structure, GeSn, MOS rectification

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1. Introduction

In a microwave wireless energy transmission system (MWETS), power is transferred by radio frequency (RF) energy beams to give a direct current (DC) without a transmission line. Such a system can be used in wireless sensor networks and radio frequency identification systems as the power supply generator instead of using a wired power supply and battery.[1–3] The most important part of this system is the RF to DC voltage converter circuit (rectifier circuit) and the rectifier device is the core of the circuit. At present, popular rectifier devices are the Schottky diode and complementary metal–oxide–semiconductor (CMOS) devices. The advantages of a Schottky diode are its low turn-on voltage and the simple manufacturing process.[4] However, Schottky diodes are not compatible with the CMOS process and show a low rectification efficiency under weak energy conditions. In contrast, MOS devices can be integrated into a circuit using the mature CMOS process. However, due to the larger internal loss caused by the complexity of the structure compared with the Schottky diode, a special design is required to improve the rectification efficiency under weak energy conditions.

Current work is focused on the design and implementation of an optimized CMOS rectifier with good efficiency in a MWETS because of the compatibility of the bulk silicon process. However, most attention is paid to circuit optimization rather than improving the characteristics of the device. A review[5] has concluded that it is possible to design high-performance devices compatible with the CMOS process by changing materials such as Ge and setting a reasonable device structure.

Direct band gap germanium–tin (DR-$Ge_{1-x}Sn_x$) material has a higher electron mobility than Ge, and its band gap can be adjusted by changing the Sn content.[6–8] By adjusting the band gap of $Ge_{1-x}Sn_x$ and silicon–germanium–tin ($Si_yGe_{1-y-z}Sn_z$) to form a $Si_yGe_{1-y-z}Sn_z$/DR-$Ge_{1-x}Sn_x$/Ge quantum well structure, channel scattering can be reduced and the channel mobility of the device can be further improved.

Using the $Si_yGe_{1-y-z}Sn_z$/DR-$Ge_{1-x}Sn_x$/Ge quantum well structure as our basis, in this work we design a quantum structure n-MOS device that can be used for 2.45 GHz weak energy microwave wireless energy transmission. First, a $Si_yGe_{1-y-z}Sn_z$/DR-$Ge_{1-x}Sn_x$/Ge quantum structure n-MOS device is designed based on the characteristics of $Ge_{1-x}Sn_x$ materials. Then its threshold voltage and I–V characteristics are analyzed using simulation. Finally, a simple half-wave rectifier circuit is built using the mixed-mode mode of Silvaco TCAD software, and the rectification characteristics of the quantum structure device and the Si n-MOS device are compared.

2. The n-MOS design

The key to the design of a $Si_yGe_{1-y-z}Sn_z$/DR-$Ge_{1-x}Sn_x$/Ge quantum well structure for an n-MOS device is to adjust the content of Si and Sn in $Si_yGe_{1-y-z}Sn_z$ and the content of Sn in DR-$Ge_{1-x}Sn_x$ to form a deep band offset of

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the conduction band (ΔE_c). In this way, the electrons are confined in the quantum well (DR-$Ge_{1-x}Sn_x$ channel layer) and the influence of the surface cap layer is suppressed due to the Fermi pinning effect of the $Si_yGe_{1-y-z}Sn_z$ alloy with a high Ge content.

2.1. Physical design of layer structure material

The electron and hole mobilities of Ge material are superior to Si, and therefore it can be regarded as a substitute for Si. However, the disadvantage of Ge is that its band gap is narrow and its thermal stability is not as good as that of Si. At the same time, due to the Fermi pinning effect of Ge materials and the low activation concentration of n-type impurities, production of a Ge n-MOS can be problematic.[5]

Ge–Sn material has higher electron and hole mobilities than Ge. By adjusting the Sn doping, indirect band gap Ge–Sn can be converted to direct band gap Ge–Sn to improve the electron mobility. Also, the introduction of Si–Ge–Sn can allow formation of a heterojunction structure with Ge–Sn, making it possible to produce a Ge-based n-MOS device.

The band structure of $Ge_{1-x}Sn_x$ and $Si_yGe_{1-y-z}Sn_z$ materials[9,10] and their mobility characteristics[11] have been studied. Equation (1) shows the influence of the content of $Si_yGe_{1-y-z}Sn_z$ on the band gap[12–14]

$$\begin{aligned}\Delta E_{v,av}(Si_xGe_{1-x-y}Sn_y) &= -0.48x + 0.69y,\\ \Delta E_{so}(Si_xGe_{1-x-y}Sn_y) &= 0.295(1-x-y)\\ &\quad +0.043y + 0.800y,\\ E_{v,av}(Si_xGe_{1-x-y}Sn_y) &= \Delta E_{v,av}(Si_xGe_{1-x-y}Sn_y)\\ &\quad + \frac{\Delta E_{so}(Si_xGe_{1-x-y}Sn_y)}{3},\end{aligned} \tag{1}$$

where x and y are the contents of Si and Sn in $Si_yGe_{1-y-z}Sn_z$. $\Delta E_{v,av}(Si_xGe_{1-x-y}Sn_y)$ is the average valence band of $Si_yGe_{1-y-z}Sn_z$, with the average valence band of Ge as the reference. $\Delta E_{so}(Si_xGe_{1-x-y}Sn_y)$ is the spin coupling splitting value of $Si_xGe_{1-x-y}Sn_y$ and $E_{v,av}(Si_xGe_{1-x-y}Sn_y)$ is the top of valence band of $Si_yGe_{1-y-z}Sn_z$. In addition, the band gap of $Si_yGe_{1-y-z}Sn_z$ (or $Ge_{1-z}Sn_z$ for $y = 0$) varies with composition as shown below:

$$\begin{aligned}E_g(Si_xGe_{1-x-y}Sn_y) &= E_{gGe}(1-x-y) + E_{gSi}x + E_{gSn}y\\ &\quad - b_{GeSi}(1-x-y)x - b_{GeSn}(1-x-y)y - b_{SiSn}xy,\end{aligned} \tag{2}$$

where E_{gGe}, E_{gSi} and E_{gSn} are the band gaps of Ge, Si and Sn, respectively, and b_{GeSi}, b_{GeSn}, and b_{SiSn} are the band bowing parameters corresponding to Γ or L valleys which were calculated in Ref. [15]. The values are shown in Table 1.

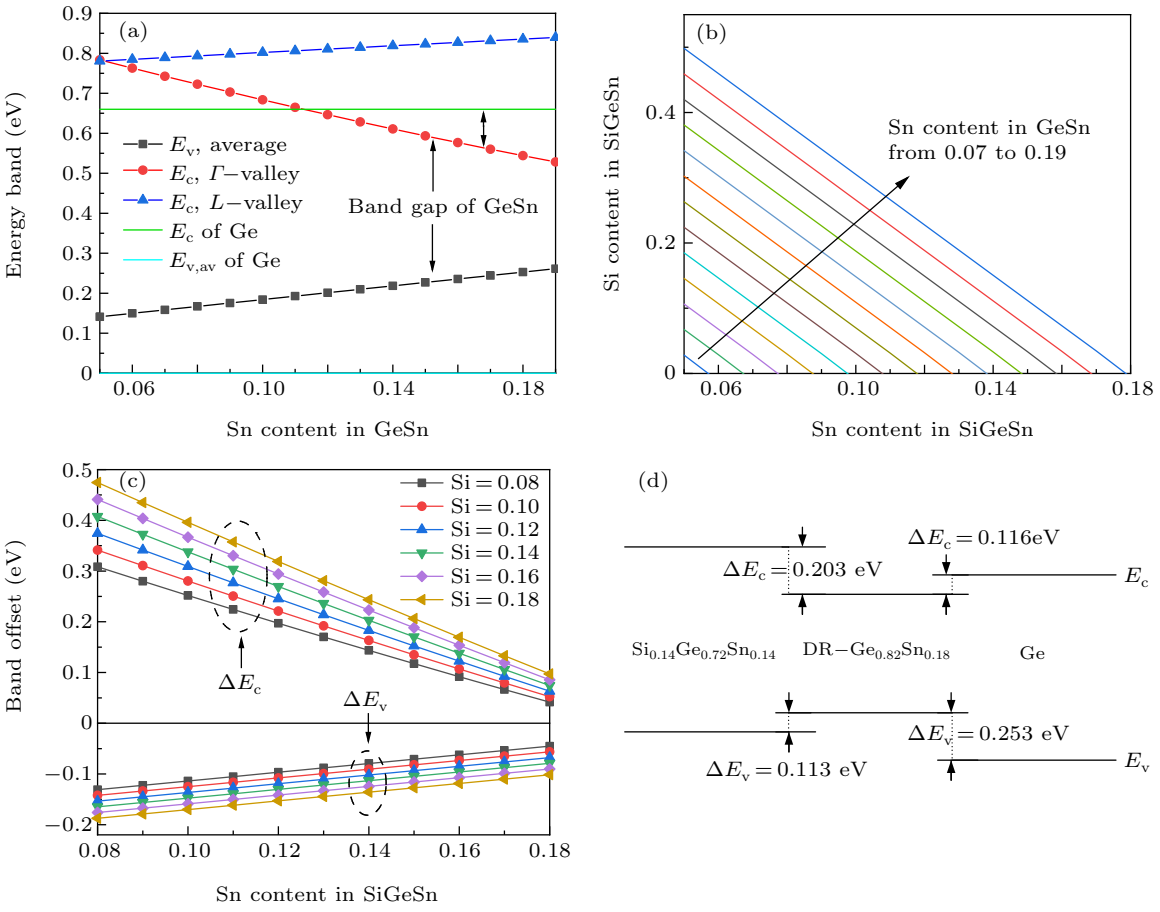


Fig. 1. (a) Variation of the energy band of $Ge_{1-x}Sn_x$ due to variation of the Sn content in $Ge_{1-x}Sn_x$ with the band of Ge as reference. (b) The Si and Sn contents in $Ge_{1-x}Sn_x$ and $Si_yGe_{1-y-z}Sn_z$ for the lattice matching between $Ge_{1-x}Sn_x$ and $Si_yGe_{1-y-z}Sn_z$. (c) The band offsets (ΔE_c and ΔE_v) between $Ge_{1-x}Sn_x$ and $Si_yGe_{1-y-z}Sn_z$. (d) Schematic diagram showing the band offsets (ΔE_c and ΔE_v) between $Si_yGe_{1-y-z}Sn_z$ and DR-$Ge_{1-x}Sn_x$ and between DR-$Ge_{1-x}Sn_x$ and Ge.

Table 1. Band gaps and bowing parameters for Ge, Si, and Sn and their alloys from Ref. [15].

	b_{GeSi}	b_{GeSn}	b_{SiSn}	E_{gGe}	E_{gSi}	E_{gSn}
L-valley	0	−0.11	0	0.66	2	0.14
Γ-valley	0.21	1.94	13.2	0.795	4.06	−0.413

The bottom of the conduction bands for $Ge_{1-x}Sn_x$ and $Si_yGe_{1-y-z}Sn_z$ can be deduced from the above relationships. On this basis, figure 1(a) shows the band structure of $Ge_{1-x}Sn_x$. The relationships between the lattice constants of $Ge_{1-x}Sn_x$ and $Si_yGe_{1-y-z}Sn_z$ are

$$a(Si_xGe_{1-x-y}Sn_y) = a_{Ge}(1-x-y) + a_{Si}x + a_{Sn}y, \quad (3)$$

where a is the lattice constant. Therefore, lattice matching between $Ge_{1-x}Sn_x$ and $Si_yGe_{1-y-z}Sn_z$ can be achieved by adjusting the content of $Si_yGe_{1-y-z}Sn_z$, as shown in Fig. 1(b). With increasing Sn content in $Ge_{1-x}Sn_x$, the proportional range of lattice-matched $Si_yGe_{1-y-z}Sn_z$ alloy is wider. Considering the requirement of ΔE_c for formation of a quantum well, it is appropriate to take the Sn content in $Ge_{1-x}Sn_x$ as 0.18, and the conduction band offset ΔE_c is 0.116 eV relative to the bottom of the conduction band for Ge.

The variation trend of the $Si_yGe_{1-y-z}Sn_z$–$Ge_{0.82}Sn_{0.18}$ band offset with $Si_yGe_{1-y-z}Sn_z$ composition is shown in Fig. 1(c). Considering lattice matching and band offset, $Si_{0.14}Ge_{0.72}Sn_{0.14}$ and $Ge_{0.82}Sn_{0.18}$ are used to form a $Si_{0.14}Ge_{0.72}Sn_{0.14}$–$Ge_{0.82}Sn_{0.18}$–Ge double heterojunction structure. As shown in Fig. 1(d), in the above structure ΔE_c between $Si_{0.14}Ge_{0.72}Sn_{0.14}$ and $Ge_{0.82}Sn_{0.18}$ is 0.203 eV and ΔE_v between them is 0.113 eV. Meanwhile, ΔE_c between Ge and $Ge_{0.82}Sn_{0.18}$ is 0.116 eV and ΔE_v between them is 0.253 eV. The above data show that a good quantum structure is formed.

2.2. Electron mobility calculation

The energy band structure of DR-$Ge_{1-x}Sn_x$ is different from that of Ge. The Sn composition makes the effective mass of this alloy smaller than that of Ge, so that its mobility is greatly improved relative to Ge. However, the solid solubility with a high Sn content will cause disordered scattering of the alloy, resulting in a decrease in mobility, and the proportion of Sn will also affect the mobility.[11] The formula for mobility calculation is

$$\mu_n = \frac{q\tau_n}{m_n^*}, \quad (4)$$

where μ_n is the electron mobility, m_n^* is the effective mass of the electron and τ_n is the electron mean free time. Considering that the electron scattering mechanism in DR-$Ge_{1-x}Sn_x$ is mainly ionized impurity scattering ($P_{e,//}$), acoustic phonon scattering ($P_{e,ac}$) and alloy disorder scattering ($P_{e,ad}$), the following relationships between scattering and electron mean free time are obtained:

$$P_{e,//} = \frac{1}{\tau_i}, \quad P_{e,ac} = \frac{1}{\tau_a}, \quad P_{e,ad} = \frac{1}{\tau_{ad}}. \quad (5)$$

Therefore, the electron mean free time is given by

$$\frac{1}{\tau_n} = \frac{1}{\tau_i} + \frac{1}{\tau_a} + \frac{1}{\tau_{ad}}. \quad (6)$$

Combining the above analysis and literature data,[11] the change in bulk material mobility with Sn composition can be calculated (Fig. 2). The electron mobility of bulk materials increases with increase in the Sn content, and its value is as high as 1.75×10^4 cm^2/(V·s) when $x = 0.18$. However, this is an ideal value. In actual devices, the energy band structure of the channel layer, the influence of the mobility between different energy valleys of $Ge_{1-x}Sn_x$ and the influence of the quantization effect in the device all need to be considered.[16] For DR-$Ge_{1-x}Sn_x$, limited Γ-valley occupied electronic energy rates and the impact of mobility in the L-valley cannot be ignored. Figure 2 also indicates that the average electron mobility and Γ-valley electron mobility of the device both increase with increase in the Sn content. From this figure, where $x = 0.18$, the average electron conductance mobility of the channel is about 1.67 times that of Ge, namely, 6333 cm^2/(V·s) as used in the simulation.

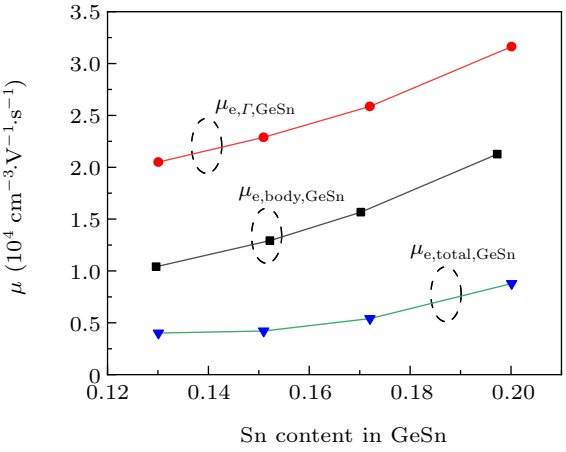


Fig. 2. Variation of bulk material mobility ($\mu_{e,body,GeSn}$)[11] and the average electron mobility ($\mu_{e,total,GeSn}$) and Γ-valley electron mobility ($\mu_{e,\Gamma,GeSn}$) of the device for DR-GeSn[16] with variation of the Sn content in $Ge_{1-x}Sn_x$.

2.3. Design of the device structure

At present, the research on quantum structure MOS devices is mostly focused on SiGe materials, rarely on GeSn materials. It is easy for parasitic channels to form with a Si cap layer on a quantum structure metal–oxide–semiconductor field-effect transistor (MOSFET). At the same time, due to the inherent characteristics of Ge, it is difficult for a P-type substrate to generate an N-type surface channel, so a high-performance Ge-based n-MOS is extremely difficult to manufacture. The quantum well structure described in this paper can effectively avoid these problems.

In this paper, the following quantum structure n-MOS device is designed based on the structure discussed in Subsection 2.1. With regard to process compatibility, a Ge epitaxial layer was deposited on a Si substrate, and a high-quality virtual Ge substrate was formed by laser recrystallization. The

channel and doping of the device are separated by depositing a δ-doping layer on the virtual substrate, and the scattering of ionized impurities is effectively reduced, thus improving the mobility. At the same time, the threshold voltage of the device can be adjusted by controlling the doping concentration of the doped layer. Then, the DR-$Ge_{0.82}Sn_{0.18}$ channel layer and the $Si_{0.14}Ge_{0.72}Sn_{0.14}$ cap layer are deposited, thus forming the $Si_{0.14}Ge_{0.72}Sn_{0.14}$–$Ge_{0.82}Sn_{0.18}$–Ge quantum structure. The channel carrier concentration can be controlled by the MOS structure on the top, thereby controlling whether the device is on or off. The Fermi pinning effect of the cap layer of high Ge content alloy $Si_{0.14}Ge_{0.72}Sn_{0.14}$ can be used to suppress the formation of surface parasitic channels to improve the performance of the device. Finally, Al or Ni is used to anneal the source and drain to form ohmic contacts. Figure 3 plots the structure of the above MOS device and shows parameters that will be used in the simulation.

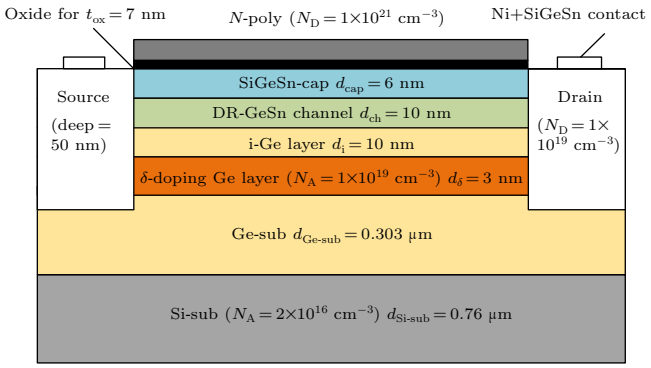


Fig. 3. A quantum structure n-MOS device with some key values for the simulation.

2.4. Simulation of band characteristics

To obtain the energy band characteristics of the device, simulations were performed using Silvaco TCAD software; the model structure is shown in Fig. 4. The entire device channel length is 400 nm, and some process technologies were not considered in order to simplify the analysis and improve the simulation speed. The vertical energy band image (for $x = 0$) is obtained by taking the oxide–cap interface as the reference interface. From Fig. 5(a), it can be seen that the bottom of the conduction band is bent at the cap–channel interface and the cap–oxide interface. Although the bottom of the conduction band at the cap–oxide interface is lower than that at the cap–channel interface, electrons do not accumulate at the surface due to the fact that high-Ge alloys are difficult to invert to form N-channels. As a result, electrons accumulate near the interface between the channel and the cap layer (closer to the $Ge_{0.82}Sn_{0.18}$ channel layer side) to form a conductive channel.

The diagram of the longitudinal distribution of the electron current density (Fig. 5(b)) also verifies the above analysis; it can be seen that the maximum electron current density in the vicinity of the channel and cap layer is 340000 A/cm^2 at a gate voltage of 2 V, while the electron current density at the top surface of the cap layer is less than 20000 A/cm^2, which is nearly 17 times smaller than the peak current density at the channel. On the one hand, this indicates that the device is indeed an n-MOS device and the vast majority of the electron current is confined inside the quantum well channel because the surface channel is suppressed. On the other hand, the intrinsic Ge layer isolates the dopant layer and the channel layer, thus avoiding any influence of the dopant layer on the electron current.

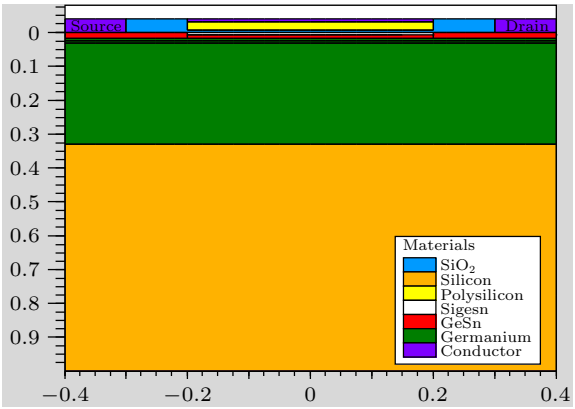


Fig. 4. The model structure used for simulation with Silvaco TCAD software.

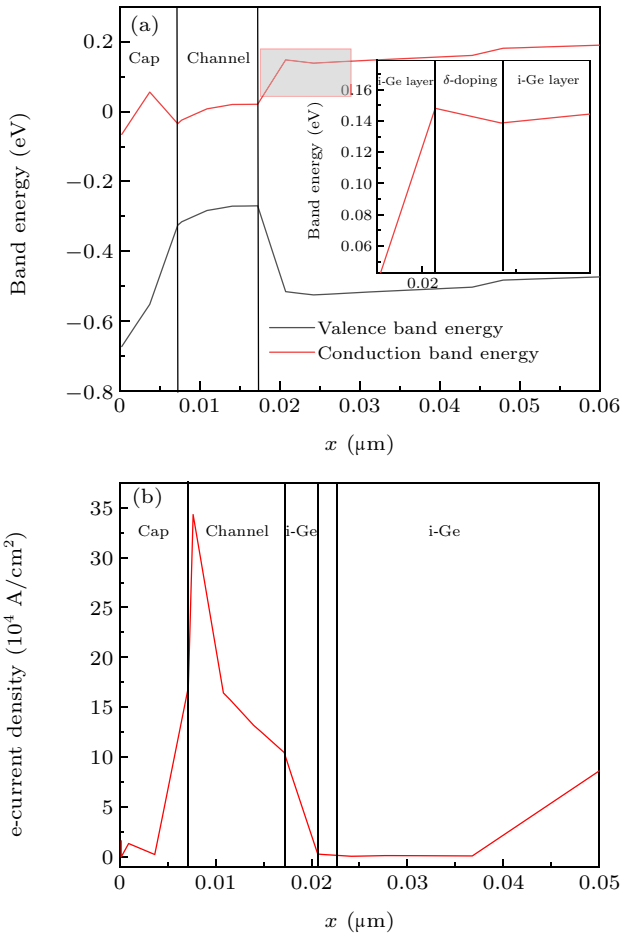


Fig. 5. (a) The vertical energy band image (for $y = 0$ μm) obtained by taking the oxide–cap interface as the reference interface (for x from 0 μm to 0.06 μm); details of the conduction band of doping layer are shown in the inset. (b) Longitudinal distribution of the electron current density in the same coordinate system as (a).

This is further verified by the two-dimensional device distribution of the electron current density with a 2 V gate voltage (Fig. 6), which clearly shows that the electrons are confined inside the quantum well with the peak close to the cap layer, and the current density gradually decreasing to both sides; it is therefore reasonable to place the dopant layer on the lower side of the channel layer and set the isolation and cap layer to reduce scattering. At the same time, the surface channel is also clearly suppressed. This fully demonstrates the superiority of the quantum well structure device. The structure of a Si MOS device is shown in Fig. 7 for comparison.

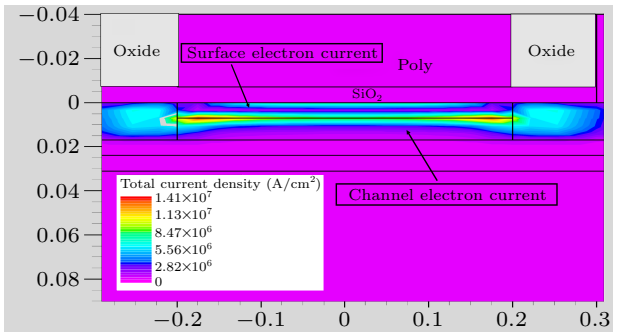


Fig. 6. The two-dimensional device distribution of the electron current density with a 2 V gate voltage, showing the surface electron current and the channel electron current.

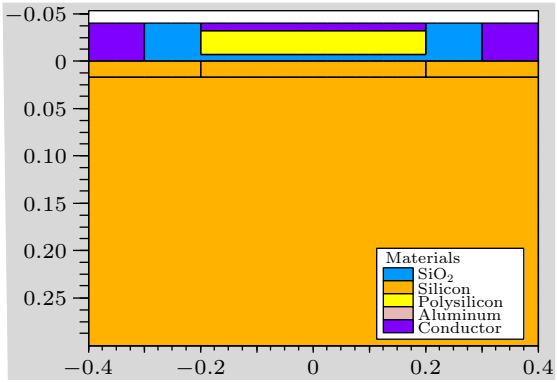


Fig. 7. Si MOS device structure used for comparison.

3. The n-MOS characterization

The quantum structure n-MOS mentioned in this paper is similar to bulk Si devices with the characteristics of both MOSFETs and modulation-doped field-effect transistors, and various small-signal models for quantum well devices are given in Refs. [17–20]. A small-signal model is considered in conjunction with the literature above and as shown in Fig. 8 for subsequent analysis. The device model is similar to a Si MOS device, with differences in threshold voltage and capacitance structure. For this quantum well structure, the threshold voltage of this device consists of the quantum well channel threshold voltage and the surface parasitic channel.[21–25] However, due to the SiGeSn cap layer having a high Ge content, the Fermi level is pinned at the interface between the cap layer and the oxide layer, making the surface parasitic channel threshold voltage much higher than the quantum well channel threshold voltage. In a weak energy density harvesting circuit the surface parasitic channel can be neglected because the gate voltage is low (much less than 1 V). In addition, unlike the MOS structure, the heterojunction capacitance between different epitaxial layers should be considered for this device in addition to the MOS gate oxide capacitance.

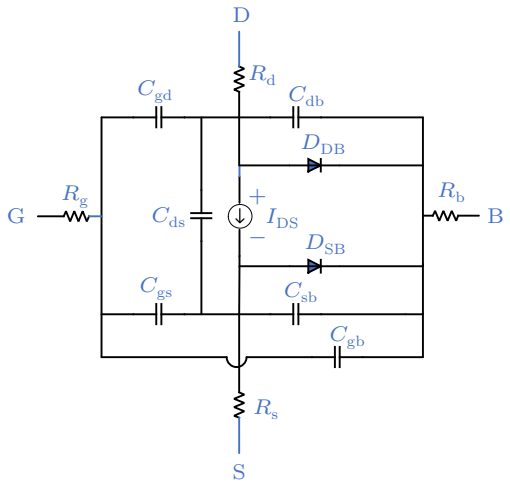


Fig. 8. A small signal model for the quantum well device discussed in this paper.

3.1. Threshold voltage calculation and simulation

For MOS devices, the threshold voltage is an important parameter whose value is related to the gate oxide thickness, the gate electrode work function and the device doping concentration. Also, for a diode connection MOSFET device used in rectification, it is effective to reduce the turn-on voltage (the threshold voltage of the MOS device) to improve the rectification efficiency. According to the literature,[2,3] the rectification efficiency of MOS devices can be improved by using very low threshold voltages. It is necessary to analyze the threshold voltage formula for the device. For a quantum structure device it is assumed that the δ-doped layer is fully depleted and the remaining charge required for the channel comes from the substrate layer.

Assuming that the charge density at the δ-doping layer is $Q_{\rm m}$, the relationships through each layer have the form of the Poisson equations[22,25] shown in Fig. 9, which are solved for when the gate voltage is lower than the threshold voltage to give the following equation:

$$\varphi_{\rm s} = -\frac{qN_{\rm B1}}{2\varepsilon_{\rm si}}\left[x_{\rm d}^2 + 2x_{\rm d}\left(t_{\rm i} + R_1 t_{\rm cha}\right)\right] + \frac{qQ_{\rm m}t_{\rm cap}}{\varepsilon_{\rm sigesn}}. \tag{7}$$

When $\varphi_{\rm s} = \varphi_{\rm th}$, we can calculate the maximum depletion layer width ($x_{\rm dm}$) by

$$x_{\rm dm} = \left[\frac{-2\varepsilon_{\rm si}\varphi_{\rm th}}{qN_{\rm B1}} + 2\frac{Q_{\rm m}}{N_{\rm B1}}\left(t_{\rm i} + R_1 t_{\rm cha}\right) + \left(t_{\rm i} + R_1 t_{\rm cha}\right)^2\right]^{1/2} - \left(t_{\rm i} + R_1 t_{\rm cha}\right), \tag{8}$$

where N_{B1} is the substrate doping concentration, R_1 is equated to $\varepsilon_{ge}/\varepsilon_{gesn}$ and ε_{ge}, ε_{gesn} and ε_{sigesn} are the material dielectric constants. For GeSn alloys with a high Ge content, R_1 is approximated as 1. Based on Eqs. (7) and (8), the threshold voltage for the n-MOS device in this paper is given by

$$V_{th0} = V_{FB} + \varphi_{th} - \frac{Q_{dp}}{C_1}. \tag{9}$$

For a flat-band voltage V_{FB}, the potential at the heterointerface φ_{th}, the equivalent charge Q_{dp} and capacitance C_1 above are related by

$$\varphi_{th} = 2\varphi_{fp} - \frac{\Delta E_C}{q} = 2\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{\Delta E_C}{q}, \tag{10}$$

$$Q_{dp} = qN_{B1}x_{dm} - qQ_m, \tag{11}$$

$$\frac{1}{C_1} = \frac{1}{C_{ox}} + \frac{1}{C_{cap}}, \tag{12}$$

where φ_{fp} is the Fermi potential, C_{ox} is the gate oxide capacitance and C_{cap} is the cap capacitance. The above equations solve for the channel threshold voltage, and it can be seen that the threshold voltage of the device introduces the conduction band offset ΔE_C and the heterojunction structure capacitance compared with the equation for calculating the threshold voltage of a Si MOS device. Therefore, according to the above equations, the threshold voltage can be adjusted by changing the process parameters such as layer structure parameters and the δ-doping layer concentration of the device.

0			
	$\frac{\partial^2\varphi}{\partial x^2} = 0$	for $0 \le x \le t_{ox}$	Oxide
t_{ox}			
	$\frac{\partial^2\varphi}{\partial x^2} = 0$	for $0 \le x \le t_{cap}$	Cap
t_{cap}			
	$V_G \le V_{th0}: \frac{\partial^2\varphi}{\partial x^2} = 0$		Channel
	$V_G \ge V_{th0}: \frac{\partial^2\varphi}{\partial x^2} = -\frac{qN_B}{\varepsilon_{GeSn}}$	for $0 \le x \le t_{cha}$	
t_{cha}			
	$\frac{\partial^2\varphi}{\partial x^2} = 0$	for $0 \le x \le t_i$	i-Ge
t_i			
	$\frac{\partial^2\varphi}{\partial x^2} = -\frac{qN_{B2}}{\varepsilon_{Ge}}$	for $0 \le x \le t_\delta$	δ-doping
t_δ			
	$\frac{\partial^2\varphi}{\partial x^2} = -\frac{qN_{B1}}{\varepsilon_{Ge}}$		Ge-sub
x			

Fig. 9. Poisson equations for different layers in a quantum-structured n-MOS.

The variation of the threshold voltage of the device with the doping concentration of the doping layer is shown in Fig. 10(a) as an orange solid line. It is easy to observe from the figure that the threshold voltage of the device increases with increase in the P-type impurity doping concentration of the doped layer, and especially between 10^{18} cm^{-3} and 10^{19} cm^{-3}, mainly due to the increase in φ_{th} as shown in Eq. (10).

It can be seen from Fig. 10(a) that the variation of the threshold voltage with the thickness of cap layer is different from that of the other layers. The electron longitudinal current density diagram in Fig. 10(b) can explain this phenomenon. As the thickness of cap layer increases, the current density of the parasitic channel gradually increases, while the current density of the DR-GeSn channel gradually decreases; together these have an effect on the threshold voltage. When the thickness of cap layer increases to 10 nm, the peak electron current density of the cap layer is higher than the peak electron current density of the channel, which means that the threshold voltage is dominated by the cap layer and the cap layer parasitic channel opens before the quantum well channel. Notice that the sum of the electron current densities of the cap layer and quantum well channel at $t_{cap} = 1$ nm is much larger than that at 6 nm and 10 nm, which also explains why the threshold voltage is lower when the cap layer is extremely thin. Considering the process compatibility, it is more reasonable to take 6 nm as the cap layer thickness.

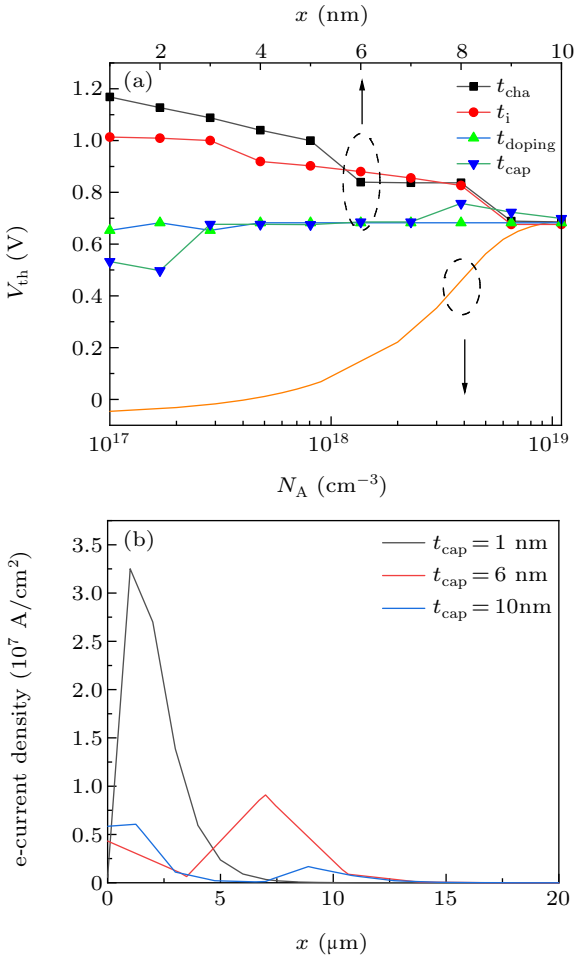


Fig. 10. The initial values for the two images: the thicknesses of the cap layer (t_{cap}), channel layer ($t_{channel}$), buffer layer (t_{buf}) and doping layer (t_{doping}) are 6 nm, 10 nm, 10 nm, and 3 nm, respectively, and the P-type impurity doping concentration of the doped layer (N_A) is 10^{19} cm^{-3}. (a) The orange solid line shows the variation of the device threshold voltage with the doping concentration of the doping layer and the dot and line graphs shows the influence of channel layer thickness, buffer layer thickness, dopant layer thickness and cap layer thickness, respectively, on the threshold voltage. (b) The electron longitudinal current density diagram for different cap layer thicknesses.

The influence of channel layer thickness, buffer layer thickness and dopant layer thickness on the threshold voltage is also shown in Fig. 10(a). As the channel layer thickness and buffer layer thickness increase, the threshold voltage gradually decreases, while the dopant layer thickness has less effect on the threshold voltage. A comprehensive analysis of the thickness parameters of each channel layer was shown in Fig. 7.

Comparison of Figs. 10(a) and 10(b) shows that the threshold voltage is more sensitive to the dopant layer concentration. Therefore, by adjusting the dopant layer concentration to 10^{18} cm^{-3}, a threshold voltage of 91 mV is obtained in order to improve the rectification efficiency of the device.

3.2. The *I*–*V* characteristics

The transfer and output characteristics of the device are shown in Figs. 11 and 12. The transfer characteristics at $V_{DS} = 0.1$ V for doping concentrations of 10^{19} cm^{-3} and 10^{18} cm^{-3}, respectively, are shown, and it can be seen that when $W/L = 1$ μm/0.4 μm, the current is up to the mA level at $V_g = 1$ V, which is an advantage of the high mobility due to the quantum wells. The threshold voltage varies at different doping concentrations, as can be seen at 10^{19} cm^{-3}, the curve shifts left relative to 10^{18} cm^{-3} and the threshold voltage decreases, which is beneficial for rectification applications. However, it also results in a larger leakage current and poorer subthreshold characteristics of the device. The output characteristics further demonstrate the excellent performance of the device and also show the effect of the channel length, which is very obvious when V_g is above 0.5 V.

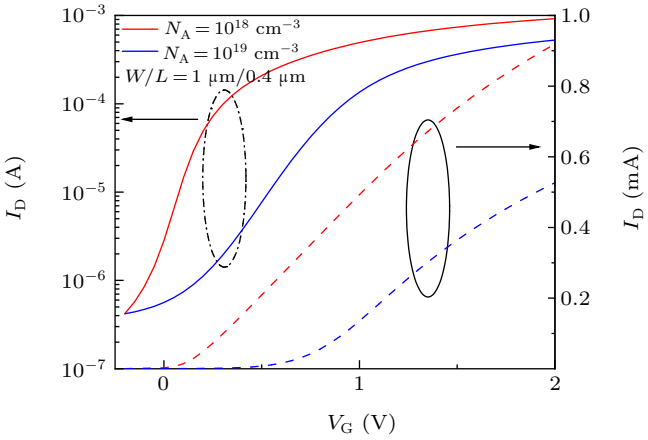


Fig. 11. Curves under the log (left) and normal (right) axes, respectively, illustrating the transfer characteristics at different doping concentrations. The device width (W) to length (L) ratio is set as 1 μm/0.4 μm.

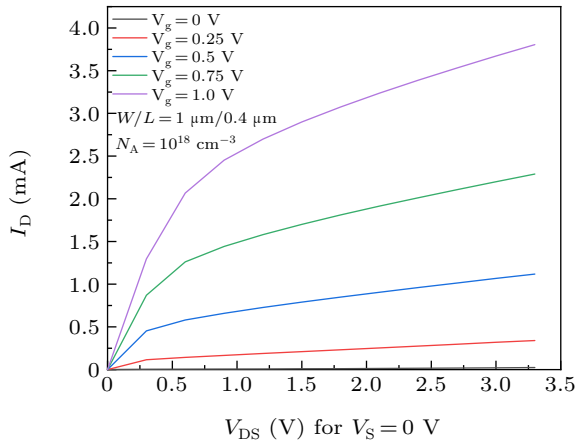


Fig. 12. The output characteristics of the gate voltage from 0 V to 1 V, where the concentration of the doping layer is 10^{18} cm^{-3} and the device size is the same as in Fig. 11.

4. Principles of rectifier circuit design and circuit simulation

In this paper, in order to analyze the effect of quantum channel devices on rectification and energy harvesting, a half-wave rectification circuit as in Fig. 13 is briefly considered. The device is connected like a diode, an AC current source with 50 Ω internal resistance is used as the power input, a load capacitor C_1 is used to stabilize the DC output waveform and the resistor R_1 is the output load.

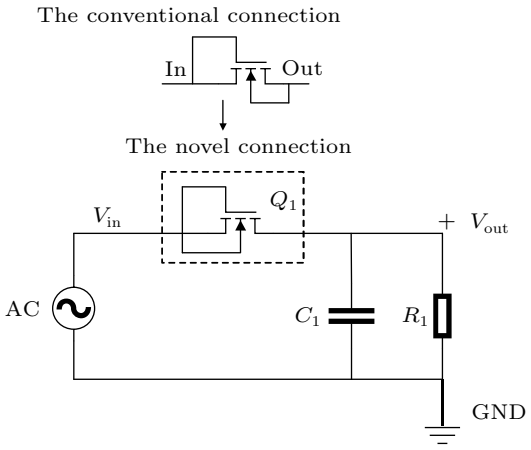


Fig. 13. Schematic diagram of the half-wave rectifier circuit for simulation.

There are two types of connections for a MOS used for rectification,[2,3] one is the conventional diode connection where the source and gate are connected as input and the source and substrate are connected as output and the other is the novel connection where the substrate, drain and gate are connected as input and the source is set as output. As the source and substrate potential of the novel connection is not zero, according to the threshold voltage Eq. (13), V_{SB} has a modulating effect on the threshold voltage. When a forward voltage is applied, which effectively reduces the forward turn-on voltage, the forward conduction current is greatly increased. When a reverse voltage is applied, the reverse leakage current is greatly reduced, helping to eliminate the problems of a high leakage current with a low threshold voltage, thus effectively improving the efficiency of the rectifier circuit[2]

$$V_{TH} = V_{th0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right). \quad (13)$$

Equation (13) still applies for the quantum structure device, where V_{th0} is the intrinsic threshold voltage described in Subsection 3.2 and Φ_F is the Fermi potential of the device herein.

4.1. DC simulation

Figure 14 compares the *I*–*V* curves of the two connection methods for the quantum structure MOS device (QS-MOS in the figure). It can be seen that in forward bias the two curves almost coincide in the 0 V–0.5 V interval, and the novel connection has a higher current in the region above 0.5 V. However, in reverse bias, the conventional connection has a significantly higher breakdown current than the new connection, with a difference of 177.2 times between them at −1 V for example. This shows that the substrate bias can effectively improve the subthreshold characteristics of the quantum structure device and greatly reduce the leakage current.

Also, comparing the Si MOS and the quantum structure device using the new connection method, the current of the quantum structure device is significantly larger than that of the Si MOS at forward bias in the figure. Although the leakage current of the Si MOS device is lower in the reverse bias case, indicating that the loss of rectification of this quantum structure device may be higher than that of the Si MOS device, the high current characteristic due to the high electron mobility makes the rectification effect of this device much better than that of the Si MOS.

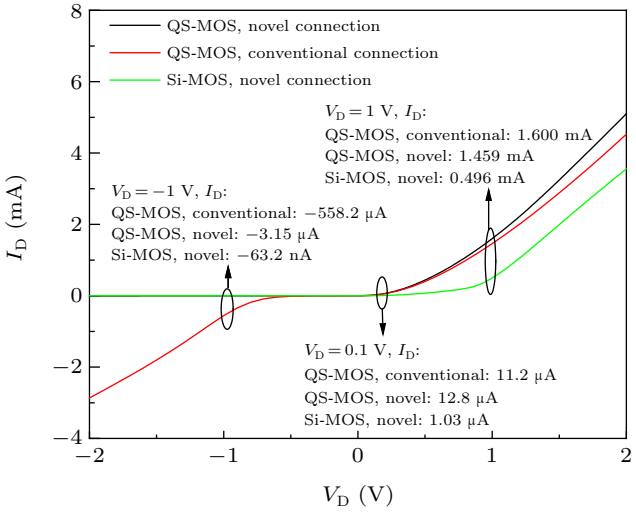


Fig. 14. The *I*–*V* curves of different devices and connection methods by DC simulation. QS-MOS is the quantum structure MOS device (V_{th0} = 91 mV) and Si–MOS is the Si MOS device (V_{th0} = 80 mV). The current values of each curve under three grid voltage conditions are marked in the figure for comparison.

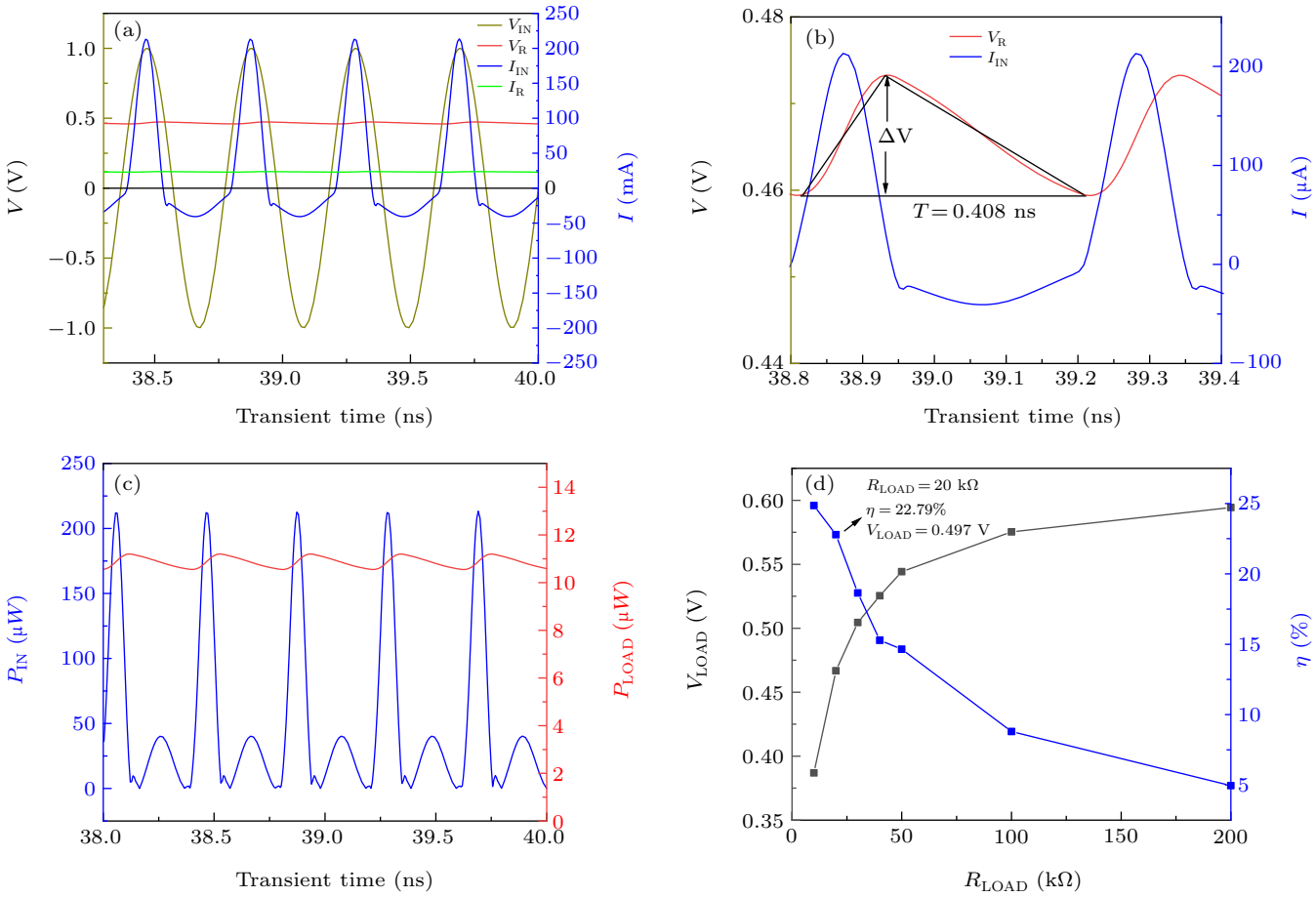


Fig. 15. (a) Stable current and voltage waveforms (from 38 ns to 40 ns) on the input and output sides obtained by transient simulations at $R = 20$ kΩ and $C = 1$ pf, with a device width of 1 μm for this condition and a peak-to-peak 2 V sine wave for the input supply at 2.45 GHz. (b) A partial enlargement of the graph (a) showing the voltage fluctuations across the load resistor. (c) Instantaneous input and output power curves. (d) Output voltage and rectification efficiency curves with the variation of load resistance.

4.2. TRAN simulation

An important indicator for AC–DC conversion circuits is the rectification efficiency, which characterizes the energy conversion efficiency of the circuit. The formula for rectification efficiency is

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\%. \tag{14}$$

Transient simulation is considered to get the input power and output power of the circuit: due to the presence of capacitance on the output side, transient simulation takes some time to reach a steady state,[2,3,26,27] so the steady state waveform after 38 ns is uniformly selected for analysis. The input voltage, input current, load voltage and load current on both sides of the circuit vary as shown in Fig. 15(a). Figure 15(b) shows a ΔV change in the output voltage within one cycle, which affects the stability of the output voltage of the circuit. The following relations hold for the output load:

$$P_{\text{out}} = \frac{V_{\text{out}}^2}{R_{\text{load}}}, \tag{15}$$

$$P_{\text{in}} = I_{\text{in}} \times V_{\text{in}}. \tag{16}$$

Based on these relationships, the instantaneous input power and output power variation curves for the circuit can be plotted (Fig. 15(c)). According to the above instantaneous power analysis, the rectification efficiency within one cycle can be solved as

$$\eta = \frac{\frac{1}{T}\int_0^T \frac{V_{\text{out}}^2}{R_{\text{load}}}}{\frac{1}{T}\int_0^T I_{\text{in}} \times V_{\text{in}}} \times 100\%. \tag{17}$$

The above conditions are analyzed and simulated to obtain the rectification efficiency and output voltage curves under different loads, as shown in Fig. 15(d). In order to have a balanced performance of output voltage and rectification efficiency, a load resistor of 20 kΩ is chosen.

Figure 16 compares the variation of the rectification efficiency between the Si MOS and the quantum MOS under the same conditions as mentioned before. It can be seen that the quantum MOS has a better conversion efficiency relative to the Si MOS in the input power range of −30 dBm to 6.9 dBm. At an input power of −10 dBm, the efficiency of the quantum device can reach 7.14%, which is 4.2 times that of the Si MOS. There is a peak conversion efficiency of 45.51% at 6.9 dBm, which is still higher than that of the Si MOS (42.13%). However, above 6.9 dBm, the rectification efficiency of the device decays rapidly and the rectification effect is weaker than that of an ordinary Si MOS. Comparison shows that their output voltages are similar. Below an input power of 10 dBm, the output voltage curve of the quantum MOS is higher than that of Si MOS, while above 10 dBm it decays rapidly. In short, this figure shows that the quantum MOS has a better weak energy density collection capability at 2.45 GHz relative to the Si MOS under the same conditions.

Comparing the efficiency curves at different widths (Fig. 17), it can be seen that as the width increases the peak rectification efficiency first increases, reaching a peak of 48.52% at $W = 2.5$ μm, and then gradually decays. When the width is greater than 2.5 μm, there is a significant overall decay in the efficiency curves and the maximum efficiency drops rapidly. For a CMOS rectifier circuit, a width of 2.5 μm means that the area of a single device can be reduced by several times, which greatly reduces the area of the chip and cuts the cost.

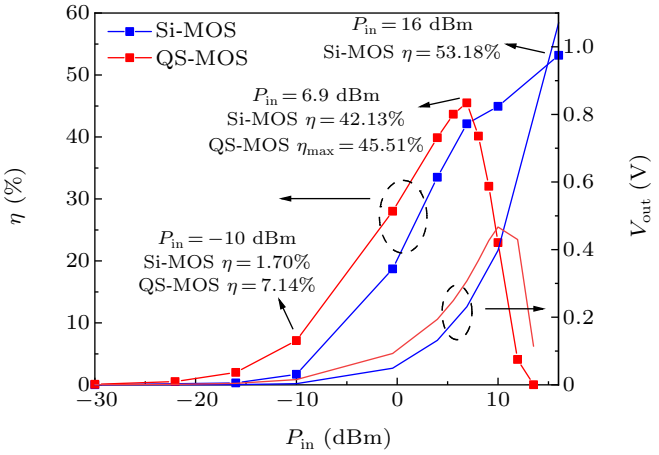


Fig. 16. The rectification efficiency and output voltage of the Si MOS and the quantum MOS with variation of input power densities under the same conditions.

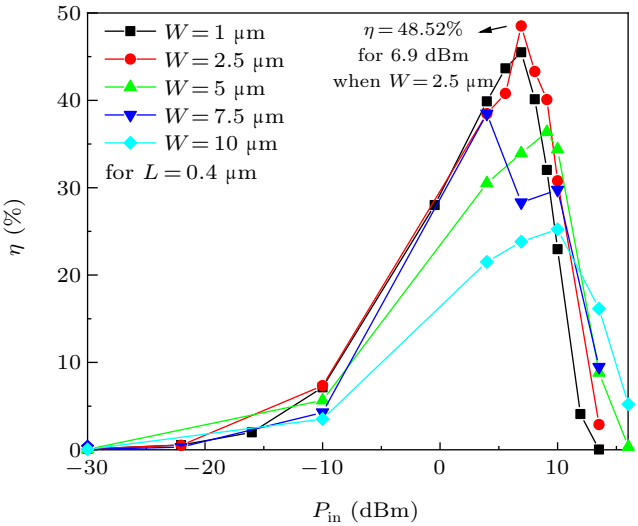


Fig. 17. The variation of the efficiency at different widths and the maximum efficiency, which is achieved at 6.9 dBm input power and 2.5 μm width.

5. Conclusion and perspectives

In conclusion, a quantum structured n-MOS device was designed using SiGeSn and GeSn materials, which greatly improved the mobility of the device compared with ordinary Si devices. The threshold voltage and electrical characteristics of the device were analyzed by simulation. In order to improve the rectification efficiency, the threshold voltage of the device

was adjusted to 91 mV, and a simple half-wave rectification test circuit was built with a novel connection method. The advantages of this MOS over a Si MOS were analyzed in terms of DC and transient simulation, and a rectification efficiency of 7.14% (at −10 dBm) was obtained, which is 4.2 times higher than that of a Si MOS under the same conditions, fully illustrating the advantages of this device.

Table 2 compares the results of this work and some previous works,[3,28–31] showing the advantages of the device described this work. It is worth noting that for simplicity of analysis the device modeling in this paper does not take into account the various process designs in the short channel case, and the device feature size is 400 nm. Therefore, it is believed that with process improvement such as advanced nodes, proper matching and boost circuit design as summarized in the Ref. [28], the device described in this paper will be more advantageous in the RF rectification field.

Table 2. CMOS performance summary.

Ref.	Tech.	Rectifier topology	Frequency (GHz)	Power conversion efficiency (% for load at input level)
This work	400 nm n-MOS	one-stage half-wave	2.45	7.14% for 20 kΩ@−10 dBm
[3]	180 nm CMOS	five-stage on-chip inductor	0.9	14.46% for 200 kΩ@−9 dBm
[29]	300 nm CMOS	three-stage Dickson	0.95	1.5% for 200 kΩ@−14 dBm
[30]	90 nm CMOS	four-stage Dickson	2.45	1% for 1 MΩ@−8.06 dBm
[31]	180 nm CMOS	five-stage Dickson	2.63	7% for 500 kΩ@−15.4 dBm

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