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High linearity AlGaN/GaN HEMT with double-V_{th} coupling for millimeter-wave applications

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We demonstrated an AlGaN/GaN high electron mobility transistor (HEMT) namely double-V_{th} coupling HEMT (DVC-HEMT) fabricated by connecting different threshold voltage (V_{th}) values including the slant recess element and planar element in parallel along the gate width with N_2O plasma treatment on the gate region. The comparative studies of DVC-HEMT and Fin-like HEMT fabricated on the same wafer show significantly improved linearity of transconductance (G_m) and radio frequency (RF) output signal characteristics in DVC-HEMT. The fabricated device shows the transconductance plateau larger than 7 V, which yields a flattened f_T/f_{max}-gate bias dependence. At the operating frequency of 30 GHz, the peak power-added efficiency (PAE) of 41% accompanied by the power density (P_{out}) of 5.3 W/mm. Furthermore, the proposed architecture also features an exceptional linearity performance with 1-dB compression point ($P_{1\,dB}$) of 28 dBm, whereas that of the Fin-like HEMT is 25.2 dBm. The device demonstrated in this article has great potential to be a new paradigm for millimeter-wave application where high linearity is essential.

Keywords: AlGaN/GaN, linearity, 1-dB compression point, millimeter-wave application

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1. Introduction

The surging demand for the Internet of things (IoT) has promoted the development of modern wireless communication technologies.[1–3] High data transfer rate and spectrum efficiency have becoming significant index parameters for modern mobile communication equipment in power amplifiers (PAs), which imposes higher linearity requirements on PAs.[4,5] Gallium nitride (GaN)-based high-electron mobility transistors (GaN HEMTs) have been the most promising devices for PAs in telecommunication applications due to superior material properties.[6,7] However, the conventional AlGaN/GaN HEMT suffers from nonlinearities with a bell-shaped transconductance (G_m) profile, which may be attributed to several physical origins including (i) self-heating effects,[8] (ii) parasitic capacitance,[9] (iii) source resistance nonlinearity,[10–12] and (iv) electron saturation velocity.[13,14] Several approaches have been employed to address the G_m roll-off at high drain current level.[15–19] Choi[20] obtained a composite device with G_m plateau $>$ 6 V and OIP_3/P_{dc} is 8.2 dB at 30 GHz by optimizing the fin width and number of fins along the gate direction. Sohel[21] has reported the polarization-graded transistors by employing a three-dimensional electron gas channel (3DEG) with OIP_3/P_{dc} of 13.3 dB at 10 GHz.

Additionally, we have recently proposed a novel architecture with transconductance plateau $>$ 5.6 V by tailoring a flat G_m profile.[22] Such structures have been proven to be able to effectively suppress the G_m roll-off at high drain current and thus enhance the linearity. However, the off-state current induced by etching is deteriorated about 2 orders compared with conventional planar HEMT, which severely impedes device reliability and deteriorates power efficiency.[23] It has been found that the plasma treatment such as N_2O can effectively suppress the leakage current.[24–26]

In this work, we optimized the structure reported in our previous work[22] by connecting different V_{th} values including the slant recess element and planar element in parallel along the gate width with N_2O plasma treatment on the gate region. The architecture of such scheme is named as double-V_{th} coupling-HEMT (DVC-HEMT). In comparison with Fin-like HEMT, the linearity of DC and RF characteristics has been significantly promoted for DVC-HEMT. The fabricated DVC-HEMT shows a gate voltage swing (GVS) of the transconductance plateau larger than 7 V and a constant f_T/f_{max} of 40 GHz/60 GHz over a wide gate voltage range. Due to the thin oxide layer formed by N_2O treatment, the DVC-HEMT demonstrates an on/off ratio of over 10^8, associated with a maximum current collapse (CC) of as low as 3.2%. At the

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operating frequency of 30 GHz, the peak power-added efficiency (PAE) of 41% accompanied by the power density (P_{out}) of 5.3 W/mm at $V_d = 20$ V is obtained by the DVC-HEMT, as well as that of Fin-like HEMT is 34% accompanied by 4 W/mm at $V_d = 2$ V. Furthermore, the proposed architecture also features an exceptional linearity performance with 1-dB compression point ($P_{1\,dB}$) of 28 dBm at 30 GHz, whereas that of the Fin-like HEMT is 25.2 dBm. Therefore, the DVC-HEMT is believed to be an attractive alternative approach for millimeter-wave application requiring high linearity and high efficiency.

2. Device structure and fabrication

The devices in this work were fabricated on an AlGaN/GaN heterostructure grown on SiC substructure by metalorganic chemical vapor deposition (MOCVD). Figure 1 shows the schematic of the devices. Its epilayers include a 1.3-μm GaN buffer layer, a 1-nm AlN interlayer, and a 24-nm AlGaN barrier. The measured two-dimensional electron gas (2DEG) mobility and density are 2096 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 1.04×10^{13} cm^{-2}, respectively.

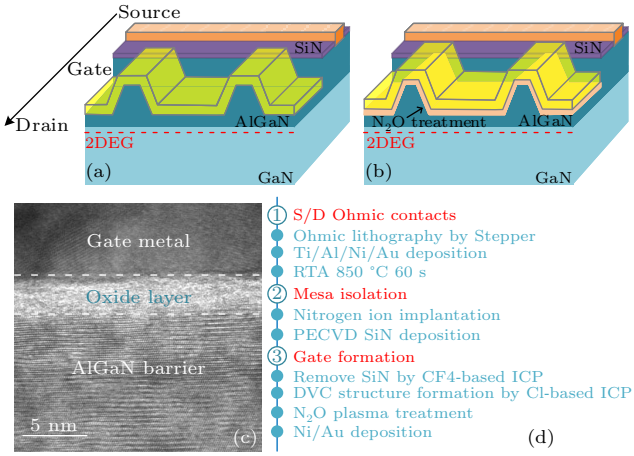


Fig. 1. The structure diagram of (a) Fin-like HEMT and (b) DVC HEMT; (c) the TEM micrograph of the surface plasma treatment formed by oxide on AlGaN barrier; (d) process flow for the fabricated DVC-HEMT.

Four different devices including a convention planar HEMT (the inset 1 in Fig. 2(b)), recess-gate HEMT (the inset 2 in Fig. 2(b)), Fin-like HEMT (as shown in Fig. 1(a)), and the DVC-HEMT (as shown in Fig. 1(b)) were fabricated together for comparison. Device fabrication started with the source and the drain Ohmic contact formation using Ti/Al/Ni/Au evaporation process followed by rapid annealing at 850 °C for 50 s in ambient N_2. After the device's electrical isolation was formed through nitrogen ion implantation, an Ohmic contact resistance of 0.36 Ω·mm was achieved and verified using transmission-line measurement (TLM). A 120-nm SiN layer was deposited by plasma-enhanced chemical vapor deposition (PECVD), and electron beam lithography (EBL) was used to define the gate foot. For the detailed information of planar HEMT, recess-gate HEMT and Fin-like HEMT is described in our previous work.[22]

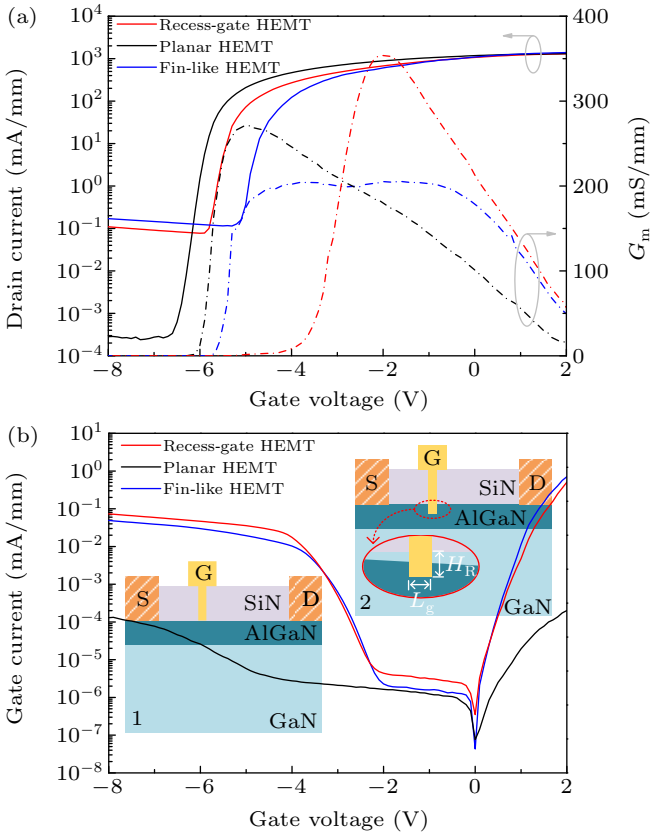


Fig. 2. Comparison of (a) transfer characteristics and (b) Schottky characteristics among planar HEMT, recess-gate HEMT, and Fin-like HEMT. Inset: cross section of 1 the planar HEMT and 2 gate-recess HEMT.

Significantly, for the DVC-HEMT as shown in Fig. 2(b), after removing the SiN in the gate region, a second EBL lithography was employed to define slant recess. Since SiN served as a hard mask during the Cl_2-based etching process, the periodic slant recess features the same length as the gate foot. After that, the gate region was treated by N_2O plasma. The N_2O plasma treatment was carried out in the PECVD system. The chamber pressure was 600 mTorr (1 Torr = 1.33322×10^2 Pa), the flow rate of N_2O was 80 sccm, the ambient temperature was 250 °C, the plasma power was 200 W, and the treatment time was 30 min. This process is aimed to form a layer of oxide instead of deposition or thermal growth using additional process. The thickness of the oxide was estimated to be around 3 nm by using the transmission electron microscopy (TEM) image as shown in Fig. 1(c). Finally, a gate cap based on Ni/Au/Ni metal stacks was deposited using electron beam evaporation. The process flow for DVC-HEMT fabrication is shown in Fig. 1(d). For a direct comparison, all devices have the same gate length (L_g) of 200 nm, a source drain distance (L_{sd}) of 3 μm. In particularly, the etch depth (H_R) of recess-gate HEMT (the inset 2 in Fig. 2(b)) and Fin-like HEMT is 7.5 nm.

3. Results and discussion

The DC measurement of the fabricated devices are measured by Keithley 4200 semiconductor analyzer. Figure 2(a) shows the comparison of transfer characteristics among planar HEMT, recess-gate HEMT, and Fin-like HEMT. It could be notably observed that the GVS (the difference in gate voltage corresponding to 80% of the peak G_m) of Fin-like HEMT is significantly improved in comparison with that of planar HEMT and recess-gate HEMT. The flatter G_m profile of Fin-like HEMT implies that the architecture can effectively inhibit G_m roll-off at high drain current. However, as shown in Fig. 2(b), the off-state leakage current of planar HEMT is at the order of 10^{-4} mA/mm, whereas, that of Fin-like HEMT and recess-gate HEMT is up to 10^{-2} mA/mm. The deterioration of leakage current is mainly attributed to the dry etching which may result in the interface scattering[27] and the increment of tunneling current.[28]

In order to comparatively investigate the DC characteristics of DVC-HEMT, we selected the Fin-like HEMT as reference. As shown in Fig. 3(a), due to a thin oxide layer formed on the gate region of DVC-HEMT, the gate leakage current at least 4 orders of magnitude lower than that of Fin-like HEMT, leading to an ultralow off-state current of 9.3×10^{-6} mA/mm accompanied by an on/off ratio of over 10^8. Interestingly, a higher RF linearity performance will be manifested for HEMT when the first- and second-order derivatives of transconductance is close to zero,[20] which means that it is key to reduce the derivative characteristics for fabricating high linearity device. Figure 3(b) compares the transconductance (G_m) and it is derivative characteristics (G'_m and G''_m) of the two kinds of devices. It could be noted that the peak transconductance (G_m-max) is 201 mS/mm for DVC-HEMT and 205 mS/mm for Fin-like HEMT, respectively. The slightly reduction of the peak G_m is attributed to the increased gate-to-channel separation for DVC-HEMT. However, as seen from in Fig. 3(b), the DVC-HEMT displays dramatically more constant G_m profile with GVS of 7 V, in contrast, that of Fin-like HEMT is 5.7 V. Thus, the enhanced GVS of DVC-HEMT leads to a lower G'_m of 0.25 S/mm·V accompanied by an G''_m of 0.5 S/mm·V^2, which are evidently improved by 0.08 S/mm·V and 0.4 S/mm·V^2 compared to those of Fin-like HEMT, respectively. That is to say, the DVC-HEMT shows significant improvement in the transitive region from the subthreshold to the peak value. In the linearly increasing region, DVC-HEMT exhibits the flattest G_m profile, thereby suppressing undesirable harmonic elements. The results imply that DVC-HEMT improve the G_m linearity effectively and have great advantages in device-level linearization.

Figure 3(c) shows the Schottky characteristics of the two kinds of devices, it could be observed that the gate current of DVC-HEMT is at least 4 orders of magnitude lower than that of Fin-like HEMT at $V_g = -8$ V, and 3 orders of magnitude lower than that of Fin-like HEMT at $V_g = 2$ V, which furtherly validates the above observations from transfer characteristics in Fig. 3(a). In short, the physical central idea of DVC-HEMT is "double-V_{th} coupling" technology, which integrates the double elements with different gate-overdrive (V_G–V_{th}) quiescent bias voltages in parallel along the gate width to suppress the premature roll-off of G_m. Meanwhile, accounting for the insertion of 3-nm oxide gate insulator between gate-to-channel, the DVC-HEMT exhibits a flattened G_m profile and decreased gate leakage current, which should result in lower levels of the RF distortions and enhance the output power and efficiency of AlGaN/GaN HEMT at the elevated power levels.[29,30]

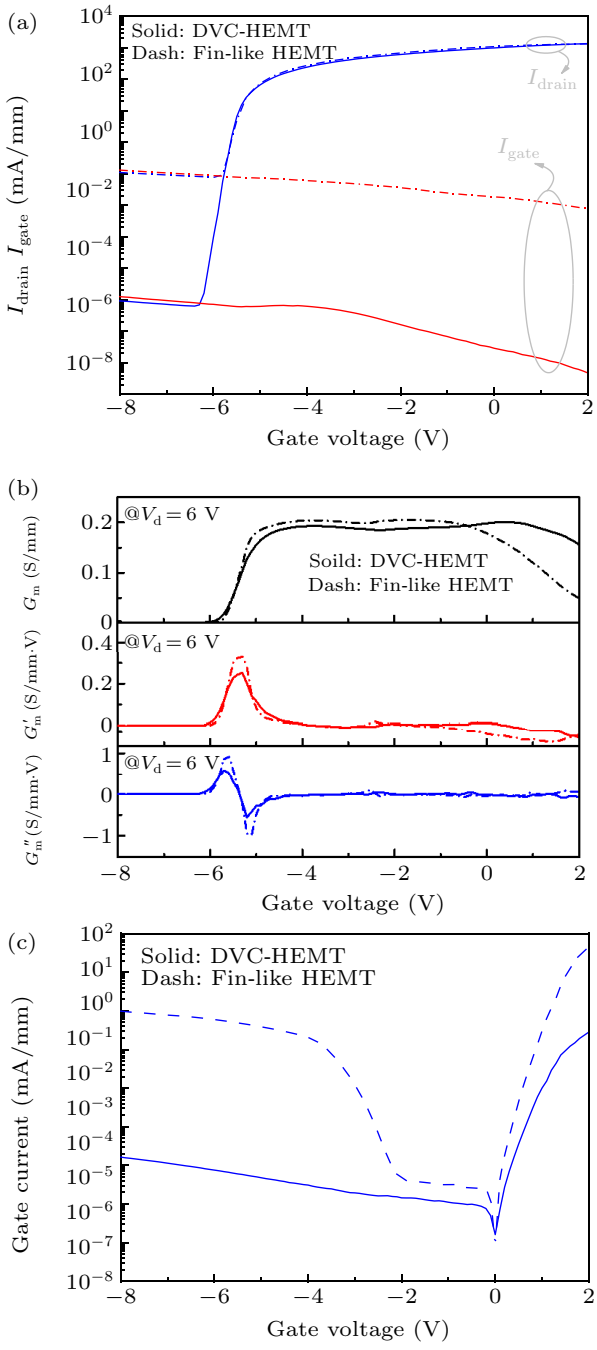


Fig. 3. Comparison of (a) transfer characteristics (log), (b) transconductance (G_m) and high order transconductance (G'_m and G''_m), and (c) Schottky characteristics between Fin-like HEMT and DVC-HEMT.

In addition to the improved DC characteristics, the current collapse (CC) of HEMT, severely limits the maximum output powers and deteriorates the device linearity, thus, the CC of DVC-HEMT was also calculated by the pulsed measurement. The pulsed measurements were performed by using the pulse of 500 ns in width and 1 ms in period (as shown in Fig. 4) to investigate the current dispersion of the device. At the bias point $(V_{GSQ}, V_{DSQ}) = (-8\ \text{V}, 0\ \text{V})$, there is a potential difference between gate and drain, so the electrons in the gate electrode could be captured by the trap state. Therefore, the bias point $(V_{GSQ}, V_{DSQ}) = (-8\ \text{V}, 0\ \text{V})$ is selected to evaluate the trap state and avoid the self-heating effect. Figure 4 shows that an 8.8% drain current (I_d) reduction of Fin-like HEMT (as shown in Fig. 4(b)) happens at $V_{GS} = 2$ V and $V_{DS} = 10$ V while that of the DVC-HEMT (as shown in Fig. 4(a)) reduces by 3.2% at the same bias condition. Furthermore, the CC of DVC-HEMT is 5.0% at $(V_{GSQ}, V_{DSQ}) = (8\ \text{V}, 20\ \text{V})$ while that of Fin-like HEMT is 11.2% at $(V_{GSQ}, V_{DSQ}) = (8\ \text{V}, 20\ \text{V})$, The results indicate that the N_2O plasma pre-treatment can essentially suppress the trap state-related carrier trapping and thus contribute to the RF efficiency.[30]

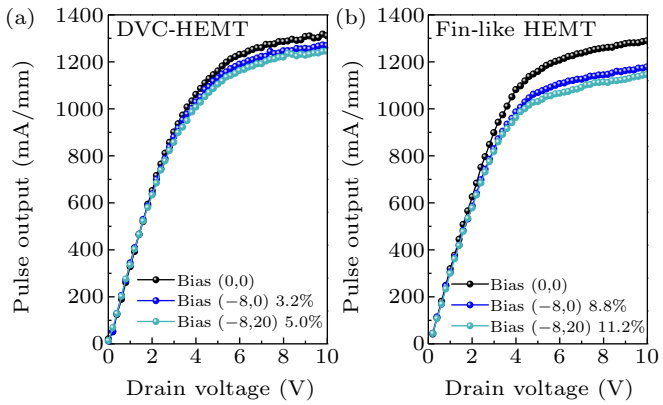


Fig. 4. Double-pulse characteristics of (a) DVC-HEMT and (b) Fin-like HEMT.

As shown in Fig. 5(a), the maximum current–gain cutoff frequency (f_T) and the maximum power gain cutoff frequency (f_{max}) of the DVC-HEMT are 40 GHz and 60 GHz, respectively. Due to increased gate-to-channel separation and lower G_m peak for DVC-HEMT, the peak f_T and f_{max} are slightly lower than those of Fin-like HEMT. However, as demonstrated in Fig. 5(b), f_T and f_{max} yield a flatter curve over a wider range of gate bias, which is associated with the increased G_m flatness of DVC-HEMT. Based on good agreement between the G_m and small signal profile, we conclude that the modulation of G_m characteristics is advantages to improve f_T/f_{max} linearity of DVC-HEMT compared to Fin-like HEMT.

To corroborate the device power characteristics and their effect on the millimeter-wave application performance, power measurement of HEMT at 30 GHz was performed in continuous wave using an on-wafer load pull system. The load and the source impendence were tuned for the optimum PAE, so that the power linear gain was lower than the small signal gain. Figures 6(a) and 6(b) illustrate the output power density (P_{out}), the power gain (G_{ain}), and the PAE as a function of the input power (P_{in}) for the DVC-HEMT and Fin-like HEMT, respectively, both of which are characterized at deep-class AB operation at $V_d = 20$ V. Due to the excellent pinch-off characteristics, minimized gate current and suppressed CC, a P_{out} of 5.3 W/mm and a peak PAE of 41% are notably observed from Fig. 6(a), whereas, those of Fin-like HEMT as shown in Fig. 6(b) are 4 W/mm and 34%, respectively. Furthermore, the DVC-HEMT device exhibits a more flattened gain curve with the compression between the linear gain and associated gain is as low as 0.8 dB, as well as, for Fin-like HEMT, the gain compression is up to 2.7 dB. Due to the improvement of gain compression, a $P_{1\,dB}$ of 28 dBm is obtained by the DVC-HEMT, in contrast, Fin-like HEMT shows a $P_{1\,dB}$ of 25.2 dBm, indicating the smaller distortion of RF linearity in DVC-HEMT. The improvement of RF linearity performance is mainly attributed to the flatter G_m profile, which indicates that the proposed architecture has an obvious potentiality in the high linearity millimeter-wave application.

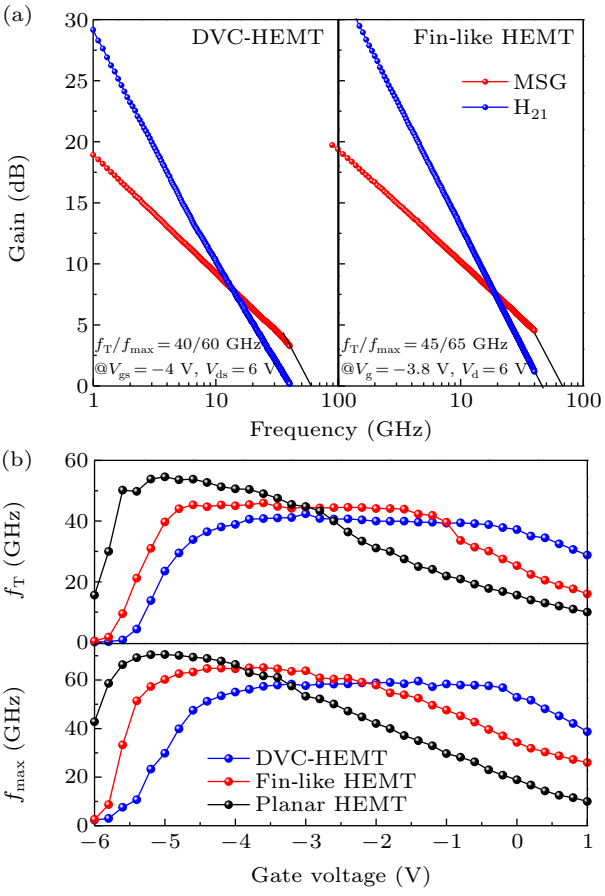


Fig. 5. (a) Small signal characteristics of DVC-HEMT and Fin-like HEMT. (b) Gate voltage dependence of f_T and f_{max} for DVC-HEMT, Fin-like HEMT, and planar HEMT at $V_d = 6$ V.

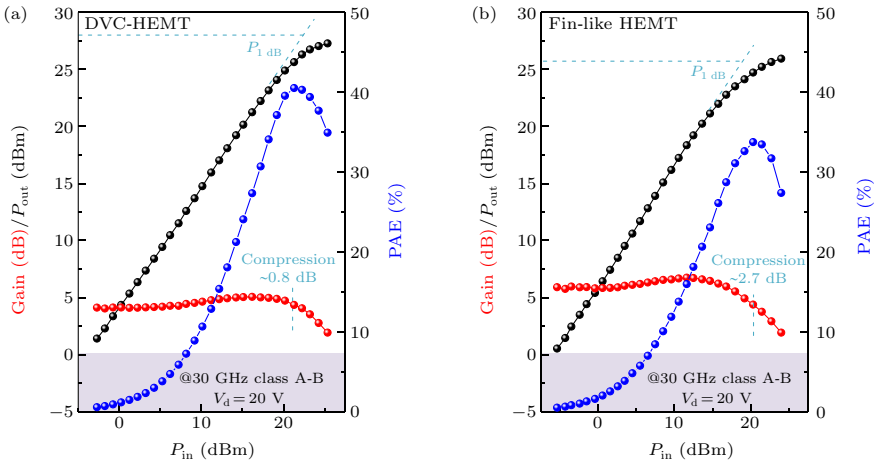


Fig. 6. Comparison of output power characteristics after a load-pull at frequency of 30 GHz and $V_d = 20$ V: (a) DVC-HEMT and (b) Fin-like HEMT.

4. Conclusion

This work presents a novel device namely DVC-HEMT obtained by integrating different V_{th} values including the slant recess element and planar element in parallel along the gate width with N_2O plasma treatment on the gate region, to produce a device with high linearity performance in millimeter-wave application. The fabricated DVC-HEMT exhibits a steady G_m and f_T/f_{max} plate curve with GVS of 7 V and a constant f_T/f_{max} of 40 GHz/60 GHz. Furtherly, it also features an exceptional linearity performance with $P_{1\,dB}$ of 28 dBm at frequency = 30 GHz, $V_d = 20$ V whereas that of the Fin-like HEMT is 25.2 dBm at same bias condition. The proposed architecture has an obvious potentiality in millimeter-wave application requiring good linearity and high efficiency.

Acknowledgments

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