

Extrinsic equivalent circuit modeling of InP HEMTs based on full-wave electromagnetic simulation

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Extrinsic equivalent circuit modeling of InP HEMTs based on full-wave electromagnetic simulation

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With the widespread utilization of indium-phosphide-based high-electron-mobility transistors (InP HEMTs) in the millimeter-wave (mmW) band, the distributed and high-frequency parasitic coupling behavior of the device is particularly prominent. We present an InP HEMT extrinsic parasitic equivalent circuit, in which the conductance between the device electrodes and a new gate–drain mutual inductance term L_{mgd} are taken into account for the high-frequency magnetic field coupling between device electrodes. Based on the suggested parasitic equivalent circuit, through HFSS and advanced design system (ADS) co-simulation, the equivalent circuit parameters are directly extracted in the multi-step system. The HFSS simulation prediction, measurement data, and modeled frequency response are compared with each other to verify the feasibility of the extraction method and the accuracy of the equivalent circuit. The proposed model demonstrates the distributed and radio-frequency behavior of the device and solves the problem that the equivalent circuit parameters of the conventional InP HEMTs device are limited by the device model and inaccurate at high frequencies when being extracted.

Keywords: extrinsic equivalent circuit modeling, InP HEMT, HFSS and ADS co-simulation, *S*-parameters

PACS: 73.40.Qv, 85.30.De, 07.05.Tp **DOI:** 10.1088/1674-1056/ac2b1d

1. Introduction

Indium-phosphide-based high-electron-mobility transistors (InP HEMTs) with outstanding high-frequency characteristics have been developed and widely investigated in the last decades. Now, the InP HEMT possesses cut-off frequency up to hundreds of gigahertz and maximum oscillation frequency over 1 THz.[1–3] And the high-frequency InP HEMT has been designed and manufactured into sub-millimeter monolithic integrated circuits (MMIC).[4–6] However, as the operating frequency of the device continues to increase, the device exhibits a distributed behavior, and the parasitic resistance, capacitance, and inductance of the metal plating layer interconnected with the device make the performance of the device degrade significantly.[7] Moreover, the conventional device models can no longer characterize the basic physical principles of device performance degradation. Hence, high-fidelity small-signal device models, in which intrinsic and extrinsic behavior concurrently are considered, are necessary for effectively designing the high-frequency band integrated circuits.

The small-signal model of InP HEMTs can be divided into nonlinear intrinsic elements and linear extrinsic parasitic couplings.[8] The extrinsic elements are independent of the bias voltage, but they basically depend on the physical geometry of the device, including interconnections, electrode structures, and pads. Therefore, the extrinsic parasitic parameters are first proposed and subtracted from the experimental data when modeling. Subsequently, the intrinsic elements related to the bias are determined according to the applied bias voltage. This shows that any calculation errors of external parasitic parameters will lead to errors in the intrinsic parameters of the device and thus affecting the correct understanding of the inherent performance of the device. Hence, the accurate modeling of extrinsic parasitic components is essential.

In the past, the small-signal equivalent circuit model of InP HEMTs is established on the basis of device measurement.[9–11] When using the measured *S*-parameters to extract the equivalent circuit, there appears a problem that the unknown parameters in the circuit model are more than the number of equations provided by the experimental data.[12] In order to avoid this problem, a numerical optimization algorithm is used to extract the extrinsic parasitic parameters. However, the extraction results of numerical optimization methods are easily affected by the initial values of the parameters. More importantly, the model established by the device measurement matches the device model, which is provided only by the device manufacturer, and cannot be applied to any other device. Hence, there is needed a modeling technique that is not affected by the device model while ensuring the modeling accuracy.

The primary purpose of this paper is to explore the InP HEMT's extrinsic parasitic equivalent circuit model through electromagnetic (EM) simulation. On the basis of the conven-

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tional HEMT's model, by HFSS and ADS co-simulation, the frequency response of InP HEMT device's parasitic coupling in the low-microwave range and the mmW frequency range are predicted. Based on the parasitic coupling effect, the extrinsic parasitic parameters of InP HEMT are extracted and the parasitic equivalent circuit model is established. By comparing the co-simulation results and complete experimental data, the feasibility of parameter extraction and the accuracy of the parasitic equivalent circuit model are verified. Finally, the utility of HFSS and ADS co-simulation results of InP HEMTs model is demonstrated through an example. In the frequency range below 40 GHz which is limited by measurement condition in our laboratory, the proposed method proves highly accurate for a resistive passive device with highly distributed embedding surroundings.

2. InP HEMT's extrinsic parasitic equivalent circuit model

A cross-sectional view of the InP HEMT is shown in Fig. 1. The epitaxial layer structure is grown by molecular beam epitaxy (MBE) on a 3-inch (1 inch = 2.54 cm) semi-insulating (100) InP substrate.[13] The epitaxial layers consists of, from the bottom to the top, a 500-nm InAlAs buffer, a 15-nm $In_{0.53}Ga_{0.47}As$ channel layer, a 3-nm InAlAs spacer layer, an 8-nm InAlAs Schottky barrier layer, a 4-nm InP etching stopper layer, and a 20-nm Si-doped composite InGaAs cap layer. An Si-doped plane is inserted between the Schottky barrier layer and the spacer layer to supply the electrons for current conduction. All InAlAs layers are lattice-matched with the InP substrate.

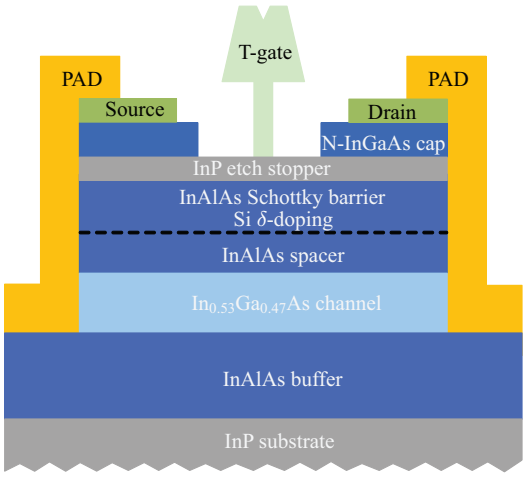


Fig. 1. Cross-sectional view of InP-based HEMT.

The extrinsic parasitic equivalent circuit of InP HEMT is independent of the external bias. Therefore, when analyzing the parasitic equivalent circuit, the device can be considered to be in a non-conducting state, which can be seen as a simplified geometric structure composed of metal and substrate as shown in Fig. 2(b).[14] To better demonstrate the distributed and mmW radio-frequency (RF) behavior of the device, the metal sizes d_1, d_2, and d_3 are set to be 40 μm, 200 μm, and 60 μm respectively. The representative geometric structure is simulated in HFSS to obtain the simulation data, which are then imported into ADS to determine the extrinsic equivalent circuit components of InP HEMT, and finally an external parasitic circuit model is established.

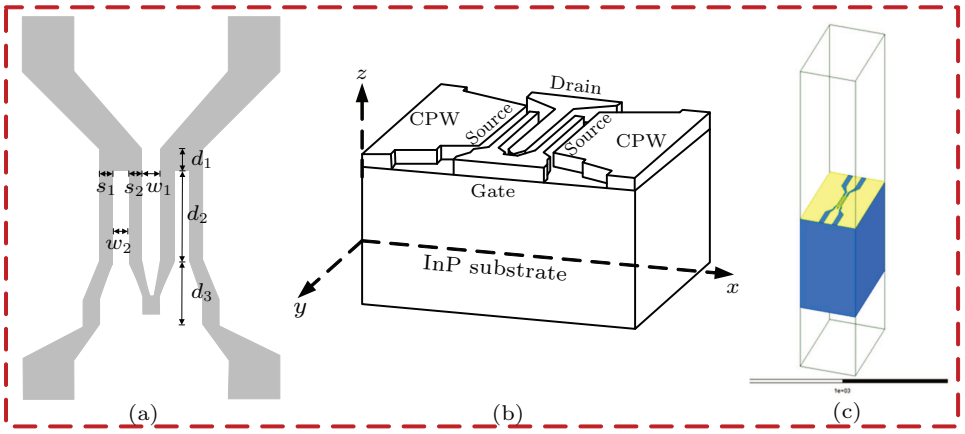


Fig. 2. (a) Simplified three-dimensional schematic diagram of InP HEMT with two fingers whose geometry dimensions are $w_1 = 6$ μm, $w_2 = 4$ μm, $s_1 = s_2 = 4$ μm, $d_1 = 40$ μm, $d_2 = 200$ μm, $d_3 = 60$ μm; (b) InP HEMT structure diagram; and (c) simulation structure diagram of InP HEMT in HFSS.

The extrinsic parasitic model of the improved InP HEMTs, shown in Fig. 3, involves 19 circuit elements. At high frequencies, the capacitive elements in the conventional HEMT equivalent circuit model are likely to shunt out the inherent transconductance, which provides the gain mechanism of the device.[15] Therefore, a conductive element corresponding to the capacitive element is introduced into the external parasitic circuit. Capacitive elements C_{egs}, C_{egd}, and C_{eds} are inter-electrode capacitances, representing the fringing electric field between the gate, drain, and source. The corresponding conductivity components G_{egs}, G_{egd}, and G_{eds} are the inter-electrode conductances, which are used to characterize the

conduction currents between the gate, drain, and source due to damage to the substrate. The electrical couplings between the gate, drain, and source contact pads are characterized by capacitive elements C_{pgs}, C_{pgd}, and C_{pds}. The corresponding conductivity components G_{pgs}, G_{pgd}, and G_{pds} are the inter-pad conductivities, which represent the electrolyte leakage losses caused by the conductivity of the semiconductor substrate. The resistive elements R_{eg}, R_{ed}, and R_{es} have physical meanings for the power consumption of the gate, drain, and source structure and the surrounding environment. The inductance elements L_{eg}, L_{ed}, and L_{es} are electrode inductances, representing the energy stored respectively in the magnetic field around the current-carrying gate, drain, and source. Most importantly, L_{mgd} is introduced to simulate the magnetic flux between the gate and the drain.

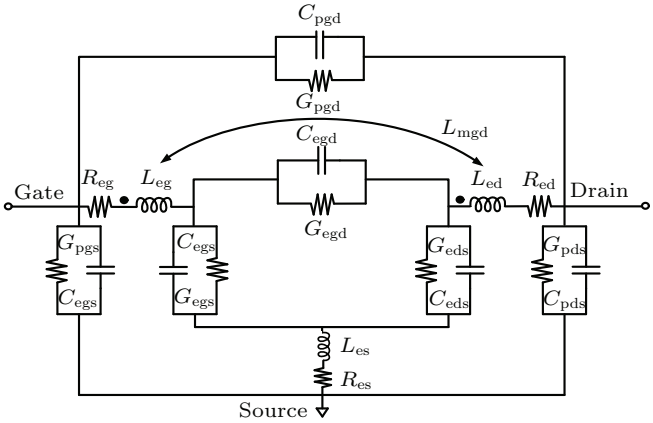


Fig. 3. Improved equivalent-circuit model for InP HEMT describing extrinsic parasitic couplings.

3. Extract extrinsic parasitic circuit components using representative test structures

Conventional InP HEMT extrinsic parameters are determined by using a cold HEMT at $V_{ds} = 0$, $V_{gs} = 0$, and pinch-off voltage.[16] Although cold HEMT conditions can be easily achieved when a probe test bench is used for testing, the de-embedding problems and some pad parasitic effects can be brought in, making the process of determining extrinsic parasitic parameters complicated and inaccurate.[17] At the same time, a large number of circuit elements that need to be concurrently determined make the single-step parameter-extraction procedure rather sensitive and unreliable. Here, a multi-step method is used to strategically divide the external circuit model into multiple sub-circuits, which can be easily adapted to experimental or simulation data to determine the frequency-dependent parasitic components of the InP HEMTs. The six proposed layouts of the algorithm are implemented in HFSS, and the corresponding lumped-element equivalent circuits for each of the test layouts are given in the ADS. The six proposed layouts and corresponding equivalent circuits are given in Figs. 4 and 5, respectively.

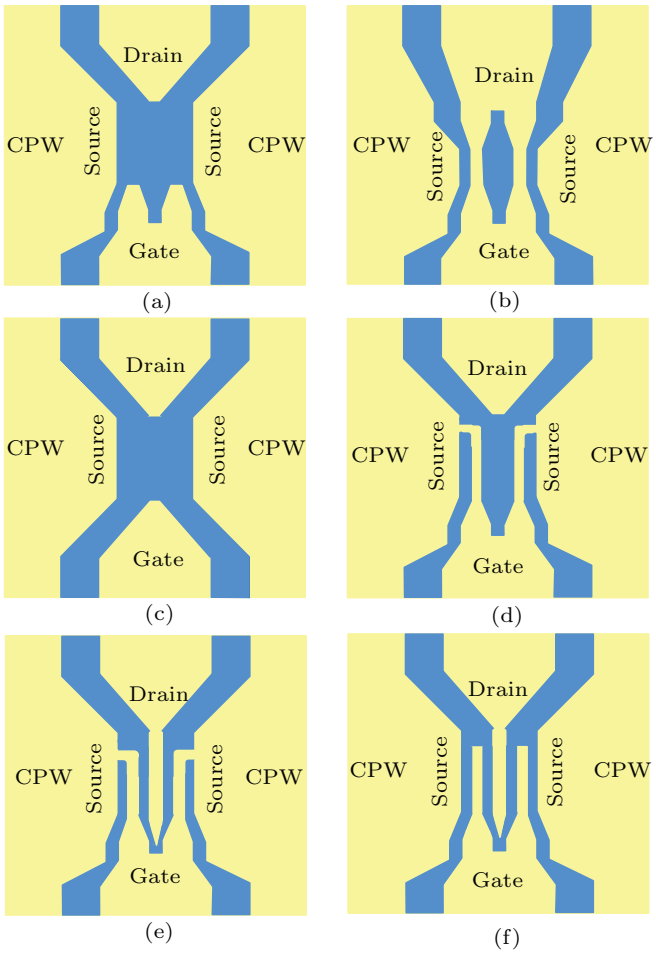


Fig. 4. Schematic diagram of the representative test structure of the proposed InP HEMTs: (a) pad, (b) thru1, (c) thru2, (d) short1, (e) short2, and (f) open test.

In the first step, the parasitic admittance matrix $[\boldsymbol{Y}^{pad}]$ of the pad is obtained by the HFSS simulation of the pad structure in Fig. 4(a). The parasitic capacitance and conductance of the corresponding padtopad in Fig. 5(a) are extracted from the the following equations:

$$
\begin{aligned}
G_{pgd} &= -\text{real}\left(Y^{pad}(1,2)\right),\\
G_{pds} &= \text{real}\left(Y^{pad}(1,2)+Y^{pad}(2,2)\right),\\
G_{pgs} &= \text{real}\left(Y^{pad}(1,2)+Y^{pad}(1,1)\right),\\
C_{pgd} &= -\text{imag}\left(Y^{pad}(1,2)\right)/(2\times\pi\times\text{freq}),\\
C_{pgs} &= \text{imag}\left(Y^{pad}(1,1)+Y^{pad}(1,2)\right)/(2\times\pi\times\text{freq}),\\
C_{pds} &= \text{imag}\left(Y^{pad}(2,2)+Y^{pad}(1,2)\right)/(2\times\pi\times\text{freq}). \quad (1)
\end{aligned}
$$

In the second step, by de-embedding the pad-related parasitics from the thru1 and thru2 test structure simulation results, the admittance matrix of the gate electrode-related parasitic couplings $[\boldsymbol{Y}^{gate}]$ and the admittance matrix of the drain electrode-related parasitic couplings $[\boldsymbol{Y}^{drain}]$ can be obtained respectively. The parasitic parameters are extracted from the

following equations:

$$
\begin{aligned}
L_{\rm eg} &= {\rm imag}\left(-1/Y^{\rm gate}(1,2)\right)/(2\times\pi\times{\rm freq}),\\
R_{\rm eg} &= {\rm real}\left(-1/Y^{\rm gate}(1,2)\right),\\
C_{\rm egs} &= {\rm imag}\left(2\times(Y^{\rm gate}(1,1)+Y^{\rm gate}(1,2))\right)/(2\times\pi\times{\rm freq}),\\
G_{\rm egs} &= {\rm real}\left(2\times(Y^{\rm gate}(1,1)+Y^{\rm gate}(1,2))\right),\\
L_{\rm ed} &= {\rm imag}\left(-1/Y^{\rm drain}(1,2)\right)/(2\times\pi\times{\rm freq}),\\
R_{\rm ed} &= {\rm real}\left(-1/Y^{\rm drain}(1,2)\right),\\
C_{\rm eds} &= {\rm imag}\left(2\times(Y^{\rm drain}(1,1)+Y^{\rm drain}(1,2))\right)/(2\times\pi\times{\rm freq}),\\
G_{\rm eds} &= {\rm real}\left(2\times(Y^{\rm drain}(1,1)+Y^{\rm drain}(1,2))\right).
\end{aligned}
\tag{2}
$$

In the third step, using short1 simulation results to remove the effects of pad parasitics and gate-to-source inter-electrode capacitance–conductance pair of ($C_{\rm egs}$, $G_{\rm egs}$), the source electrode-related parasitic coupling parameter $\boldsymbol{Y}$ matrix [$\boldsymbol{Y}^{\rm source}$] can be obtained, where the parasitic parameters are extracted by the following equations:

$$
\begin{aligned}
R_{\rm es} &= {\rm real}\left(1/Y^{\rm source}(1,1)\right)-R_{\rm eg},\\
L_{\rm es} &= {\rm imag}\left(1/Y^{\rm source}(1,1)\right)/(2\times pi\times{\rm freq})-L_{\rm eg}.
\end{aligned}
\tag{3}
$$

In the fourth step, the effects of pad-related parasitics and inter-electrode capacitance–conductance pairs of ($C_{\rm egs}$, $G_{\rm egs}$) and ($C_{\rm egs}$, $G_{\rm egs}$) are de-embedded from the simulation data of short2 layout, and the auxiliary admittance matrix [$\boldsymbol{Y}^{\rm mutual}$] can be obtained. Then, we convert the auxiliary admittance matrix [$\boldsymbol{Y}^{\rm mutual}$] into an impedance matrix [$\boldsymbol{Z}^{\rm mutual}$], and the gate–drain mutual inductance $L_{\rm mgd}$ can be obtained by the following equation:

$$
L_{\rm mgd} = {\rm imag}(Z^{\rm mutual}(1,1)-Z^{\rm mutual}(1,2))/(2\times\pi\times{\rm freq}). \tag{4}
$$

Finally, in step five, the parasitic effects of parallel-connected pads and the parasitic effects of the device electrodes in series are excluded from the open simulation data, and the inter-electrode parasitic coupling parameter $\boldsymbol{Y}$ matrix [$\boldsymbol{Y}^{\rm open}$] is obtained, in which the inter-electrode capacitance and conductance parasitic parameters are given by the following equations:

$$
\begin{aligned}
G_{\rm egd} &= -{\rm real}\left(\boldsymbol{Y}^{\rm open}(1,2)\right),\\
G_{\rm egs} &= {\rm real}\left(\boldsymbol{Y}^{\rm open}(1,1)+\boldsymbol{Y}^{\rm open}(1,2)\right),\\
G_{\rm eds} &= {\rm real}\left(\boldsymbol{Y}^{\rm open}(1,2)+\boldsymbol{Y}^{\rm open}(2,2)\right),\\
C_{\rm egd} &= -{\rm imag}\left(\boldsymbol{Y}^{\rm open}(1,2)\right)/(2\times\pi\times{\rm freq}),\\
C_{\rm egs} &= {\rm imag}\left(\boldsymbol{Y}^{\rm open}(1,1)+\boldsymbol{Y}^{\rm open}(1,2)\right)/(2\times\pi\times{\rm freq}),\\
C_{\rm eds} &= {\rm imag}\left(\boldsymbol{Y}^{\rm open}(1,2)+\boldsymbol{Y}^{\rm open}(2,2)\right)/(2\times\pi\times{\rm freq}).
\end{aligned}
\tag{5}
$$

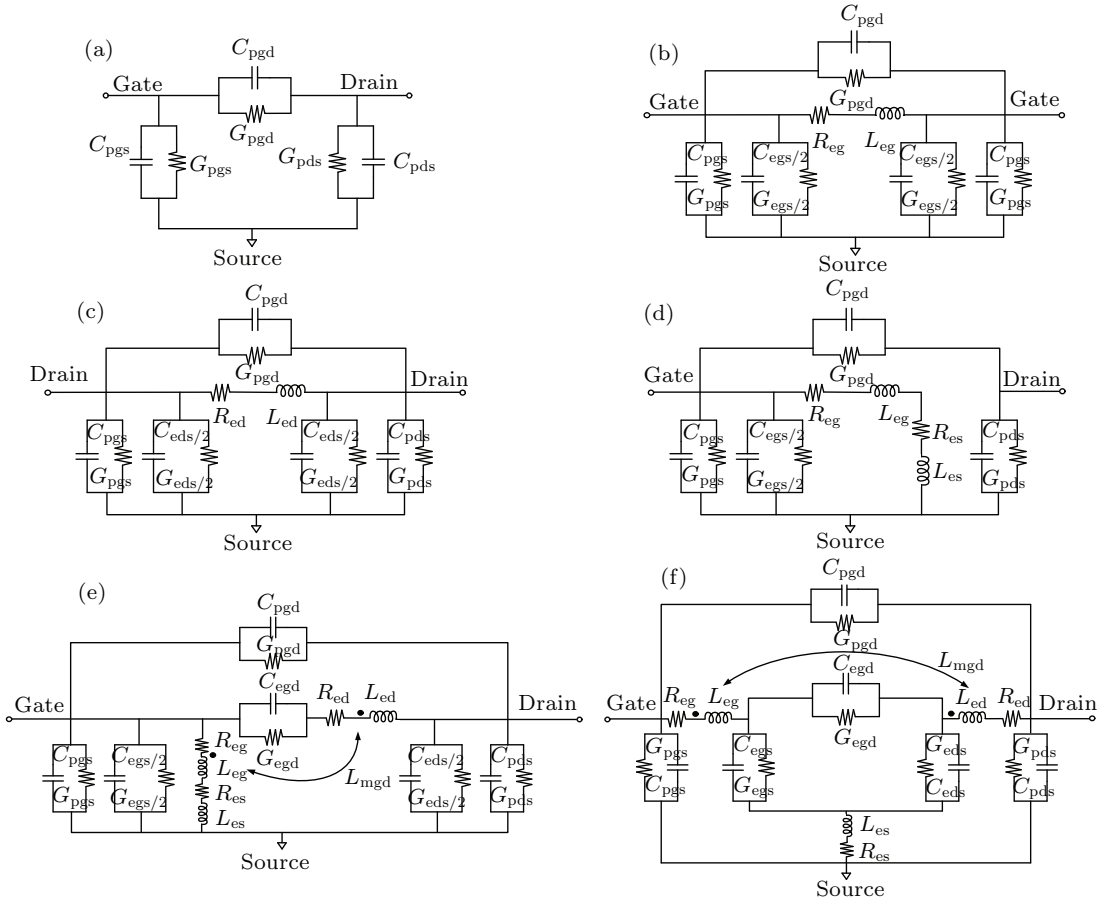


Fig. 5. InP HEMTs extrinsic circuit model proposed for different representative test structures: (a) pad, (b) thru1, (c) thru2, (d) short1, (e) short2, and (f) open test.

4. Experimental verification of proposed equivalent circuit model

To validate the accuracy of the InP HEMT parasitic equivalent circuit above, here we use the HFSS simulations of the InP HEMT topology shown in Fig. 2 in a frequency range of 1 GHz–40 GHz. All six proposed test standards are fabricated on a 3-inch InP wafer by depositing a single-layer of Au. The interconnect metallization is fabricated via Au evaporation, and the final Au layer has a thickness of 0.3 μm. The parameter settings of the substrate and gold in the HFSS simulation are shown in Table 1, which are in accordance with the characteristics of the process materials used in our laboratory. The *S*-parameters of the fabricated test patterns are measured by using the test platform in our laboratory in a range of 1 GHz–40 GHz band. The predicted and measured *S*-parameters are compared with each other to highlight the degree of agreement between the frequency responses obtained from the HFSS simulations and the experimental data.

Table 1. Parameter settings of substrate and gold in HFSS simulation.

Dielectric constant	12.9
Loss tangent	0.01
Au thickness (μm)	0.3

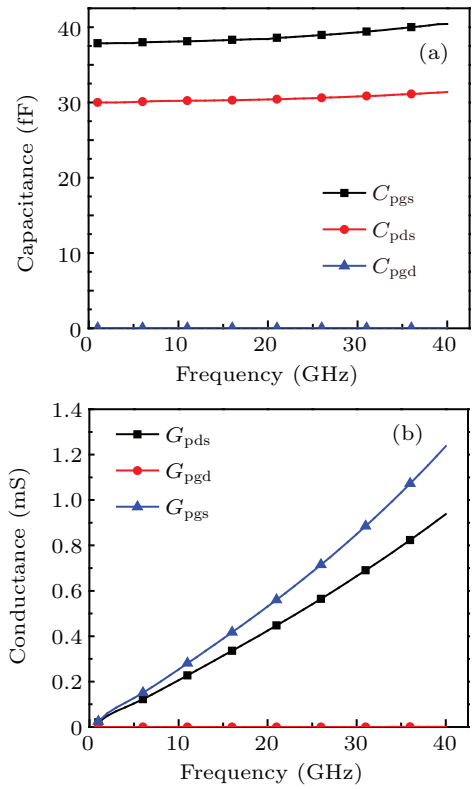


Fig. 6. Capacitances and conductances associated with the device pads: (a) C_{pgs}, C_{pds}, and C_{pgd}; (b) G_{pgs}, G_{pds}, and G_{pgd}.

The gate, drain, and source inter-pad capacitances and conductances (C_{pgs}, G_{pgs}), (C_{pgd}, G_{pgd}), and (C_{pds}, G_{pds}) are shown in Figs. 6(a) and 6(b), respectively. In the pad structure, the gate and drain electrodes are removed, leaving only the corresponding two small pieces of metal pads and they are farther apart, so the extracted feedthrough capacitance C_{pgd} between the gate and the drain pad is at least 3 orders of magnitude smaller than the remaining capacitances as can be seen from the result graph. As such, C_{pgd} is often omitted in many similar external equivalent circuits reported in Ref. [18]. In addition, the substrate conductance increases with the frequency increasing, and the substrate conductance G_{pgd} is different from the other two conductances by 3 orders of magnitude as can be seen from Fig. 6(b).

The resistance and inductance of gate, drain, and source electrode are respectively (R_{eg}, L_{eg}), (R_{ed}, L_{ed}), and (R_{es}, L_{es}), and their results calculated in the second step are plotted in Figs. 7(a) and 7(b). Owing to the similar structures of thru1 and thru2, the resistances R_{eg} and R_{ed} have the same trend as shown in Fig. 7(a). The reason why the resistance R_{es} increases sharply with frequency increasing is the skin-effect of the current, which corresponds to the concentration of current flowing on the surface of the conductor at high frequency.[19] Figure 7(b) shows that the inductance of the gate, drain and source decrease as the frequency increases. The reason is that in the high-frequency skin-effect region, there is a vertical substrate current, which leads the line inductance to decrease.[20] As the operating frequency moves well into the mmW regime, the influence of mutual inductive gate-to-drain coupling becomes more pronounced, which necessitates its accurate characterization.[21]

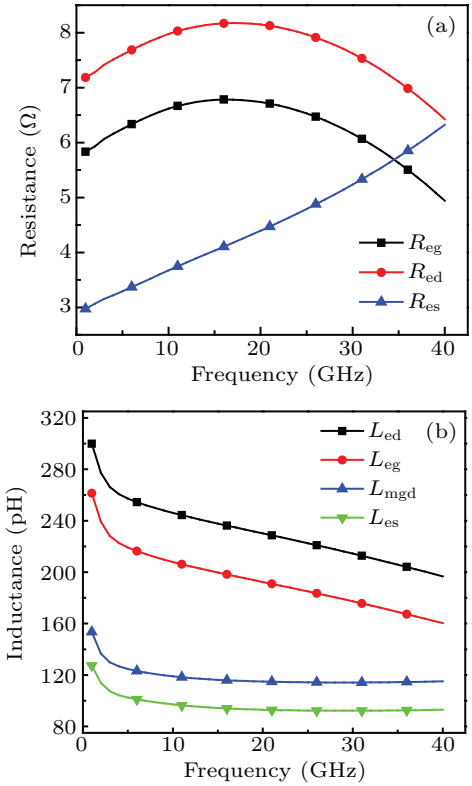


Fig. 7. Device electrode-related resistance and inductance terms. (a) R_{eg}, R_{ed}, and R_{es}; (b) L_{eg}, L_{ed}, L_{es}, and L_{mgd}.

The conventional InP HEMTs external parasitic equivalent circuit does not generally distinguish between the capacitance between pads and the capacitance between electrodes.[22,23] However, in order to maintain the modeling accuracy well in the mmW frequency range, the inter-pad coupling capacitance and the inter-electrode coupling capacitance need to be treated independently as done in this work. The calculated values of inter-electrode capacitance and conductance of (C_{egs}, G_{egs}), (C_{egd}, G_{egd}), and (C_{eds}, G_{eds}) are given in Figs. 8(a) and 8(b). Compared with the inter-pad capacitance and conductance proposed by the pad structure, the values of inter-electrode capacitance and conductance extracted by the open structure are slightly large because the metal of the open structure is intact and the electrode metal is not removed. In particular, the conductance G_{egd} between the gate and the drain varies significantly with frequency as can be seen in Fig. 8(b).

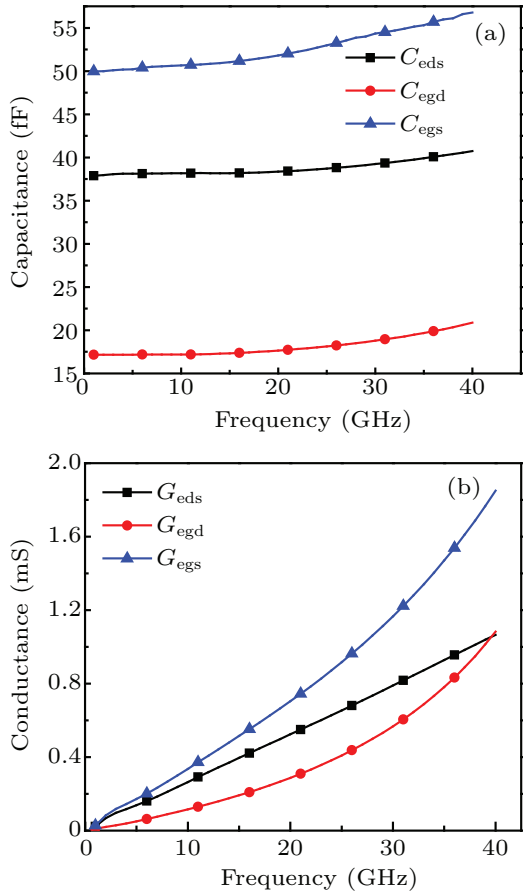


Fig. 8. Curves of frequency-dependent inter-electrode capacitance and conductance: (a) C_{egs}, C_{egd}, and C_{eds}; (b) G_{egs}, G_{egd}, and G_{eds}.

In order to verify the feasibility of the employed extraction of parasitic parameters and the accuracy of the InP HEMT equivalent circuit model, the HFSS simulation prediction, the measurement of the test structure and the modeled *S*-parameters are compared with each other as shown in Figs. 9 and 10. Bring the pad parasitic parameters extracted in the first step of the pad simulation and the parasitic parameters of the device electrodes extracted in the second and third step into the corresponding equivalent circuit, the *S*-parameter comparison results are shown in Fig. 9. The *S*-parameters obtained from the HFSS simulation exhibit excellent agreement with the measured data on the 40-GHz bandwidth. Perhaps more importantly, the simulated *S*-parameters of the proposed equivalent circuit given in Figs. 5(a)–5(d) can very accurately reproduce the frequency response of the parasitic coupling in the band range of 1 GHz–40 GHz.

To further establish the validity of the extraction method and modeling, the complete set of parasitic coupling effects is estimated by executing the five steps of the proposed parasitic extraction algorithm. Following this, the extracted element values are substituted into the equivalent circuit of the short2 in Fig. 5(e) and open test structure in Fig. 5(f). As can be seen from Fig. 10, the simulated, measured, and modeled *S*-parameters for the two test standards of parameter extraction are shown again to be in excellent agreement with each other.

To evaluate the accuracy of the HFSS simulation method, the HFSS error is defined as follows:

$$\mathrm{Err}_{\mathrm{hfss}} = \frac{1}{4}\sum_{i,j=1}^{2}\frac{|S_{ij}^{\mathrm{hfss}} - S_{ij}^{\mathrm{measure}}|}{\max\left(|S_{ij}^{\mathrm{hfss}}|\right)}, \tag{6}$$

where $\mathrm{Err}_{\mathrm{hfss}}$ is the error between the HFSS simulation value and the measure value, S^{hfss} represents the *S*-parameter of the HFSS simulation, and S^{measure} denotes the *S*-parameter of the measurements. Through calculation, the error at 40 GHz is only 2.64% which is sufficiently small for most modeling application.

The good agreement between the HFSS simulation results and the test results shown in Figs. 9 and 10 demonstrates the accuracy of the HFSS EM simulations in predicting the measured *S*-parameters on the 40-GHz bandwidth. The good agreement between the equivalent circuit simulation results and the test results proves the authenticity and accuracy of the equivalent circuit. More importantly, the *S*-parameters obtained from the equivalent circuit simulation can very accurately track the behavior of EM interaction. As seen in Figs. 10(d) and 10(e), transmission coefficient S_{21} of the open standard increases with frequency increasing, which shows that the insertion loss decreases with frequency increasing. The reason is that as the frequency increases, the capacitance C_{egd} between the gate electrode and the drain electrode plays a major role, providing an RF current flow path, so that the capacitive reactance continues to decrease.[24] This example clearly illustrates the dramatic frequency-dependence of parasitic couplings in the microwave-to-mmW regime.

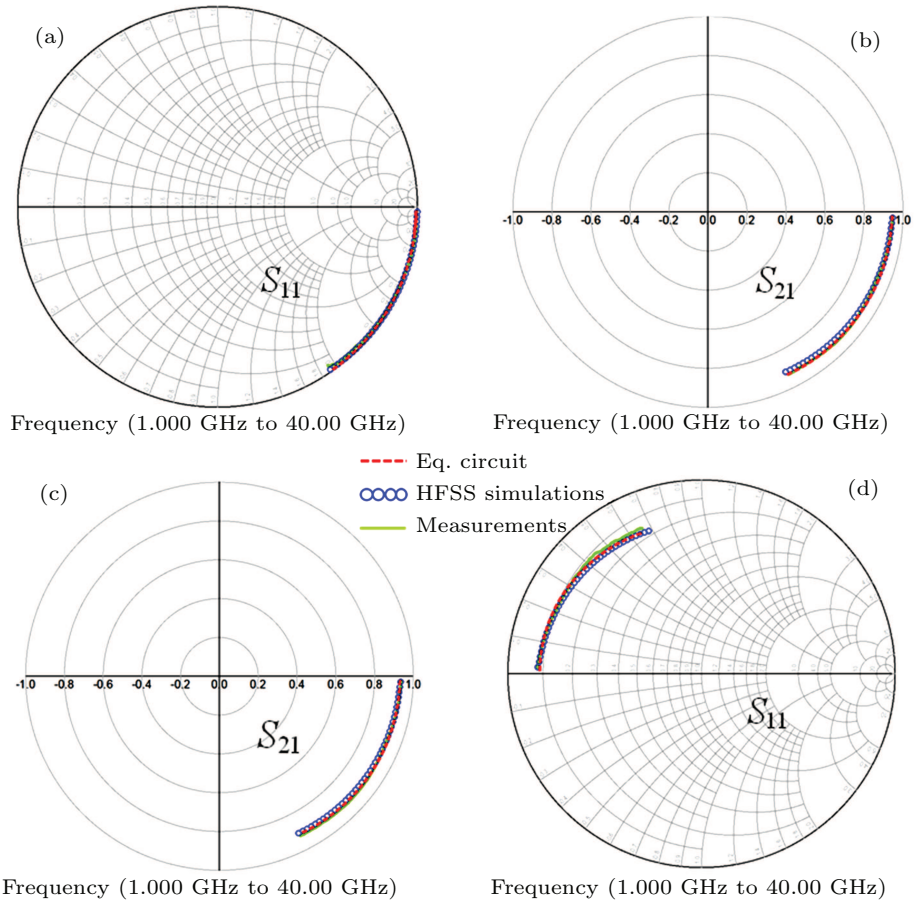


Fig. 9. The *S*-parameters from HFSS simulation, measurement, and circuit model for pad, thru1, thru2, and short1 test standards: (a) S_{11} of pad, (b) S_{21} of thru 1, (c) S_{21} of thru 2, and (d) S_{11} of short1.

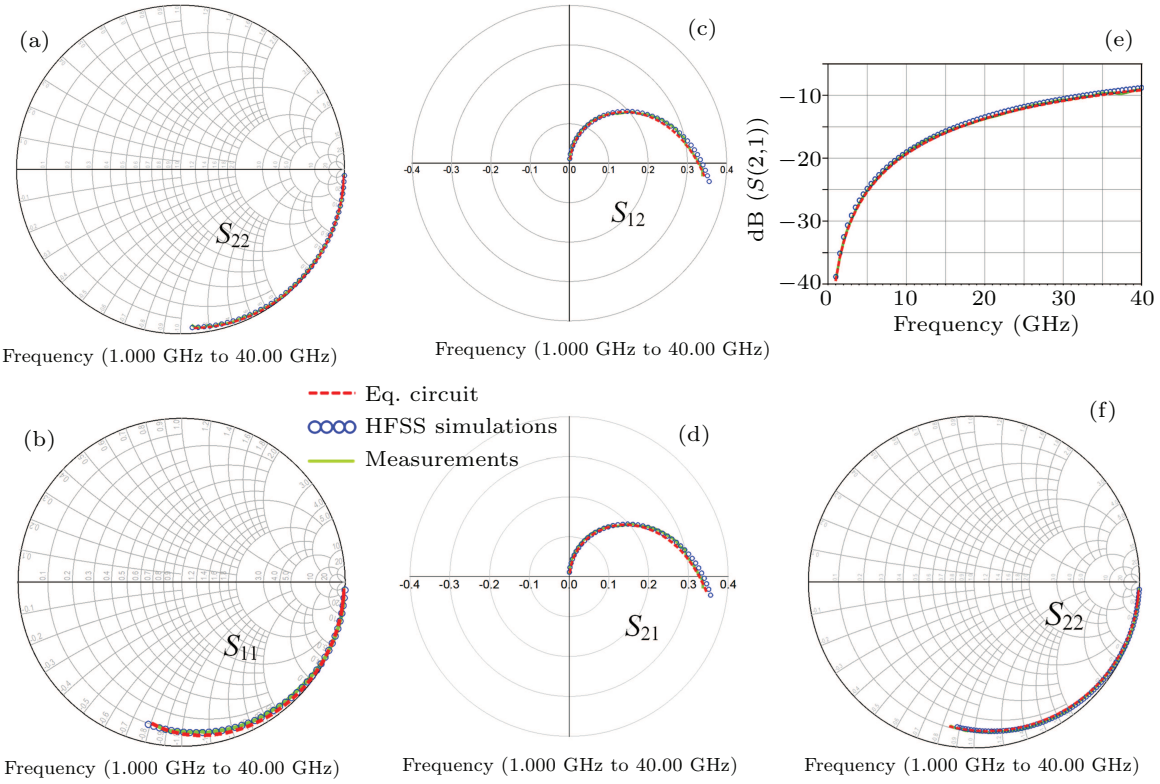


Fig. 10. The *S*-parameters from HFSS simulation, measurement, and circuit model for short2 and open test standards: (a) S_{22} of short2, (b) S_{11} of open test, (c) S_{12} of open test, (d) S_{21} of open test, (e) logarithmic magnitude of S_{21} of open test, and (f) S_{22} of open test.

Figure 11 shows the comparison between simulation results without and with the gate-to-drain mutual inductance L_{mgd} in the InP HEMT parasitic equivalent circuit. The equivalent circuit without L_{mgd} cannot accurately represent the frequency response of InP HEMT parasitic coupling in the band range of 10 GHz–40 GHz as can be seen from the figure. The transition from capacitive RF current transport at low frequency to inductive current transport at mmW frequencies is captured accurately with the aid of gate-to-drain mutual inductance of L_{mgd}. Hence, it is necessary to incorporate gate-to-drain mutual magnetic flux linkage as a separate circuit element into the parasitic equivalent circuit of the InP HEMTs to maintain modeling accuracy at mmW band.

In order to further demonstrate the utility of the proposed methodology, a conventional cold-HEMT extraction method[16] is also employed to estimate the equivalent-circuit parameters based on the simulation data of the same InP HEMT layout. The extracted circuit element values are shown in Table 2. As can be seen, the conventional extraction method includes 9 equivalent circuit elements, and the element values, especially the resistances and inductances, deviate substantially from those calculated by using multi-step simulation-based procedure (see Figs. 6–8). It is also important to underline that achieving close agreement between the frequency responses of the equivalent circuit established by the conventional method and actual device may not necessarily mean that the calculated component values are physically representative. That is, the proposed extrinsic equivalent circuit in Fig. 5(f) contains 19 elements. Consequently, it is necessary to develop a multi-step device modeling strategy, thereby precisely determining the parasitic equivalent circuit of InP HEMT as presented here.

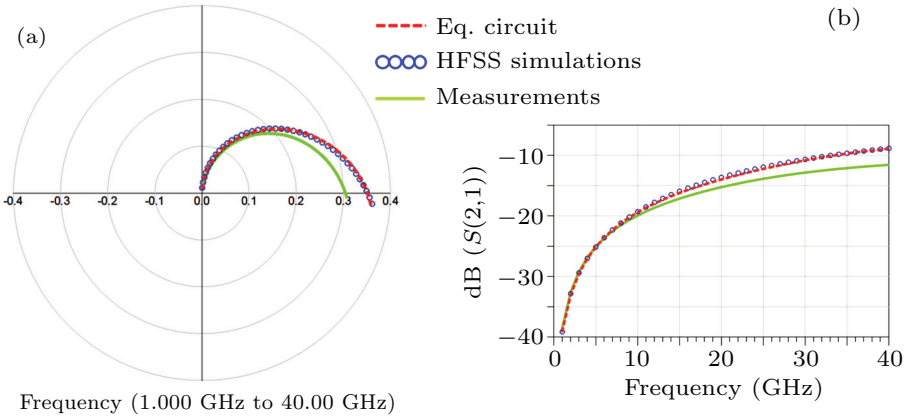


Fig. 11. Comparison between simulated and modeled transmission coefficient S_{21} for open test structure with and without gate-to-drain mutual inductance component L_{mgd}, where Y_L_{mgd} means that L_{mgd} is present, and N_L_{mgd} means that L_{mgd} is absent, showing (a) polar S_{21} and (b) logarithmic S_{21}.

Table 2. Element values extracted by conventional cold-HEMT extraction method.

Elements	C_{pgd} (fF)	C_{pgs} (fF)	C_{pds} (fF)	R_d (Ω)	R_g (Ω)	R_s (Ω)	L_d (pH)	L_g (pH)	L_s (pH)
Value	1.7	23	22	0.7	0.6	0.1	32.7	32.6	32.4

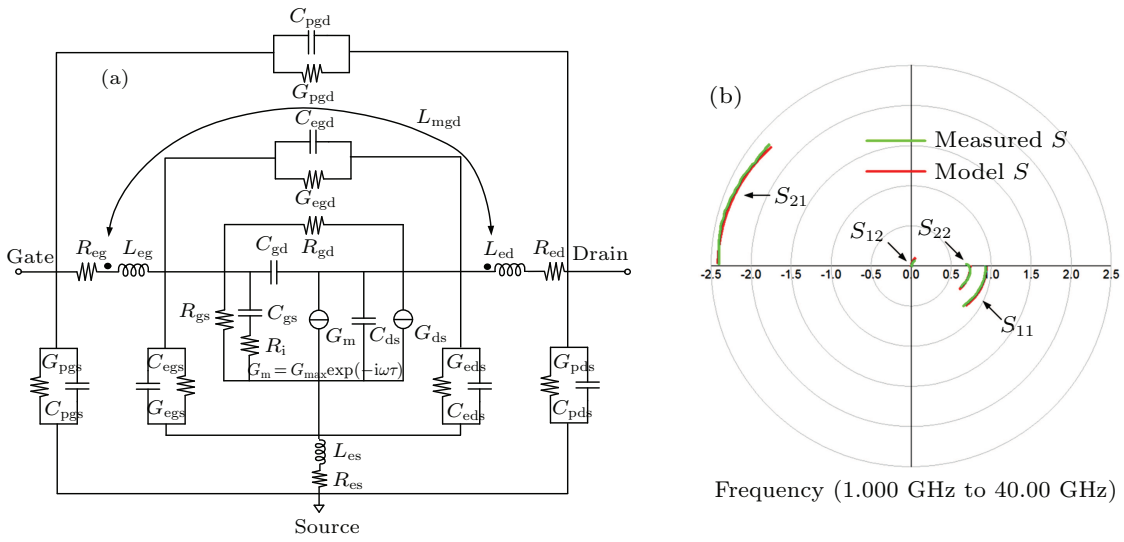


Fig. 12. (a) Small signal equivalent circuit model of InP HEMTs and (b) fitting result of *S*-parameters.

The next step in HEMT characterization is to evaluate the influence of parasitic couplings on the high-frequency performance of InP HEMT. In order to do so, the intrinsic small-signal equivalent-circuit parameters of a demonstrated device from our laboratory are combined with the extrinsic parasitic couplings extracted by using the full-wave simulation-based methodology described in this paper. The small signal equivalent circuit diagram of the complete InP HEMT can be obtained as shown in Fig. 12(a). After that, the topology is simulated and all values of parasitic parameters and intrinsic parameters are tuned to fit the model in the ADS. The fitting result of S parameters for the model is demonstrated in Fig. 12(b). As we can see, the curved portion in the low- and high-frequency range of S parameters can be fitted by the small signal equivalent circuit model, showing good fitting.

5. Conclusions

We have demonstrated an extrinsic equivalent circuit model for the parasitic coupling of a two-finger InP HEMT. In addition, using the equivalent circuit extraction method of HFSS and ADS co-simulation, the InP HEMT topology is systematically partitioned, and allows for the straightforward determination of parasitic circuit elements. In the process of co-simulation extraction, the gate–drain mutual inductance L_{mgd} is introduced to improve the incomplete accuracy of the conventional model in high frequency modeling. The feasibility of the parameter extraction method and the accuracy of the model are demonstrated via comprehensive comparisons between simulated and measured equivalent-circuit frequency responses of the proposed test standards on a bandwith of up to 40 GHz. Subsequently, the small signal modeling and fitting results of InP HEMT prove the accuracy of the parasitic model. Finally, the practicality of the HFSS EM simulation tool serving as an alternative to fabrication and measurement-based equivalent-circuit extraction is verified to be a cost-effective solution to optimizing the InP HEMT device performance.

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