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Fast-switching SOI-LIGBT with compound dielectric buried layer and assistant-depletion trench

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A lateral insulated gate bipolar transistor (LIGBT) based on silicon-on-insulator (SOI) structure is proposed and investigated. This device features a compound dielectric buried layer (CDBL) and an assistant-depletion trench (ADT). The CDBL is employed to introduce two high electric field peaks that optimize the electric field distributions and that, under the same breakdown voltage (BV) condition, allow the CDBL to acquire a drift region of shorter length and a smaller number of stored carriers. Reducing their numbers helps in fast-switching. Furthermore, the ADT contributes to the rapid extraction of the stored carriers from the drift region as well as the formation of an additional heat-flow channel. The simulation results show that the BV of the proposed LIGBT is increased by 113% compared with the conventional SOI LIGBT of the same length L_D. Contrastingly, the length of the drift region of the proposed device (11.2 μm) is about one third that of a traditional device (33 μm) with the same BV of 141 V. Therefore, the turn-off loss (E_{OFF}) of the CDBL SOI LIGBT is decreased by 88.7% compared with a conventional SOI LIGBT when the forward voltage drop (V_F) is 1.64 V. Moreover, the short-circuit failure time of the proposed device is 45% longer than that of the conventional SOI LIGBT. Therefor, the proposed CDBL SOI LIGBT exhibits a better V_F–E_{OFF} tradeoff and an improved short-circuit robustness.

Keywords: lateral insulated gate bipolar transistor, breakdown voltage, electric field modulation, turn-off loss

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1. Introduction

Because of the lower turn-on voltage, better thermal stability and easier integration,[1–3] silicon-on-insulator lateral-insulated gate bipolar transistors (SOI-LIGBTs) are common devices in power integrated circuits that are prevalent for example in automotive electronics and switching mode power supplies. The low forward voltage drop (V_F) arises a modulation in conductivity in the drift region during turn-on. Concurrently, many injected nonequilibrium carriers need to be extracted or recombined during turn-off. The shortcoming is that it leads to a large turn-off loss (E_{OFF}).[4–6]

One important challenge for power semiconductor devices of the LIGBT is to obtain an optimal compromise between V_F and E_{OFF}. The main ways of generating a better V_F–E_{OFF} trade-off are through: i) anode engineering including a shorted anode structure, a Schottky anode structure and a segmented NPN anode structure, which are realized by adding an extra carrier extraction channel;[7–10] ii) effectively accelerating carrier recombination by shortening carrier lifetime with high-power irradiations of protons and electrons,[11,12] and iii) creating deep oxide trenches that assist in sustaining the lateral field from the anode side, so as to increase the breakdown voltage (BV) and shorten the length of the drift region while maintaining a superior V_F–E_{OFF} trade-off.[13–15] Moreover, to optimize the distribution of surface electric field, an electric field modulation is introduced by adjusting the size and composition of the buried layer,[16,17] thereby improving BV and reducing the device pitch.

In this paper, a fast-switching SOI-LIGBT with compound dielectric buried layer (CDBL) and assistant depletion trench (ADT) is investigated and simulated. New electric field peaks are generated with the presence of the CDBL, resulting in a uniform distribution of the surface electric field and a shorter drift region length that improves the breakdown characteristics and reduces the total number of carriers stored in the drift region. Moreover, the stored carriers are extracted rapidly through an expedited depletion of the N-drift region by the ADT. Consequently, the proposed device exhibits a lower turn-off loss than a conventional SOI LIGBT. This study was performed by using Sentaurus device simulation tools, which contain models of the Enormal mobility, Auger recombination, high-field-saturation mobility, Philips unified mobility, Lackner avalanche generation, and the theory of Shockley–Read–Hall recombination.

2. Device structure and description

The SOI LIGBT (Fig. 1) comprises an oxide segment and a low-k dielectric segment that are alternately placed as a buried layer and both have the same thicknesses (T_{ox}). The relative permittivity k_I of the low-k dielectric layer increases from 1 to 3 with a step size of 0.5, and a k_I value near 1 is obtained by employing buried gaps of air or gas. The dielectric layer

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introduced into the buried air gap structure is formed by removing a SiGe layer using isotropic plasma dry etching.[18] In addition, a gas-dielectric process to achieve a minimum physically possible value for the dielectric constant was instigated in which the carbon trench in the buried layer reacts with oxygen in an oxidation furnace to form carbon dioxide gas.[19] With N being the number of alternately placed oxide and low-k dielectric segments, we set N_d and T_d as the concentration and thickness of the N-drift region, respectively. When the lateral length of the device is much larger than the vertical thickness of the top Si layer, breakdown occurs along the vertical direction. New electric field peaks are produced because of the variable-k buried layer, which raises the electric field at the surface of the substrate of different k_I and introduces electric field peaks on both sides of the p–n junction and the n–n$^+$ junction. This rise helps to produce a uniform surface electric field distribution and thus increase the BV.

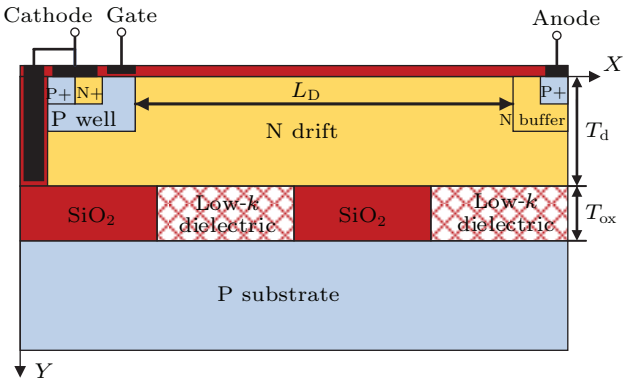


Fig. 1. Schematic cross-section of the proposed CDBL SOI LIGBT.

From another perspective, while maintaining the same BV value, both the length of the proposed device and the total number of stored carriers in the drift region decrease significantly. Hence, a superior V_F–E_{OFF} trade-off is obtained. The ADT consisting of an enclosed oxide and grounded polysilicon is located leftmost of the cathode and connected to the P+ cathode. The ADT reshapes laterally the electric potential distribution, which expedites the depletion of the drift region and generates an additional heat flow with the formation of a hole inversion layer along the ADT.

3. Results and discussion

Table 1 provides a list of the main simulation parameter settings for both the proposed structure and the conventional structure. The concentrations of the drift region for all devices are optimized to meet the reduced surface field (RESURF) condition. Because the dielectric at the interface between the top Si layer and the buried layer changes (Fig. 2), two new surface electric field peaks in the proposed device appear near M and N through the coupling of the electric field peaks for the new interface. Moreover, the new electric field peaks reduce the original electric field peak at the gate and drain edges, ensuring a more uniform electric field distribution within the proposed CDBL LIGBT structure. Furthermore, the lower k_I is, the higher the electric field peak is. When the minimum value of k_I is 1, the internal electric field peak reaches its maximum value, thereby improving the BV of the proposed CDBL LIGBT correspondingly.

Table 1. Design parameters of the two devices.

Symbol	Description	CDBL SOI LIGBT		SOI LIGBT
BV	breakdown voltage (V)	141	300	141
L_D	N-drift length (μm)	11.2	33.0	33.0
N_D	N-drift doping (cm^{-3})	3.2×10^{15}	4.7×10^{15}	3.0×10^{15}
T_d	N-drift thickness (μm)	2.0		2.0
T_{ox}	buried-layer thickness (μm)	1.0		1.0
k_I	relative permittivity	1.0–3.0		/

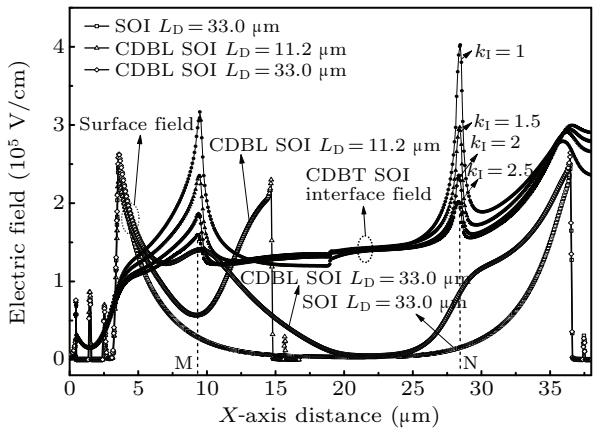


Fig. 2. Electric field distributions on the bottom interface of the Si/buried layer and the surface.

The simulation results of the surface electric potential distributions of a conventional SOI LIGBT ($L_D = 33$ μm, $k_I = 1$, $N = 4$ and $T_{ox} = 1$ μm) and the proposed CDBL SOI LIGBT ($L_D = 33$ μm and $T_{ox} = 1$ μm) at breakdown [Fig. 3(a)] show that their BVs are approximately 300 V and 141 V, respectively, despite the device size being the same. This shows that for the same L_D the BV of the proposed CDBL SOI LIGBT is 113% higher compared with the conventional SOI LIGBT. Furthermore, when maintaining the same BV of 141 V, the length of the drift region of the CDBL SOI LIGBT is 11.2 μm, which is approximate a third of the length (33 μm) of a conventional structure. Consequently, the CDBL of the proposed LIGBT creates a drift region of shorter length and a higher BV by modulating the electric field. The equipotential contour of the proposed CDBL LIGBT and the conventional SOI LIGBT at breakdown [Fig. 3(b)] manifest a laterally reshaped electric potential distribution in the structure because of the ADT, which expedites the depletion of the drift region and contributes to a fast extraction of the stored carriers in the off-state.

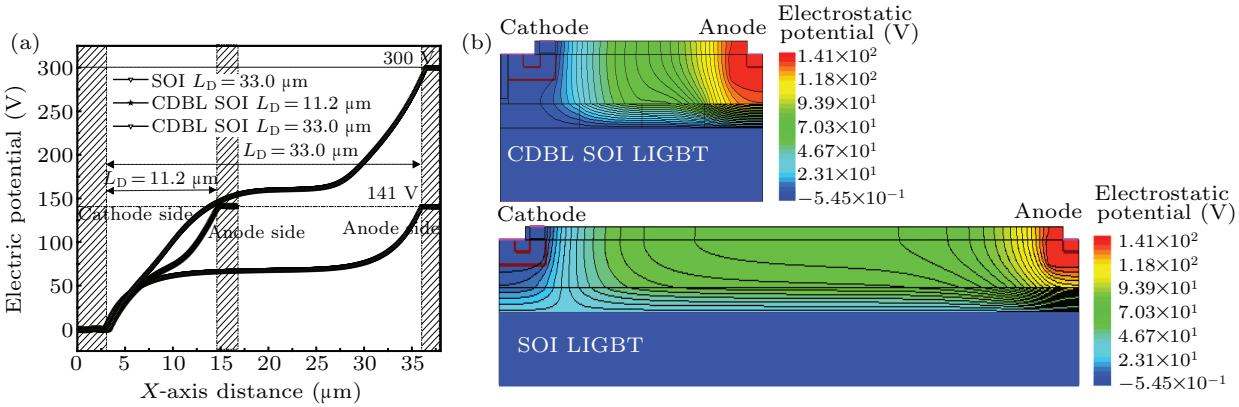


Fig. 3. (a) Horizontal surface electric potential distributions and (b) equipotential contour distributions of the proposed CDBL LIGBT and the conventional SOI LIGBT at breakdown.

The dependence of the BV on T_{ox} for various k_I [Fig. 4(a)] exhibits linearity with T_{ox} and an inverse proportionality with k_I. To better analyze this relationship, breakdown characteristics were investigated by using an analytical model taking into account the effects of electric field modulation. With a reverse bias applied to the device, the completely depleted drift region is divided up within the variable-k_I buried layer. The potential distribution function $\varphi_i(x,y)$ in each drift region satisfies the two-dimensional Poisson equation[20,21]

$$\frac{\partial^2\varphi_i(x,y)}{\partial x^2}+\frac{\partial^2\varphi_i(x,y)}{\partial y^2}=-\frac{qN_{di}}{k_s},$$
$$(i=1,2,3,\ldots,n,\ 0\le y<T_d). \tag{1}$$

Through applying a second-order Taylor series expansion, the potential distribution $\varphi_i(x,y)$ of the drift region in the y direction is expressed as

$$\varphi_i(x,y)=\varphi_i(x,0)+\frac{\partial^2\varphi_i(x,0)}{\partial y}y+\frac{\partial^2\varphi_i(x,0)}{2\partial y^2}y^2. \tag{2}$$

With imposing boundary conditions and the continuity of the electric potential, the surface potential distribution obtained by substituting Eq. (2) into Eq. (1) satisfies

$$\frac{\partial^2\varphi_i(x,0)}{\partial x^2}-\frac{\varphi_i(x,0)}{t_i^2}=-\frac{qN_{di}}{k_s}, \tag{3}$$

where t_i denotes the characteristic thickness, for which

$$t_i^2=\frac{1}{2}t_s^2+\frac{k_s}{k_i}T_dT_{ox}. \tag{4}$$

After a series of derivations and calculations, the surface potential at the interface of regions i and $i+1$ of the device is

$$V_i=\frac{\Psi_i t_{i+1}th(L_{di}/2t_i)+\Psi_{i+1}t_i th(L_{di+1}/2t_{i+1})+\frac{t_iV_d}{\sinh(L_{di+1}/t_{i+1})}}{t_{i+1}cth(L_{di}/t_i)+t_icth(L_{di+1}/t_{i+1})}, \tag{5}$$

where

$$\Psi_i=\frac{qN_{di}t_i^2}{k_s}. \tag{6}$$

Clearly, from Eqs. (4)–(6), the characteristic thickness t_i increases with increasing T_{ox} and decreases with increasing k_I. Accordingly, the BV also increases, which is consistent with the simulation results [Fig. 4(a)]. The drift region of the proposed CDBL SOI LIGBT is divided into N equal parts according to the different k_I of the buried layer. The maximum BV is 316 V when k_I is 1 and N is 2. Moreover, with increasing k_I, the BV has little effect on value N [see Fig. 4(b)].

The forward characteristics [Fig. 5(a)] of the conventional SOI LIGBT and the proposed CDBL SOI LIGBT with the same BV (141 V) show that, because of its shorter L_D of 11.2 μm, the latter acquires a lower V_F of 1.02 V at J_C = 100 A/cm^2 that is significantly less than V_F of 1.64 V for the conventional structure. The proposed device has a better current capability. The dependence of V_F on T_{ox} for different k_I [Fig. 5(b)] exhibits a linear relationship, and lower V_F values are obtained because of the optimal drift concentration. However, the functional relationship between V_F and k_I is weak and demonstrates that changes in k_I influence the forward conduction characteristics less, and V_F only changes by approximately 0.02 V between k_I from 3 to 1.

From the turn-off equivalent circuit [Fig. 6(a), inset], the inductive turn-off characteristics for the proposed CDBL SOI LIGBT (L_D = 11.2 μm) and the conventional SOI LIGBT (L_D = 33 μm) were obtained [Fig. 6(a)]. The turn-off time (T_{off} = 71.4 ns) for the CDBL SOI LIGBT is 48.9% lower than that of the conventional SOI LIGBT (T_{off} = 139.6 ns). In addition, the area of the overlapped region between the cur-

rent and voltage curves of the CDBL SOI LIGBT is smaller than that of the conventional SOI LIGBT during turn-off. The decrease indicates that the proposed structure gives a lower E_{OFF}. This is because the number of stored carriers in a drift region of shorter L_D is obviously lower. In addition, the ADT contributes by laterally reshaping the electric potential distribution and expediting the depletion of drift region. Therefore, by changing the concentrations of the P+ anode, lower E_{OFF} and V_F are obtained with the proposed CDBL SOI LIGBT [Fig. 6(b)]. By adjusting the anode concentration, the E_{OFF} of the CDBL SOI LIGBT is 88.7% lower than that of the conventional SOI LIGBT for the same V_F.

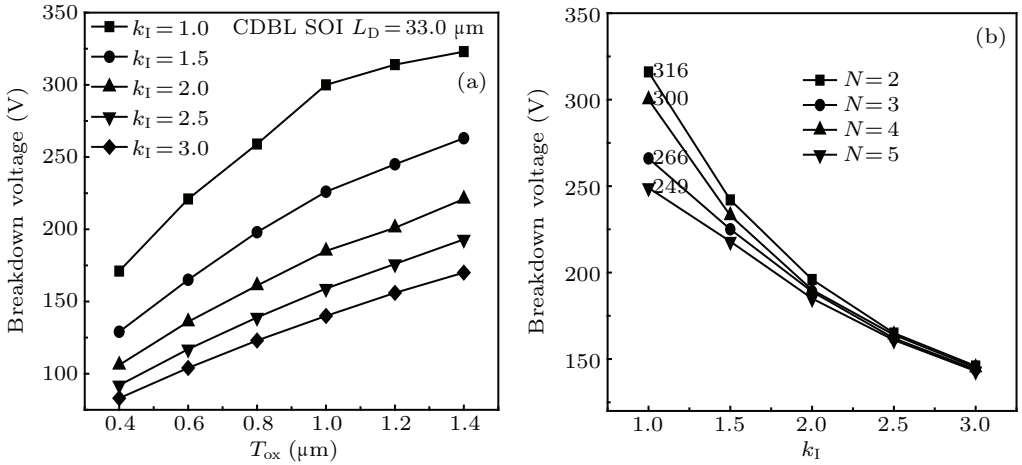


Fig. 4. BV as a function of T_{ox} and k_I: (a) BV versus T_{ox} and (b) BV versus k_I.

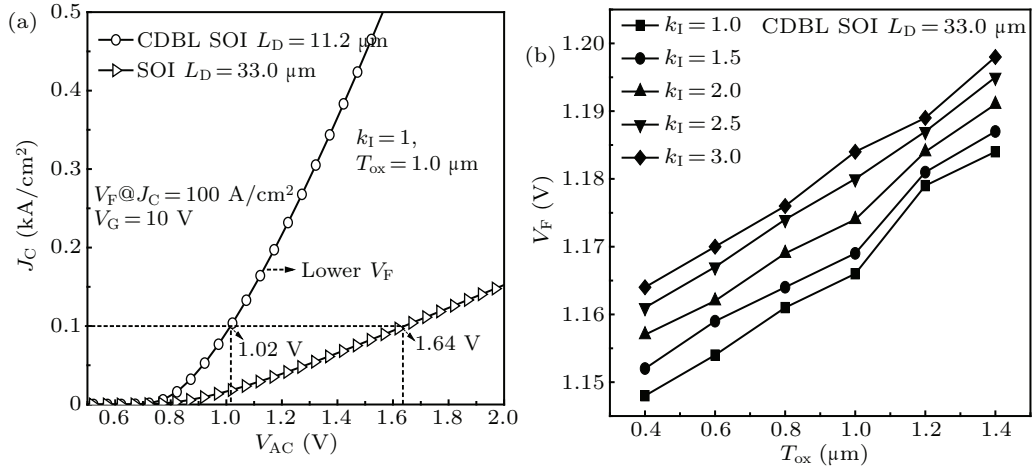


Fig. 5. Forward characteristics of the conventional and proposed structure: (a) profiles of the simulated forward characteristics and (b) V_F as a function of T_{ox} for various k_I.

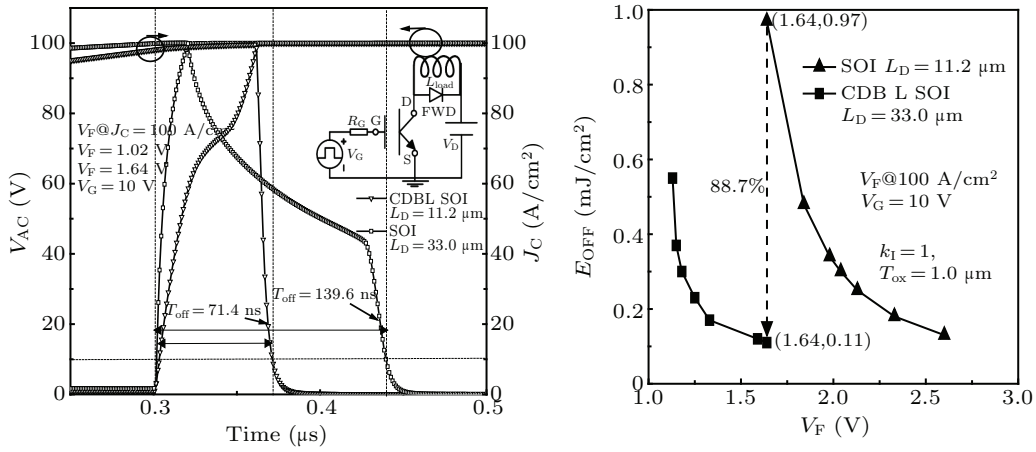


Fig. 6. (a) Inductive turn-off characteristics and (b) E_{OFF} versus V_F for the CDBL and conventional SOI LIGBTs.

A failure in self-heating appears during the on-state of the device when the intrinsic temperature of the device increases rapidly. A hole inversion layer is realized along the ADT of the proposed structure, which acts as an extra heat dissipation path during a short-circuit [Fig. 7(a)]. Therefore, the proposed CDBL SOI LIGBT exhibits a lower maximum lattice temperature (681 K) in comparison with the conventional SOI LIGBT (753 K) [Fig. 7(b)]. Correspondingly, the short-circuit failure time of the proposed CDBL SOI LIGBT is 45% longer than that of the conventional SOI LIGBT (Fig. 8), which indicates a better short-circuit robustness for the proposed structure.

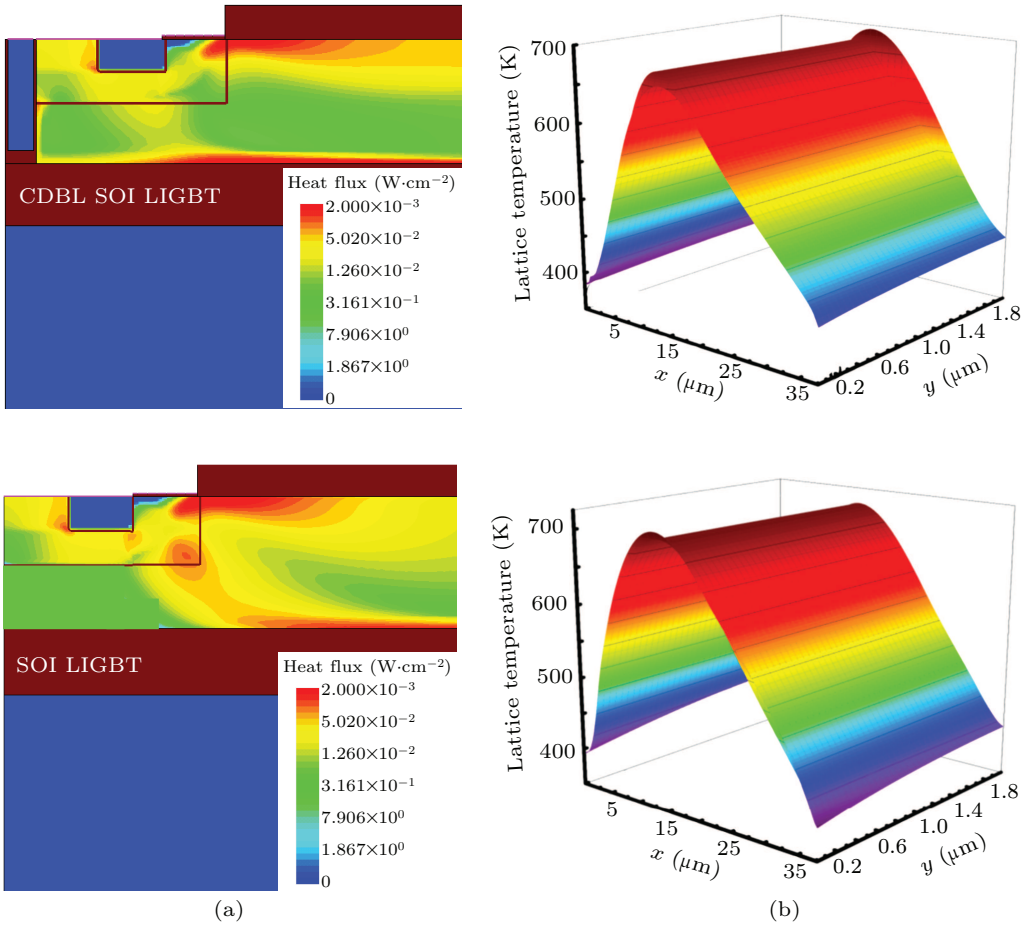


Fig. 7. (a) Hole heat flux distributions and (b) lattice temperature profiles for the CDBL and conventional SOI LIGBTs under short-circuit condition with $V_A = 80$ V.

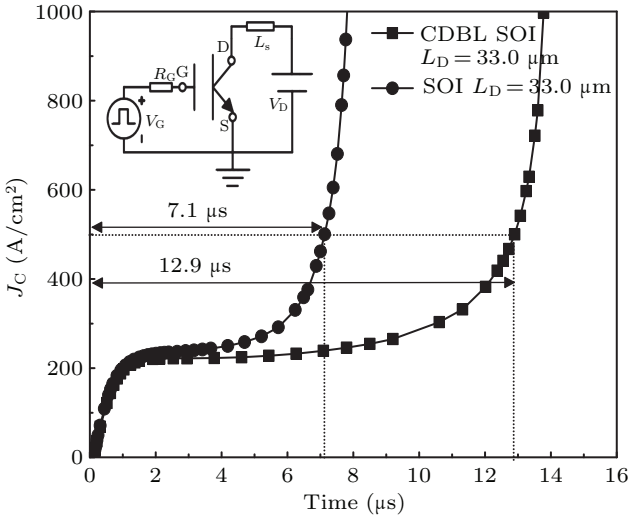


Fig. 8. Short-circuit waves for the CDBL SOI LIGBT and conventional SOI LIGBT.

The steps in fabrication of the proposed CDBL LIGBT are similar to those for a conventional SOI LIGBT [Fig. 9(a)]. One major difference between the two devices concerns the formation of the low k dielectric. In the flow of the low-k dielectric implementation process [Fig. 9(b)],[22] the trenches are firstly etched in the insulator film, which is located in the low k dielectric regions, and subsequently, carbon is produced during either a physical or a chemical vapor deposition, which fills up the trenches with carbon. Next, an approximately 50-nm-thick thin insulator film is deposited over the low k dielectric area. Finally, when oxygen is diffused through the thin layer of insulator, a thermal treatment of about 450 °C is performed in the oxygen atmosphere of the furnace. The carbon then reacts with oxygen to form carbon dioxide that pervades the spaces, thereby forming the ultra-low k dielectric regions.

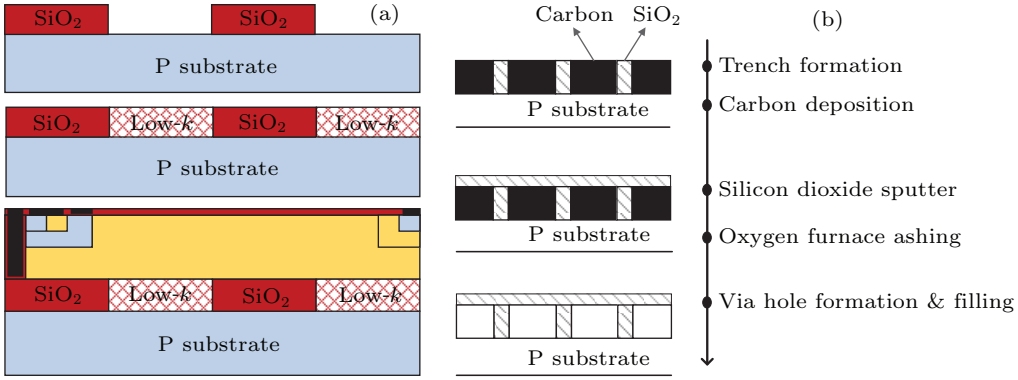


Fig. 9. Key process steps of the CDBL LIGBT: (a) basic process flows, (b) low k dielectric implementation process.

4. Conclusion

A SOI LIGBT with a CDBL and an ADT was proposed and investigated. By employing a CDBL, two electric field peaks were produced to optimize the surface electric field distributions. The BV of the LIGBT was improved as a result of a more uniform electric field distribution. Simulation results of the BV for the proposed CDBL SOI LIGBT showed an increase of 113% over that for the conventional SOI LIGBT under the same $L_{\rm D}$ condition. This increase leaded to a shorter length of the drift region and a smaller number of stored carriers, compared with the conventional SOI LIGBT. The proposed CDBL SOI LIGBT exhibited a better $V_{\rm F}$–$E_{\rm OFF}$ tradeoff. Moreover, aided by the ADT, a rapid extraction of the stored carriers and a high switching speed were achieved. We demonstrated also that self-heating within the proposed CDBL SOI LIGBT was alleviated effectively.

Acknowledgements

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