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Study on a novel vertical enhancement-mode Ga_2O_3 MOSFET with FINFET structure

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A novel enhanced mode (E-mode) Ga_2O_3 metal–oxide–semiconductor field-effect transistor (MOSFET) with vertical FINFET structure is proposed and the characteristics of that device are numerically investigated. It is found that the concentration of the source region and the width coupled with the height of the channel mainly effect the on-state characteristics. The metal material of the gate, the oxide material, the oxide thickness, and the epitaxial layer concentration strongly affect the threshold voltage and the output currents. Enabling an E-mode MOSFET device requires a large work function gate metal and an oxide with large dielectric constant. When the output current density of the device increases, the source concentration, the thickness of the epitaxial layer, and the total width of the device need to be expanded. The threshold voltage decreases with the increase of the width of the channel area under the same gate voltage. It is indicated that a set of optimal parameters of a practical vertical enhancement-mode Ga_2O_3 MOSFET requires the epitaxial layer concentration, the channel height of the device, the thickness of the source region, and the oxide thickness of the device should be less than 5×10^{16} cm^{-3}, less than 1.5 μm, between 0.1 μm–0.3 μm and less than 0.08 μm, respectively.

Keywords: gallium oxide, E-mode, device simulation, threshold voltage

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1. Introduction

The monoclinic β-phase of gallium oxide (Ga_2O_3) is one of the promising ultra-wide bandgap (UWBG) materials for power device application due to its fundamental properties and a low-cost manufacturable native substrate,[1,2] such as large bandgap E_g of $\sim$ 4.9 eV, critical electric field E_c of 8 MV/cm, and electron saturation velocity υ_{sat} of 1.8×10^7 cm/s–2.0×10^7 cm/s. In recent years, the research on Ga_2O_3 metal–oxide–semiconductor field-effect transistor (MOSFET) devices is more in-depth worldwide,[4–12] such as Ga_2O_3 vertical MOSFET with $V_{br} > 1$ kV is published.[12] Ga_2O_3 MOSFET is becoming a major breakthrough in the research of high temperature, voltage, and power devices. Due to the low donor energy level ($E_c - 0.04$ eV) formed by the oxygen vacancy in the growth process, the β-Ga_2O_3 is an n-type semiconductor. However, due to the large hole effective mass and the self-trapping effect, the p-type doping of Ga_2O_3 has not achieved adequate practical progress so far.[3] The research of Ga_2O_3 based MOSFET devices mainly focuses on the depletion-mode (D-mode),[4–7] and the more in-depth studies of enhancement-mode (E-mode) MOSFET are urgently pending.[8–10] Because the MOSFET worked in enhanced mode operation with $V_{th} > 0$ V is considered to work as a preferred safety mode.[11,12]

Technology-Computer-Aided-Design (TCAD) provides a practical approach to understand the device physics. Up to now, there have been many works on the TCAD simulation of β-Ga_2O_3 transistors, especially in the vertical MOSFET.[13–21] Researchers have gained comprehensive knowledge of the material characteristics of Ga_2O_3 single crystal and significantly promoted the incomplete ionization model, mobility model, energy band model, collision ionization model, high field mobility model, temperature dependence model of gallium oxide for practical device simulation. The simulation work of the Ga_2O_3 device currently remains on the change of characteristic regularity and trend, thus lacking the capability to precisely quantify the electrical parameters of the device, such as the breakdown voltage (V_{br}), the maximum electric field strength, the output, and the transfer characteristics of the device. The vast deviations regarding the device performances between the simulation and the experiments are critical issues hindering Ga_2O_3 device design and broader applications.[22,23]

This paper reports establishing the basic model of vertical E-mode Ga_2O_3 MOSFET by TCAD and demonstrating the model's correctness by combining it with the experimental data. Experimental data verify the correctness of the model, and the device structure is optimized considering the output

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current and threshold voltage.

2. Simulation details

2.1. Bandgap model

The bandgap (E_g) of Ga_2O_3 is set as 4.85 eV at room temperature. According to the equation,[24] the relationship between E_g and the lattice temperature (T) is as follows:

$$E_g(T) = 5.0243 - dE_g/dT \times (T+\beta)^{-1}, \quad (1)$$

where T is the lattice temperature, $dE_g/dT = 4.45 \times 10^3$ (eV/K), β is 2000 K.

2.2. Effect of incomplete ionization and compensation doping

Since the incomplete ionization and compensation doping have a significant influence on the electrical properties of Ga_2O_3 devices, especially in the drift region, the model of the incomplete ionization state of donor energy level is established as follows:[19]

$$E_D = E_{D0} - \alpha_{ion} N_D^{1/3}, \quad (2)$$

where E_{D0} is the zero doping ionization energy, which is 36.3 meV, α_{ion} is 2.0609×10^{-8} eV·cm (effective electronic mass is $0.28m_0$, and the effective density of states (N_C) of the local conduction band is 3.67×10^{18} cm^{-3}).[20]

2.3. Mobility model

For power Ga_2O_3 MOSFET, mobility is one of the essential electrical parameters, and modeling usually considers factors such as the doping concentration, the high field saturation effect, and the surface effect. Because electrons flow in a vertical MOSFET's fin center, the surface effect does not play an important role. The low electric field mobility of Ga_2O_3 is usually used as follows:[21]

$$\mu_{low} = \mu_0 \times \left(\frac{T}{300}\right)^{-T_{mun}}, \quad (3)$$

where μ_{low}, μ_0, T, and T_{mun} are the low field mobility, the initial mobility, the lattice temperature, and temperature coefficient, respectively. The μ_0, and the T_{mun} were 118 cm^2·V^{-1}·s^{-1} and 2.0.[21]

According to the nonlinear relationship between the carrier drift velocity and the electric field, the high-field saturation mobility is calculated based on the Caughey–Thomas velocity saturation model[25]

$$\mu_{high\ field} = \frac{\mu_{low}}{[(1+\mu_{low}E/\upsilon_{sat})^{\beta}]^{1/\beta}}, \quad (4)$$

where υ_{sat} is the saturation drift velocity of the carrier and E is the electric field. Because the [001] direction is the preferred direction for fabricating β-Ga_2O_3 vertical MOSFETs, the optimization of stimulation parameters is conducted only along the z direction, corresponding to [001] orientation. The carrier saturation drift velocity υ_{sat} in Ga_2O_3 is about 1.708×10^7 cm/s.[26] The formula of parameters β are the same as that of the Si $\beta(T)$ relationship, as follows:[5]

$$\beta(T) = \beta_0 \times (T/300)^{0.66}, \quad (5)$$

where β_0 is set to 6.97 at [001] direction.

For vertical MOSFET, the doping-dependent mobility is calculated based on the Arora model[17] as follows:

$$\mu_{doping} = \mu_{min} + \frac{A_d}{1+(\frac{N_{A,0}+N_{D,0}}{N_0})^{A^*}}, \quad (6)$$

$$\mu_{min} = A_{min} \cdot \left(\frac{T}{300}\right)^{\alpha_m}, \quad \mu_d = A_d \cdot \left(\frac{T}{300}\right)^{\alpha_d}, \quad (7)$$

$$N_0 = A_N \cdot \left(\frac{T}{300}\right)^{\alpha_N}, \quad A^* = A_a \cdot \left(\frac{T}{300}\right)^{\alpha_a}, \quad (8)$$

where A_{min}, A_d, A_N, and A^* are parameters related to Ga_2O_3 materials.[16]

2.4. Device structure

The simulated structure and related parameters of the vertical Ga_2O_3 MOSFET is shown in Fig. 1 and Table 1.

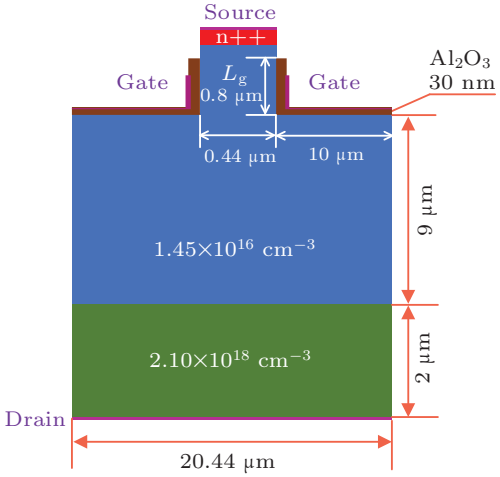


Fig. 1. Structure of vertical gallium oxide MOSFET. The green area is drain area, the blue area is epilayer film, the red area is source area.

Table 1. Structural parameters of the vertical Ga_2O_3 MOSFET.

Structural parameters	Vertical Ga_2O_3 MOSFET
Thickness of drain area (H_{drain})	2 μm
Thickness of epilayer (H_{drift})	9 μm
Doping concentration of epilayer (N_{epi})	1.45×10^{16} cm^{-3}
Doping concentration of source (N_{source})	5×10^{19} cm^{-3}
Doping concentration of drain (N_d)	10^{18} cm^{-3}
Thickness of source area (H_s)	0.1 μm
Space length of source and gate (H_k)	0.1 μm
Height of Fin (L_g)	0.8 μm
Width o f Fin (W_g)	0.44 μm
Workfunction of gate (Φ_m)	5.65 eV
Width of gate (W)	10 μm

3. Results and discussion

Figure 2 shows the transfer curve and the output curve obtained by TCAD, whcih are consistent with the experimental results.[23] In Fig. 2(a), the threshold voltage (V_{th}) obtained is 0.24 V (V_{th} is defined as the gate voltage when $I_{ds} = 0.1$ mA/cm^2). In Fig. 2(b), the I_{ds} is microampere level when the gate voltage is less than 0 V. I_{ds} in the saturation region and the I_{ds} with TCAD are 22.7% and 6.9% smaller than the literature values, respectively.[23] This is because $\mu_0 = 118$ cm^2·V^{-1}·s^{-1} used in the Arora model comes from practical measurement, which is not particular optimized for simulation. We note that the output saturation current of the device will increase with increasing μ_0, and the simulation results and experimental can reach better consistency.

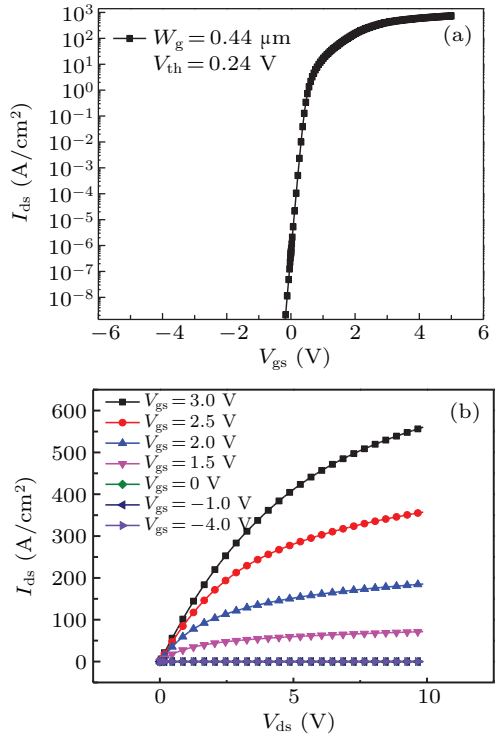


Fig. 2. (a) Transfer characteristics and (b) output characteristics of vertical Ga_2O_3 MOSFET.

Figure 3 shows the output and transfer characteristic curve of different gate metals with different work functions. It shows that the output current density decreases, and the threshold voltage increases with the increasing of work function. As the metal work function is rising up to 5.95 eV, the device operation will change from depletion device to enhancement device. In order to realize the E-mode MOSFET device, the material with a large gate metal work function should be chosen, such as Au and Pt for Ga_2O_3 devices.

Figure 4 shows the output and the characteristic transfer curves with different gate oxide materials under the oxide layer thickness (H_O) is 30 nm. The I_{ds} of the device with the HfO_2 layer increases with the increase of the dielectric constant of the gate oxide material. The threshold voltage reaches the maximum when I_{ds} and V_{th} with SiO_2 layer are the minimums at the same thickness, which is attribute to I_{ds} and V_{th} increasing with the increase of the oxide layer's dielectric constant (ε_{ox}).

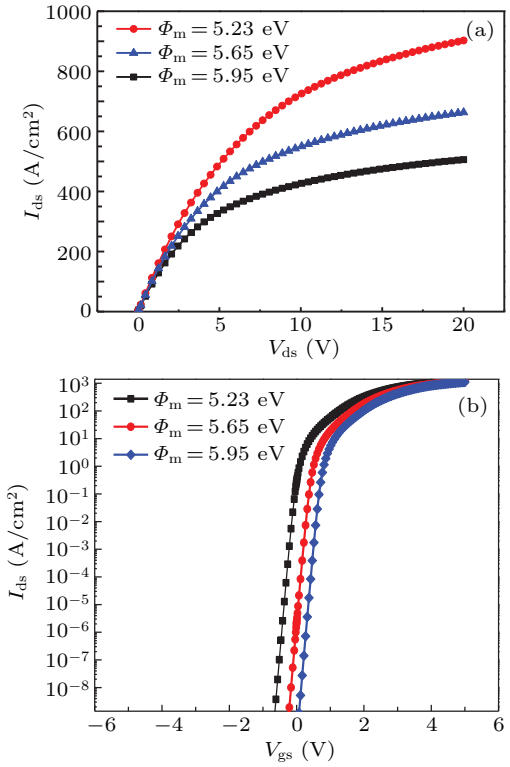


Fig. 3. (a) Output curves and (b) transfer characteristic curves of the device with different metal work functions.

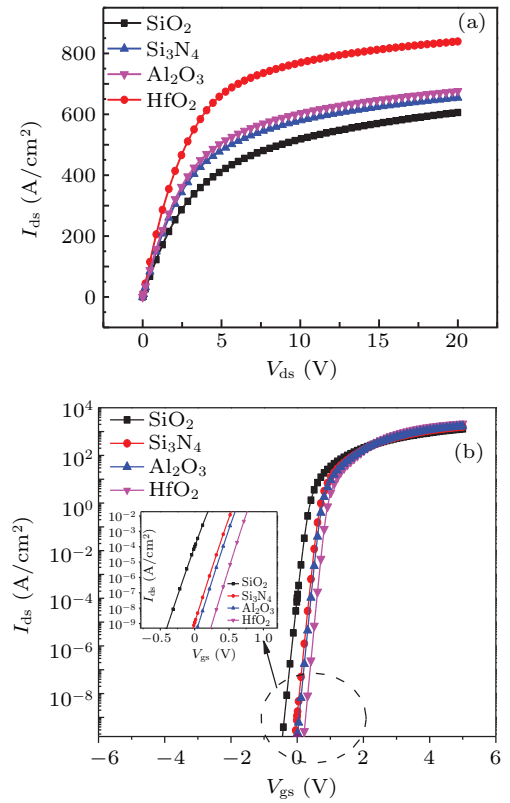


Fig. 4. (a) Output curves and (b) transfer characteristic curves of the device with different gate oxide materials.

Figure 5 shows the output and transfer characteristic curves with different epilayer concentrations ($N_{\rm drift}$). The output current density increases, and the threshold voltage decreases with the increase of epitaxial layer concentration. With the increase of epitaxial layer concentration, the hole concentration in the depletion region of the device channel becomes smaller and easier to be turned on under the same gate metal condition so that the threshold voltage will shift to the left. The results indicate that the epitaxial layer concentration should not exceed 5×10^{16} cm^{-3}.

Figure 6(a) shows the transfer characteristic curve of channel height ($L_{\rm g}$) at different channel heights. It can be seen from the curves that the output current density decreases, and the threshold voltage increases with the increase of channel height. The resistance in the channel region increases with the increase of $L_{\rm g}$, leading to the current decreasing and the threshold voltages shift to the right, as shown in Fig. 6(b). With the increase of channel height, the increase of threshold voltage decreases gradually, and the output current decreases significantly, suggesting that the channel height should be smaller than 1.5 μm.

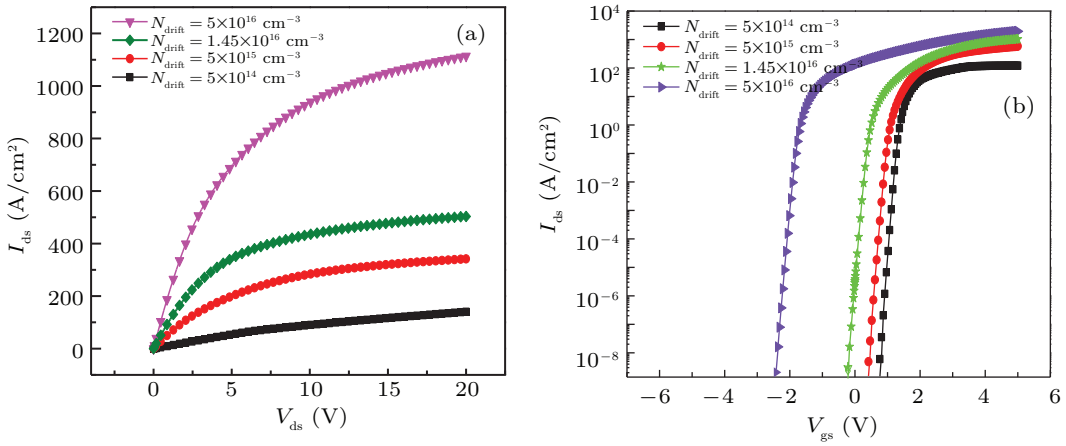


Fig. 5. (a) Output curves and (b) transfer characteristic curves of the device with different epilayer concentrations.

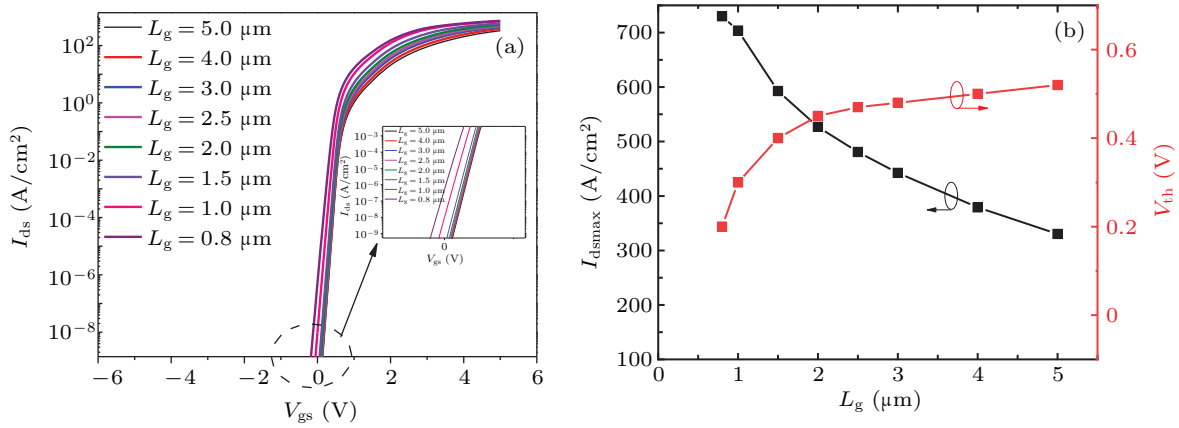


Fig. 6. (a) Transfer curves and (b) characteristics comparison at different channel heights.

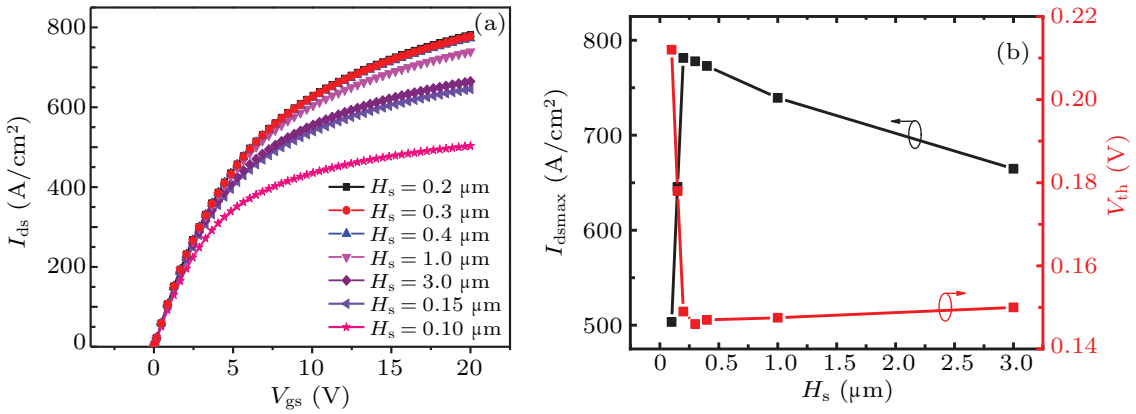


Fig. 7. (a) Transfer curves and (b) characteristics comparison at different source heights.

Figure 7(a) shows the output curves with different heights of the source region (H_s). It can be seen from Fig. 7(b) that with the increase of the source height, the output current density increases firstly and then decreases. Threshold voltage firstly decreases and then increases. With the increase of the source height, the depletion of the channel undermines, and the current density increases. When the source thickness is more than 0.2 μm, the L_g and the resistance become rising, and the current decreases. The device's threshold voltage is mainly related to the concentration and width of gate metal and channel area. Therefore, the source area thickness of the device is set at 0.1 μm–0.3 μm is more suitable.

Figure 8 shows the output transfer characteristic curves with different oxide layer heights (H_O). It can be seen from the curves that with the increase of oxide layer height, the output current density first decreases and then increases. Due to the work function difference between the gate metal and the semiconductor, the device's channel is in the depletion state, and the device is turned off. When the thickness of the gate oxide layer is reduced, the gate voltage is easier to control the formation of holes, and the depletion region is easier to form, leading to an increase of the threshold voltage of the device. When the device is turned on, the output current increases with decreasing the oxide layer's height. When the thickness of the oxide layer is beyond 0.13 μm, the threshold voltage becomes negative. Therefore, the oxide thickness of the device should not exceed 0.08 μm.

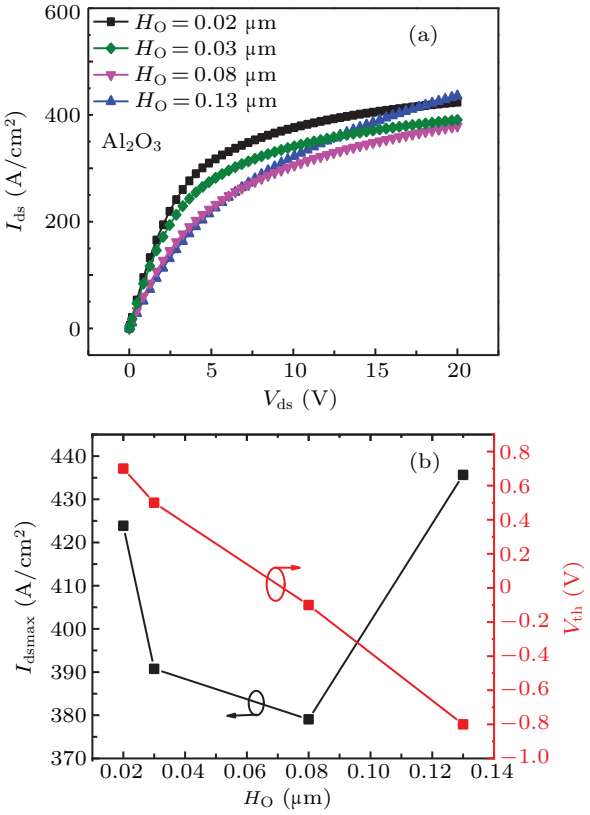


Fig. 8. (a) Out curves and (b) characteristics comparison with different oxide layer heights.

Figure 9 shows the output and transfer characteristics of different channel widths (W_g). The output current density and the threshold voltage decrease with the increase of channel width. The cross-sectional area of current flow increases, and the resistance of channel area decreases with the increase of channel width at the same channel length so that the output current will increase with the increase of channel width. At the same gate voltage, the resistance in the channel region of the device becomes smaller and easier to turn on, and the threshold voltage will shift to the left.

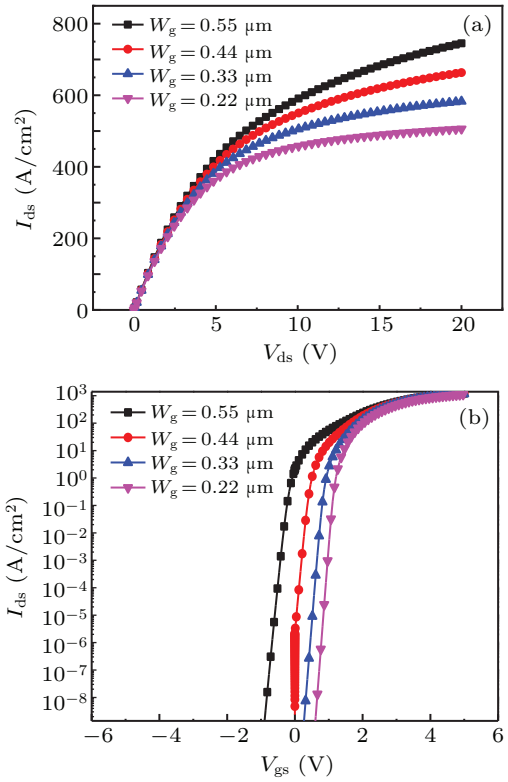


Fig. 9. (a) Output curves and (b) transfer characteristic curve of the device with different drift heights.

Through simulation above, it can be found that the width and height of source "fin" will have a significant impact on the performance of the device. Therefore, the high precision etching process is the key step to achieve this device. In addition, the covering ability of the gate electrode on the "fin" mesa also has influence on the gate control of the device.

4. Conclusion

Based in TCAD simulation and experimental data verification, we propose an improved Ga_2O_3 model for Ga_2O_3 MOSFET device simulations. Based on the established model, the static characteristics of vertical Ga_2O_3 MOSFET are calculated by the TCAD simulation software. The simulation results are in good agreement with the experimental results giving rise to optimization simulation parameters of the device. Through the optimization of the gate metal work function, the channel length, the width, the gate oxide material,

the thickness, the epitaxial layer concentration thickness, the source region thickness, the concentration are included in the simulation. We found that the gate metal material, the oxide layer thickness and material, the source region concentration, the epitaxial layer concentration, the source region thickness, and the source region concentration are the key factors. The channel region's width and height greatly influence the output current, while the gate metal material, the thickness of the oxide layer, and the concentration of material and epitaxial layer greatly influence the threshold voltage. According to the simulation results, materials with a large gate metal work function and large oxide dielectric constant should be chosen for fabricating the E-mode MOSFET device. The epitaxial layer concentration should not exceed 5×10^{16} cm^{-3}, and the channel height of the device should be smaller than 1.5 μm. The thickness of the source area is set at 0.1 μm–0.3 μm. The thickness of the oxide layer should be less than 0.08 μm. Our findings from the theoretical calculations are omportant guidelines in designing and manufacturing the Ga_2O_3 MOSFET device.

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