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Observation of source/drain bias-controlled quantum transport spectrum in junctionless silicon nanowire transistor

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We investigate the influence of source and drain bias voltages (V_{DS}) on the quantum sub-band transport spectrum in the 10-nm width N-typed junctionless nanowire transistor at the low temperature of 6 K. We demonstrate that the transverse electric field introduced from V_{DS} has a minor influence on the threshold voltage of the device. The transverse electric field plays the role of amplifying the gate restriction effect of the channel. The one-dimensional (1D)-band dominated transport is demonstrated to be modulated by V_{DS} in the saturation region and the linear region, with the sub-band energy levels in the channel ($E_{channel}$) intersecting with Fermi levels of the source (E_{fS}) and the drain (E_{fD}) in turn as V_g increases. The turning points from the linear region to the saturation region shift to higher gate voltages with V_{DS} increase because the higher Fermi energy levels of the channel required to meet the situation of $E_{fD} = E_{channel}$. We also find that the bias electric field has the effect to accelerate the thermally activated electrons in the channel, equivalent to the effect of thermal temperature on the increase of electron energy. Our work provides a detailed description of the bias-modulated quantum electronic properties, which will give a more comprehensive understanding of transport behavior in nanoscale devices.

Keywords: junctionless nanowire transistors, quantum transport spectrum, source and drain voltage, low-temperature conductance

PACS: 77.55.df, 85.30.–z, 05.60.Gg, 61.46.Km **DOI:** 10.1088/1674-1056/ac21ba

1. Introduction

The sub-7-nm downscaling of complementary metal–oxide–semiconductor (CMOS) technology is reaching fundamental limits that could spell the end of Moore's scaling law. Nowadays junctionless silicon nanowire field-effect transistor (JNT) is considered as a potential candidate for sub-7-nm CMOS node due to its simplified manufacturing technology and outstanding gate controllability.[1,2] In such nanoscale dimensions, the electronic transport characteristics of the device can perform quite differently from those in bulk silicon.[3,4] Indeed, the reduction of device dimensions enhances the importance of quantum mechanical effects.[2,5,6] For example, the conductance oscillation of nanowire transistors caused by inter-sub-band scattering in one-dimensional (1D) transport,[7,8] the single-electron tunneling current and quantum interference originated from the impurity energy levels of the dopants.[9–14] The transport characteristics of the nanoscale device are investigated more at low source/drain bias voltage below kT/q (T is temperature, k is Boltzmann constant, and q is electron charge, normally $kT/q = 0.5$ mV at $T = 6$ K) to keep stable performance and protect the device from failure.[15–17] However, studying the electrical transport behavior of nanowire transistors at higher bias voltages is of significant importance for comprehensively understanding the transport mechanism in nanoscale quantum devices in both saturation region and linear region, which is even potential for the moderation mechanism of the quantum device in the future. With a specially designed extremely thin but long junctionless nanowire, the risk of high V_{DS} destructive influence can be dramatically reduced. In our work, we investigated the source/drain-voltage-controlled quantum sub-band electrical transport spectrum in our 10-nm width and 485-nm length N-typed junctionless nanowire transistor under the temperature of 6 K. We observed that the drain-source voltage has a limited influence on the threshold voltage of the device and the single-electron tunneling below the threshold voltage. The transverse electric field introduced from V_{DS} plays the role of amplifying the gate restriction effect of the channel. The 1D sub-band dominated transport is demonstrated to be modulated by V_{DS} in different ways in the saturation region and

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the linear region. We observed two sets of conductance fluctuations, which are related to the sub-band energy levels in the channel (E_{channel}) intersecting with the Fermi levels of the source (E_{fS}) and the drain (E_{fD}) in turn as V_{g} increases. We also find that the bias electric field has the effect to accelerate the thermally activated electrons in the channel, equivalent to thermal temperature on the increase of electrons energy. Our work provides a more comprehensive understanding of transport behaviors at nanoscale devices under the influence of changing source/drain bias voltages.

2. Device fabrication

Our device was based on the 55-nm-thick top silicon layer of the (100)-oriented silicon-on-insulator wafer. First, a 30-nm-thick oxidation layer was formed by thermal oxidation, following the phosphorus ion implantation of a dose of 1×10^{13} cm^{-2} on the top silicon layer with an energy of 33 keV. We used electron beam lithography (EBL) to define the silicon nanowire and then used inductively coupled plasma (ICP) etching to complete the pattern transfer process. To reduce the etching-induced damages, a sacrificial oxidation process after ICP etching was essential. During this step, we oxidized about 25-nm sacrificial SiO_2 layer under 900-°C dry oxygen and then removed the layer with HF corrosion to further reduce our silicon nanowire. Then the 10-nm-thick gate oxide layer was formed by thermal oxidation under 900-°C dry oxygen. Next, with the help of low pressure chemical vapor deposition (LPCVD) equipment, the gate material layer — the 200-nm-thick polysilicon layer was deposited on the oxide silicon nanowire. Then the sample was annealed in 1000-°C nitrogen ambient for 15 s after boron ion implantation. The 485-nm-long polysilicon gate which wrapped the Si/SiO_2 core–shell nanowire was defined by electron beam overlay exposure and ICP etching. Finally, the 200-nm-thick SiO_2 passivation layer was deposited, followed by the standard Ni/Al metal contact formation. The SEM image of the single-channel JNT in the inset of Fig. 1 shows the width of 30 nm for the Si/SiO_2 core-shell nanowire. As a result, we can estimate the silicon core has a physical width of about 10 nm. The estimated height after three times thermal oxidation processes should also be around 10 nm. Besides, the dopant concentration of the silicon channel is estimated to be 1×10^{19} cm^{-3} according to the implantation dose of phosphorus ions. The fabricated device was measured in a vacuum chamber which can be cooled down to the low temperature of 6 K with the help of a Lakershore-340 temperature controller. Figure 1 shows the transfer characteristics of the device at room temperature. It can be seen that the subthreshold slope of the device at room temperature is 77 mV/dec, and the cut-off current is in the order of 10^{-13} A.

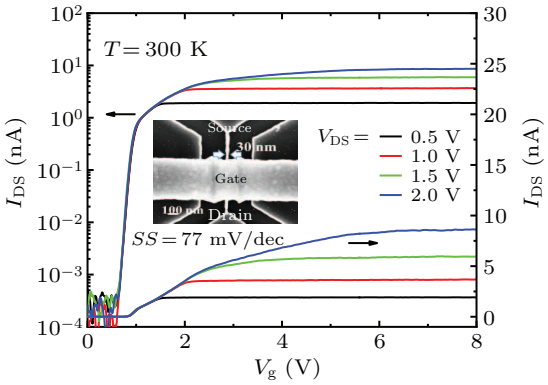


Fig. 1. Transfer characteristics of the device at room temperature. The inset is the SEM image of our silicon nanowire after gate formation.

3. Transport spectrum results and discussion

3.1. Low-temperature current characteristics

Figure 2 shows the current *versus* gate voltage transfer curves under different V_{DS} bias voltages ($V_{\text{DS}} = 0.4$ V–2.3 V) at a low temperature of 6 K. Below the threshold region, a current peak is observed at $V_{\text{g}} = 1$ V for all V_{DS} drain biases. This current peak is attributed to single-electron tunneling between doping impurities in the channel, which has negligible dependence on the transverse electric field.[18] The current curves of all V_{DS} bias voltages begin to increase dramatically above the threshold voltage $V_{\text{th}} = 2$ V, with several similar current steps (seen from the black circle in Fig. 2).

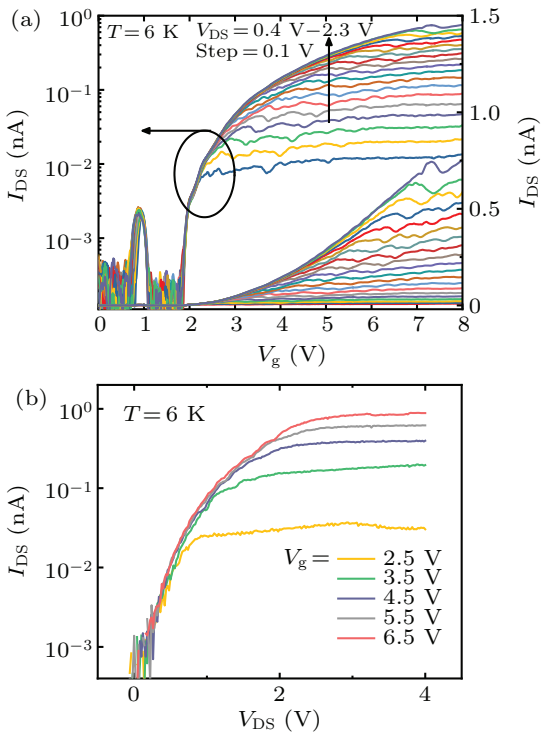


Fig. 2. (a) Transfer characteristic curves under the V_{DS} bias voltages from 0.4 V to 2.3 V at the temperature of 6 K, with curves in log coordinate on the left side and linear coordinate on the right side. (b) The corresponding output curves of the device at the temperature of 6 K.

The transverse electric field is indicated to have less influence on the turn-on position of the device. Interestingly,

the conductive currents show obvious fluctuations after the device turning on. The positions of these conductance fluctuations shift to the right with V_{DS} voltage increasing. Figure 2(b) shows the corresponding output curves with the source/drain voltage V_{DS} changing from 0 V to 4 V, from which we can see that the transfer curves under the source/drain voltage range (0.4 V–2.3 V) in our main discussion part are absolutely in the safe conductive range of the device. The following part of our paper will focus on the influence of source and drain voltages on these interesting transfer characteristics of our device.

3.2. Threshold characteristics with V_{DS} voltage changing

The threshold position of the device is also related to the position of the edge of the conduction band in the channel. The exact position of the conduction band edge can be obtained from the extended line of the activation energy E_a with the V_g axis, where the energy of the electrons in the channel is already enough energy for jumping into the next state that does not need additional activation energy ($E_a = 0$). Figure 3 shows the activation energy E_a plots under different V_{DS} bias voltages from 0.5 V to 2.0 V, with the comparison of the corresponding current curves. The activation energies E_a are extracted from the temperature-dependent conductance of the device at the room-temperature segment ($T = 250$ K–300 K) which are proportionated to $\exp(-E_a/k_B T)$, where k_B is the Boltzmann constant. Interestingly, the tangent lines of the activation energy (E_a) of all bias voltage settings intersect with the horizontal axis (V_g) at the same position, *i.e.*, the edge of the conduction band, at $V_g = 2.0$ V,[19] indicating that the conduction band edge in the channel is highly dependent on the gate voltage, but has less dependence on the source/drain voltages. Correspondingly, the current curves also start to increase rapidly from this conduction band edge position for all bias voltages, which is exactly the evidence of the position of the threshold voltage (V_{th}).[20] Generally, the highest Fermi energy position in the channel should reach the Fermi level of the source pool at $V_g = V_{th}$, where the energy barrier between the source and the channel should diminish, resulting in the device turning on. The transverse electric field introduced from source and drain voltage has quite limited influence on the highest channel energy level close to the source region, as well as the energy barrier between the channel and the source pool, resulting in the independence of the V_{th} position on V_{DS} voltage. Besides, we also noticed that the room-temperature activation energy at the high V_g conductive region decreases from 176.5 meV to 95.9 meV with V_{DS} bias voltage increasing from 0.5 V to 2.0 V. This is due to that the bias electric field can highly accelerate the thermally activated electrons in the channel, equivalent to thermal temperature on the increase of electron energy.

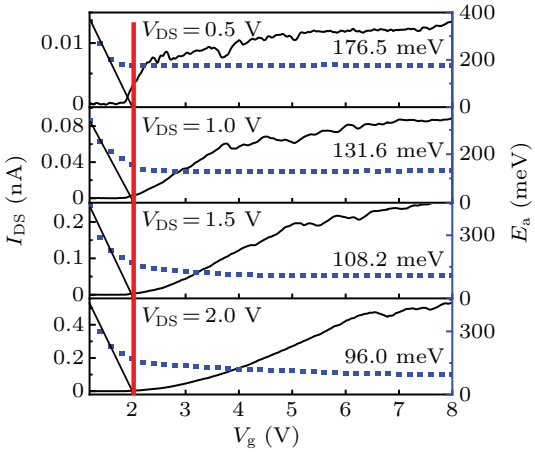


Fig. 3. The current with corresponding activation energy curves for various V_{DS} bias voltages, $V_{DS} = 0.5$ V, 1.0 V, 1.5 V, 2.0 V.

3.3. Transport spectrum beyond the threshold voltage under the influence of V_{DS}

To further explore the mechanism of the current fluctuations in Fig. 2 after the threshold voltage, figure 4 shows the three-dimensional (3D) transconductance (g_m) data for various V_g from 0 V to 8 V and V_{DS} from 0.4 V to 2.3 V at the temperature of 6 K. Clearly, the regular transconductance fluctuations with the stable V_g spacing (ΔV_g) of 0.81 V, 0.81 V, 0.59 V, 0.83 V, 1.07 V, respectively (marked in red arrows in Fig. 4) move linearly to higher V_g section with V_{DS} bias voltage increasing. Let us first focus on these consistent set of fluctuation spacings. The corresponding energy intervals between sub-bands are calculated by[5]

$$\Delta E_{exp} = (\pi\hbar C_{ox}/2m^* e) \times \Delta V_{GS}, \tag{1}$$

as 91.3 meV, 91.3 meV, 66.5 meV, 93.6 meV, and 120.6 meV, where the oxide layer thickness d_{ox} in C_{ox} is 10 nm. To study these energy spacings, we calculate the theoretical spacings between discrete sub-bands of silicon nanowire caused by 1D quantum confinement[21] through

$$E_{m,n} = (\hbar^2\pi^2/2m^*) \times \left[(m/W)^2 + (n/H)^2\right], \tag{2}$$

where the effective mass of electron m^* is $0.2m_0$. W and H are the channel width and height, and m, n are quantum numbers in two directions ($m, n = 1, 2, 3, \ldots$). From this equation, the 1D theoretical energy intervals are calculated as 92.6 meV, 92.6 meV, 61.7 meV, 92.6 meV, 123.5 meV, supposing $W = H = 8$ nm. We can find that the theoretical results are highly consistent with the sub-band energy level spacing observed in the inset of Fig. 4. Therefore, we demonstrate that these regular fluctuations are caused by inter-sub-band scattering originated from 1D quantum confinement.

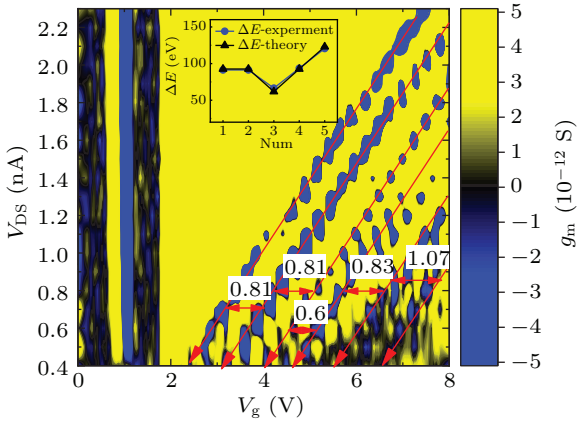


Fig. 4. The transconductance characteristics g_m for various V_g from 0 V to 8 V and V_{DS} from 0.4 V to 2.3 V at the temperature of 6 K. The inset shows the sub-bands intervals extracted from the transconductance experiment data and calculated from 1D transport theory.

Figure 5(a) shows the transconductance and corresponding current curves at the temperature of 6 K at $V_{DS} = 1.0$ V. Here we can clearly observe the two sets of fluctuations, with similar spacing as the 1D energy sub-band level intervals. The second set of fluctuations is exactly what we have demonstrated in Fig. 4 as the 1D transform and the positions shift with V_{DS} increasing. While the first set of transconductance fluctuations from the position around $V_{th} = 2$ V do not migrate with V_{DS}, shown from the enlarged g_m characteristics at the region around threshold voltage in the inset of Fig. 5(a).

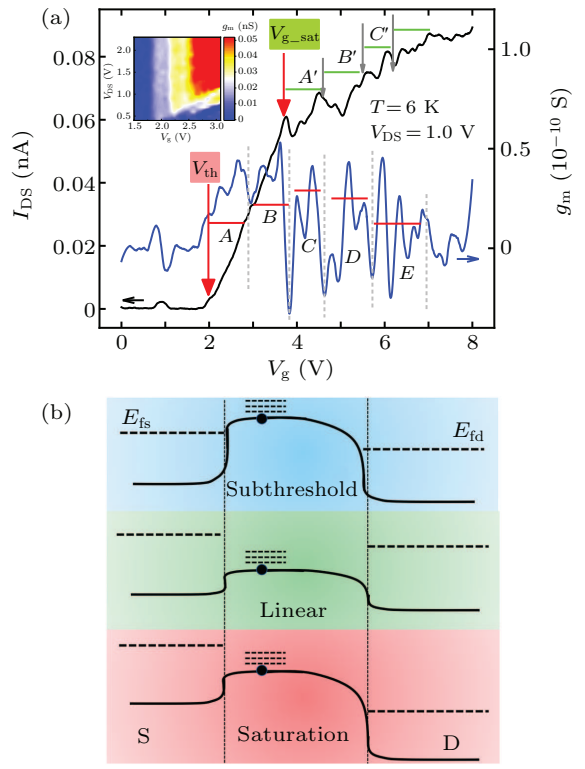


Fig. 5. (a) The current curves at the temperature of 6 K and corresponding transconductance at $V_{DS} = 1.0$ V. The inset shows the transconductance characteristics at the threshold region for various V_g and V_{DS} voltages at the temperature of 6 K. (b) Energy band diagram for the three operation regimes along the nanowire direction.

Here, the two sets of conductance fluctuations are related to the sub-band energy levels in the channel ($E_{channel}$) intersecting with the Fermi levels of the source (E_{fS}) and drain Fermi energy level (E_{fD}) in turn as V_g increases.[22] The first sub-band in the channel intersects the source Fermi level ($E_{fS} = E_{channel}$) at the position of V_{th} (the conduction band edge), resulting in the current starting to rise rapidly as the first transconductance peak appearing.[23–25] The energy level in the channel and the energy barrier between the source and the channel are strongly controlled by the gate voltage. The transverse electric field induced from V_{DS} can merely influence the intersection of E_{fS} and $E_{channel}$, therefore, do not influence the threshold voltage. As V_g increase above V_{th}, there come two kinds of situations — the liner region and the saturation region, depending on the relative position of $E_{channel}$ and the Femi energy level of the drain pool E_{fD}. Figure 5(b) shows the energy band diagram for the three operation regimes. Here we name "V_{g-sat}" as the position of gate voltage where $E_{channel} = E_{fD}$.

Keeping an unchanged value of V_{DS}, when V_g is high enough than V_{g-sat}, the first sub-level in the channel must go below both the drain and source Fermi levels, *i.e.*, $E_{fS} > E_{fD} > E_{channel}$, there comes the linear region. The channel is highly conductive and the current can be expressed as

$$I_{dlin} = \frac{\pi t_{si}\mu_{eff}C_g E_c}{(E_c L + V_D)} \cdot (V_{gs} - V_{th})^{\alpha/2} \cdot V_D \propto (V_{gs} - V_{th})^{\alpha/2}, \quad (3)$$

where E_c is the saturated electric field in the channel, L is the channel length, μ_{eff} is the effective mobility of the electrons in the channel, C_g is the effective gate capacitance of the device, t_{si} is the width of the nanowire, and the exponential fitting factor α is between 1 to 1.5.[26,27] As the V_g-related exponential factor "$\alpha/2$" is lower than 1 from Eq. (3), the currents in the linear region are less dependent on V_g than that on V_{DS}.

The saturation region comes when the increasing number of sub-levels reach the source–drain Fermi level window ($E_{fS} > E_{channel} > E_{fD}$). The gate voltage range for the saturation region is generally between V_{th} and V_{g-sat}. The saturation current can be expressed as

$$I_{dsat} = \beta \frac{\pi t_{si}\mu_{eff}C_g}{\left(1 + \frac{V_{dsat}}{E_c L}\right)(L - L_{sat})} \cdot (V_{gs} - V_{th})^{\alpha} \times V_{dsat} \propto (V_{gs} - V_{th})^{\alpha}, \quad (4)$$

where V_{d-sat} is the V_{DS} at the saturation point, L_{sat} is the effective channel length. As we mentioned above, the V_g-related exponential factor α is larger than 1, which means current at saturation region is highly dependent on V_g, which can also be observed in the current curve of Fig. 5(a) in the region of $V_{th} < V_g < V_{g-sat}$.

We can use the general formula: $y = a(x-b)^c$ for the currents in both linear and saturation regions according to Eqs. (3) and (4), where the parameter b indicates the threshold voltages

V_{th} which should be uniform in both regions, and the exponential fitting factor c in the saturation region is α, and supposed to be $\alpha/2$ in the linear region. Figure 6(a) shows the fitting results of the two transport regions at $V_{DS} = 1.0$ V. The inset of Fig. 6(a) shows the factors b corresponding to V_{th} from all the transfer characteristics under different V_{DS} from 0.4 V to 2.3 V, which remain quite stable at exactly the position near $V_{th} = 2$ V.

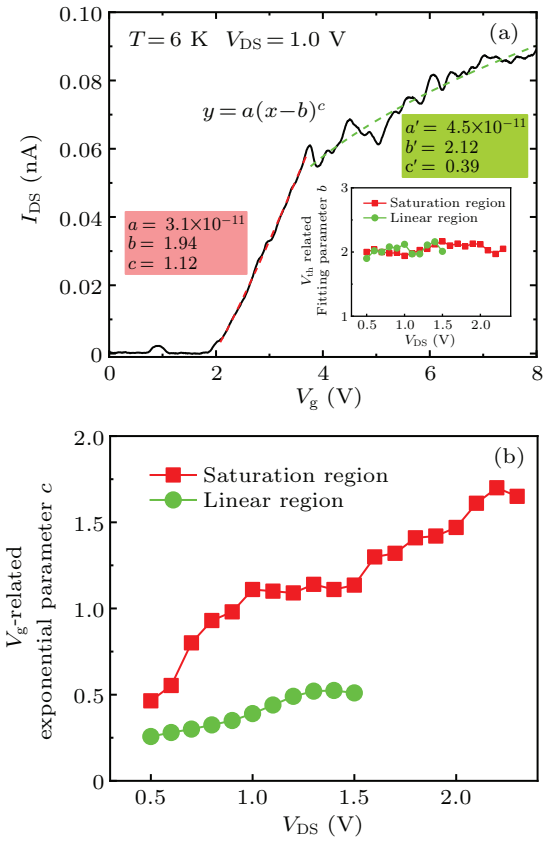


Fig. 6. (a) The fitting results of the saturated region and the linear region at the temperature of 6 K under $V_{DS} = 1.0$ V. The inset shows the fitting factors b, which is corresponding to V_{th} according to the theory. (b) The V_g-related exponential fitting factor c extracted by fitting results from the transfer characteristics of different V_{DS} voltages at the temperature of 6 K. This parameter c in the saturation region is supposed to be twice that in linear region.

Figure 6(b) shows the V_g related exponential coefficient c for both operation regions, which is twice in the saturation region than that in the linear region as our model. This indicates that in the saturation region, the relatively high transverse electric field makes the current highly limited by gate potential. While in the linear region, the Fermi energy level is under both source and drain Fermi levels, the conductive current in the channel is almost dependent on the energy gap between the drain and the source, which is less influenced by the gate voltage. Another characteristic we should notice from Fig. 6(b) is that the V_g-related exponential factor c in both regions increases with V_{DS}. The transverse electric field induced from V_{DS} is supposed to have the role of amplification the gate restriction effect of the channel.

Figure 7 shows the positions of V_{g-sat} shift linearly with V_{DS}, with the data extracted from the transfer curves under the V_{DS} from 0.4 V to 2.3 V. As discussed above, V_{g-sat} indicates the turning point from the saturation region to the linear region where the energy satisfies the equation $E_{fD} = E_{channel}$. The Fermi energy level of the drain region E_{fD} is mostly dependent on the V_{DS} voltage and will certainly go down with the V_{DS} voltage increase. Correspondingly, the turning point V_{g-sat} willshift to higher gate voltage to upraise the Femi energy level of the channel to rebalance the energy to $E_{fD} = E_{channel}$ with the V_{DS} increase. The inset of Fig. 7 shows the output curves for different gate voltages of V_g =2.5 V, 3.5 V, 4.5 V, 5.5 V, 6.5 V at the temperature of 6 K. The turning points of the output currents from the linear region to saturation region are marked as triangles in color, which are exactly consistent with the V_{g-sat} points from I_D–V_g curves (marked as arrows in color in Fig. 7).

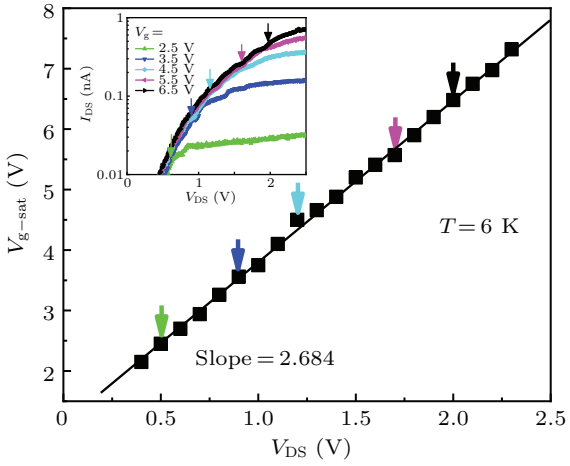


Fig. 7. The V_{g-sat} *versus* V_{DS} data points. V_{g-sat} is the turning point extracted from the transfer characteristics under different V_{DS} at the temperature of 6 K. The inset shows the output curves of the device at 6 K under different gate voltages of 2.5 V, 3.5 V, 4.5 V, 5.5 V, 6.5 V. The triangles point to the turning position from linear region to saturation region.

The transconductance curves at room temperature for different V_{DS} from 0.4 V to 2.3 V all exhibit two obvious peaks in Fig. 8(a), indicating the position of V_{th} and V_{g-sat} which have been discussed above. Besides, the positions of the first peaks (V_{th}) stay fixed for different V_{DS}, as the transverse electric field has less influence on the energy barrier between the source and channel to turn on the device. While the second peaks (V_{g-sat}) shift right with V_{DS} increase because the higher Femi energy level of the channel required to meet the situation of $E_{fD} = E_{channel}$ where the transport mode transform from linear mode to saturation mode. We should notice that the regularly transconductance fluctuations almost disappear in contrast to what we have observed before at the temperature of 6 K seen from Fig. 8(b). This is because the energy of the electrons at room temperature is high enough to overcome the 1D quantum energy sub-band intervals.

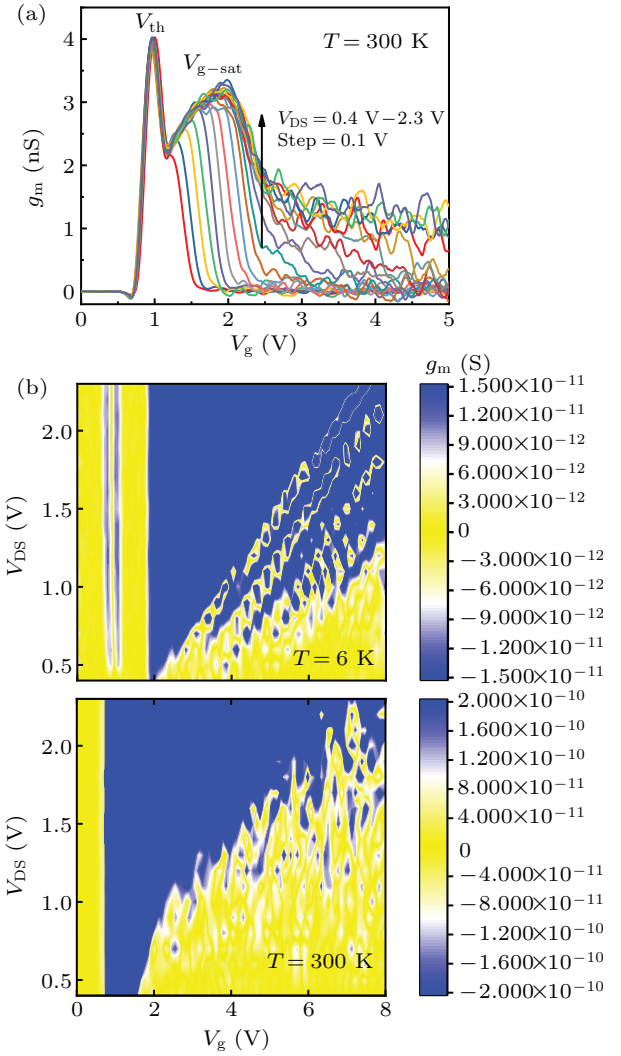


Fig. 8. (a) The transconductance curves of the device at room temperature under different V_{DS} voltages. (b) The combo chart of the 3D transconductance curves of the device at the temperature of 300 K and 6 K under different V_{DS} voltages.

4. Conclusion

In our work, we studied the influence of source and drain bias voltage on the quantum sub-band transport spectrum in our 10-nm width N-typed junctionless nanowire transistor at the low temperature of 6 K. We observed the single electron tunneling current peaks below the edge of the conducting band which shows the independence of V_{DS}. We demonstrated that the transverse electric field introduced from V_{DS} has less influence on the threshold voltage of the device. Above the conduction band edge, the transverse electric field is supposed to have the role of amplifying the gate restriction effect of the channel. The 1D sub-band dominated transport is demonstrated to be modulated by V_{DS} in different ways in the saturation region and the linear region. The turning point from the linear region to the saturation region (V_{g-sat}) shifts right with V_{DS} increase because the higher Femi energy level of the channel is required to satisfy $E_{fD} = E_{channel}$. We also find that the bias electric field has the effect to accelerate the thermally activated electrons in the channel, equivalent to thermal temperature on the increase of electrons energy. Our work provides a more comprehensive understanding of transport behaviors at nanoscale devices under the influence of changing source/drain bias voltages.

Acknowledgement

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