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Heterogeneous integration of InP HEMTs on quartz wafer using BCB bonding technology

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Heterogeneous integrated InP high electron mobility transistors (HEMTs) on quartz wafers are fabricated successfully by using a reverse-grown InP epitaxial structure and benzocyclobutene (BCB) bonding technology. The channel of the new device is $In_{0.7}Ga_{0.3}As$, and the gate length is 100 nm. A maximum extrinsic transconductance $g_{m,max}$ of 855.5 mS/mm and a maximum drain current of 536.5 mA/mm are obtained. The current gain cutoff frequency is as high as 262 GHz and the maximum oscillation frequency reaches 288 GHz. In addition, a small signal equivalent circuit model of heterogeneous integration of InP HEMTs on quartz wafer is built to characterize device performance.

Keywords: heterogeneous integration, InP high electron mobility transistor, quartz, small-signal model

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1. Introduction

InP-based high electron mobility transistors (HEMTs) are considered as one of the most competitive semiconductor devices for millimeter and terahertz monolithic integrated circuits. These applications are based on the excellent properties of the InP-based HEMTs, such as low noise, low power consumption and high gain performance.[1–6] However, owing to the high dielectric constant of InP, the transmission loss of InP-based monolithic integrated circuits is large, and the application of InP-based HEMTs in the high-frequency field is restricted. Therefore, it is necessary to replace the substrate of InP HEMTs through heterogeneous integration.

In recent years, many structures and methods have been used to achieve the heterogeneous integration of InP-based transistors on Si and other substrates in order to gain better performance and larger application fields. Liu *et al.*[7] have reported the heterogeneous integration of InP-based heterojunction bipolar transistor (HBT) structures on Si substrates by using molecular beam epitaxy, which have the similar direct current (DC) and radio frequency (RF) performance to the device grown on lattice-matched InP substrate. Hayashi *et al.*[8] have investigated the layer transfer of GaAs, InP, GaSb, and InAs by using hydrogen ion exfoliation and wafer bonding. Kim *et al.*[9] have presented the InGaAs-on-insulator fabrication from an InGaAs layer grown on a Si donor wafer with a III–V buffer layer instead of growth on an InP donor wafer, and such transistors exhibit the high electron mobility and uniform distribution of the leakage current.

Quartz has the features of low dielectric constant and insulation, so it is very suitable to serving as the substrate for high frequency circuits. The excellent RF characteristics of InP-based HEMTs and the low dielectric constant of quartz wafer can be combined on the same device by using heterogeneous integration. The heterogeneous integration of InP-based transistors on quartz wafer shows a promising future, and the design, fabrication and characteristics of heterogeneous integration of InP HEMTs on quartz wafer still need further studying.

In the present research, we describe the design, fabrication, and characteristics of the heterogeneous integration of $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ InP-based HEMTs on quartz wafer with 100-nm gate-length. The reverse-grown InP epitaxial structure is used to realize the layer transfer with the BCB bonding technology. The BCB bonding technology is chosen here in this work, for the BCB bonding is not sensitive to the surface morphology of the bonded wafer, the temperature during the bonding process is relatively low, and the BCB after bonding is robust again the attack from various strong acids, strong alkalis, and chemical solvents. A small signal equivalent circuit model is established to evaluate the mechanism of RF performance, and the excellent agreement between the measured and simulated f_T, f_{max}, and k is observed.

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2. Experiment

Figure 1(a) shows the epitaxial structure of the HEMT used in this work and figure 1(b) shows a schematic cross-sectional view of our heterogeneous integrated InP-based HEMT structure. All epitaxial layers were grown by molecular beam epitaxy (MBE) on a 3-inch (1 inch = 2.54 cm) semi-insulating (100) InP substrate.[10,11] From bottom to top, the epitaxial layers constituting a 50-nm InP buffer were a 100-nm $In_{0.53}Ga_{0.47}As$ etching stopper layer, a 10-nm InP etching stopper layer, a 40-nm Si-doped composite InGaAs cap layer, a 4-nm InP etching stopper layer, an 8-nm $In_{0.53}Al_{0.47}As$ Schottky barrier layer, Si delta doping layer with 5×10^{12} cm^2 doping concentration, a 3-nm $In_{0.52}Al_{0.48}As$ spacer layer, a 10-nm $In_{0.7}Ga_{0.3}As$ channel layer, and a 500-nm $In_{0.52}Al_{0.48}As$ buffer. A 10-nm Si-doped $In_{0.65}Ga_{0.35}As$ layer, a 15-nm Si-doped $In_{0.53}Ga_{0.47}As$, and a 15-nm Si-doped $In_{0.53}Al_{0.47}As$ transition layer constituted the composite cap layer to facilitate the formation of non-alloyed Ohmic contacts. After device fabrication we could obtain the heterogeneous integration of InP HEMTs on quartz wafer as shown in Fig. 1(b).

The device fabrication started with interconnections of InP epitaxy and quartz through BCB (3022-46, Dow Chemical) adhesive bonding and InP substrate removing as shown in Fig. 2. The epi-wafer and quartz were first treated in oxygen plasma, and then placed on a hot plate to remove surface moisture. After that, the wafers were coated with BCB, precured for 10 min and finally placed in an oven filled with N_2 at 0.18 MPa pressure for curing BCB.

Then the origin InP substrate and InP buffer were removed by using HCl:H_2O = 3:1, the InGaAs stopper layer was removed by using H_3PO_4:H_2O_2:H_2O = 3:1:50 and the InP etched stopper layer was removed by using HCI:H_3PO_4 = 1:4 to expose the InGaAs cap layer. After mesa-etching, Ohmic-contact formation, and T-shaped gate recess via e-beam lithography, the heterogeneous integration of InP HEMTs on a quartz wafer was fabricated.

Detailed fabrication processes of the HEMT devices are similar to those of our previously reported devices.[12] And the process of heterogeneous integration is compatible with the process of CPWG MMIC. The specific contact resistivity was determined by transmission line method (TLM) to be about 1.09×10^{-7} $\Omega\cdot cm^{-2}$.

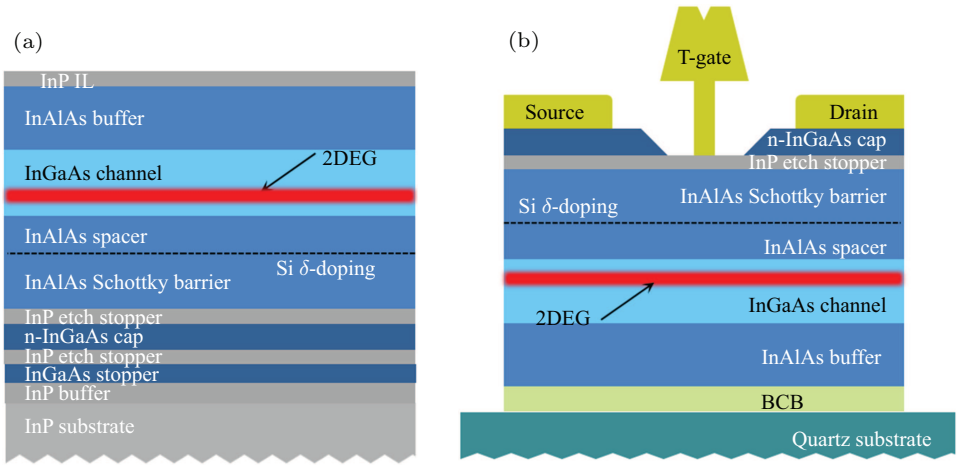


Fig. 1. (a) Schematic cross-sectional view of epitaxial structure and (b) heterogeneous integrated InP-based HEMTs.

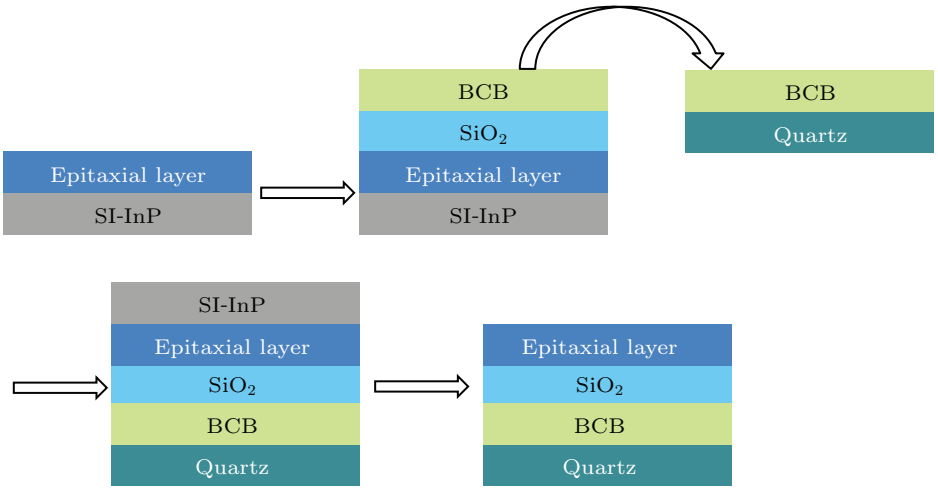


Fig. 2. Process of BCB adhesive bonding and InP substrate removing.

To characterize the device performance, DC performance was revealed through HP4142 semiconductor parameter analyzer at room temperature, and the RF performance was characterized via an Agilent E8363B PNA vector network analyzer from 0.1 GHz to 50 GHz at room temperature. After measurement the *S*-parameters were extracted and studied.

3. Results and discussion

3.1. DC characteristics

Figure 3(a) shows the current–voltage (*I*–*V*) characteristics of a 100-nm gate length HEMT with a gate width of 2×20 μm at room temperature. The gate–source voltage (V_{GS}) increases from −1.3 V to 0 V in steps of +0.1 V, and the drain–source voltage (V_{DS}) is scanned from 0 V to 0.8 V. The heterogeneous integration of InP HEMTs on quartz wafer has good pinch-off characteristics, and we obtain a maximum drain current of 536.5 mA/mm which is achieved at $V_{GS} = 0$ V and $V_{DS} = 0.8$ V. The extrinsic transconductance (g_m) and the drain current of the HEMT at a bias of $V_{DS} = 0.8$ V are shown in Fig. 3(b). In addition, figure 3(c) shows the dependence of g_m on the V_{GS} for different values of V_{DS}. The device shows a pinch-off voltage of about −0.9 V. A maximum extrinsic transconductance $g_{m,max}$ of 855.5 mS/mm is achieved at $V_{GS} = -0.6$ V and $V_{DS} = 0.8$ V. Figure 3(d) shows the curve of gate leakage current of the HEMTs *versus* V_{GS} for $V_{DS} = 0$ V in a range from −1.3 V to 0 V. The gate leakage current of the device is small enough for the LNA applications.

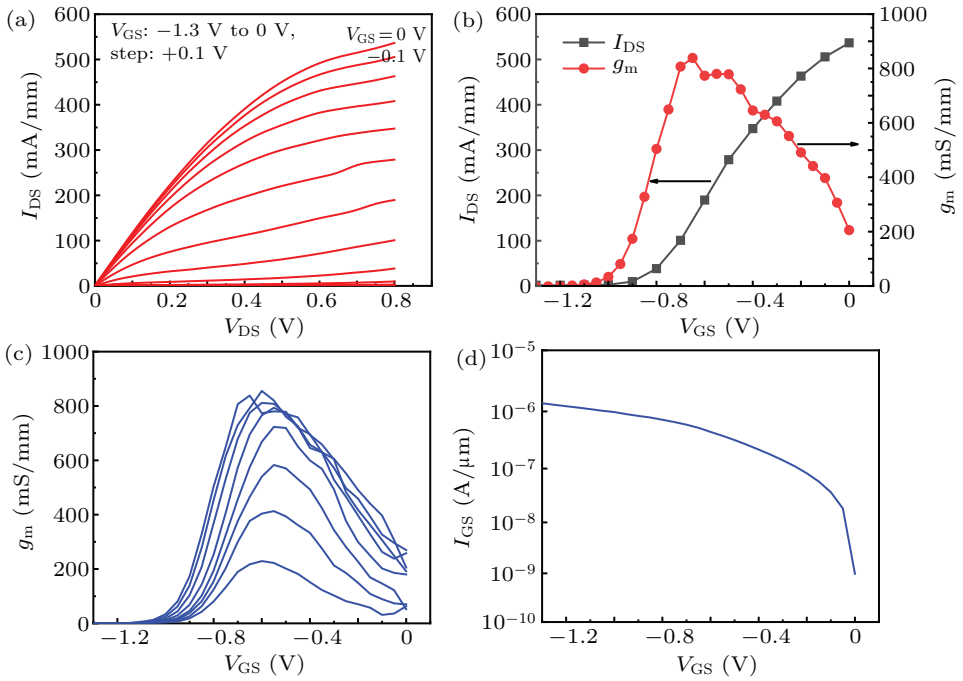


Fig. 3. DC performances of heterogeneous integration of InP HEMTs with L_g of 100 nm, shown by (a) I_{DS}–V_{DS} curve of InP-based HEMTs, (b) transfer curves of InP-based HEMTs measured at $V_{DS} = 0.8$ V, (c) dependence of transconductance on V_{GS} and V_{DS}, and (d) gate leakage current *versus* V_{GS} with $V_{DS} = 0$ V of HEMTs.

3.2. RF characteristics

The device under test is measured by using on-wafer open and short patterns to subtract pad capacitances and inductances from the measured device *S* parameters. Figure 4 shows the RF characteristics of heterogeneous integration of InP HEMTs with L_g of 100 nm, which is approximately biased at a peak g_m point of $V_{GS} = -0.6$ V and $V_{DS} = 0.8$ V. The current gain H_{21} and the maximum stable gain (MSG)/maximum available gain (MAG) of the HEMTs are determined by the measured *S*-parameter. Because of the limit of measuring frequency, we have to extrapolate the current gain (H_{21}) and the maximum available power gain (MAG) by using a least-squares fitting with a −20-dB/decade slope after the parasitic parameters have been de-embedded to acquire the f_T and f_{max}.[13] The value of f_T extrapolated from H_{21} is 262 GHz, and f_{max} extrapolated from MAG is 288 GHz. However, the device is still unstable ($k < 1$) at the maximum test frequency of 50 GHz, so it can be inferred that the actual f_{max} can be larger. The f_T and f_{max} are expressed as follows:

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)\left[1+G_{ds}\left(R_s+R_d\right)\right]+C_{gd}\cdot g_m\left(R_s+R_d\right)}, \tag{1}$$

$$f_{max} = \frac{f_{T,int}}{2\sqrt{G_{ds}\left(R_g+R_s\right)+\pi\cdot f_{T,int}\cdot C_{gd}\left(R_g+R_s\right)}}, \tag{2}$$

where C_{gs} is the parasitic capacitance from gate to source, C_{gd} is the parasitic capacitance from gate to drain, and R_g, R_d, and R_s are the parasitic resistances of gate, drain, and source, respectively. The g_m is the transconductance, the G_{ds} is conductance between the drain and the source, and $f_{T,int}$ is the value

of f_T for the core part of HEMTs without any parasitic resistances and capacitances. Equations (1) and (2) show that f_T and f_{max} have a positive correlation with g_m, and the f_T and f_{max} will be good because of the high g_m.

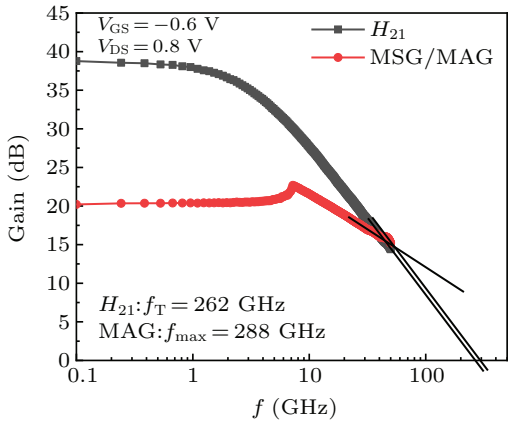


Fig. 4. RF characteristics of heterogeneous integration of InP HEMTs with L_g of 100 nm.

In order to characterize the properties and performance of device, a small signal equivalent circuit model of heterogeneous integration of InP HEMTs on quartz wafer is built. Figure 5 illustrates a small signal equivalent circuit model for the devices, biased at $V_{DS} = 0.8$ V and $V_{GS} = -0.6$ V. For the short gate length, the drain–source voltage will cause the source-side barrier to drop, resulting in the drain-induced barrier lowering effect (DIBL), which affects the channel current characteristics. Therefore, τ_{ds} is added into the model to characterize the influence of drain–source voltage on channel current.[14,15]

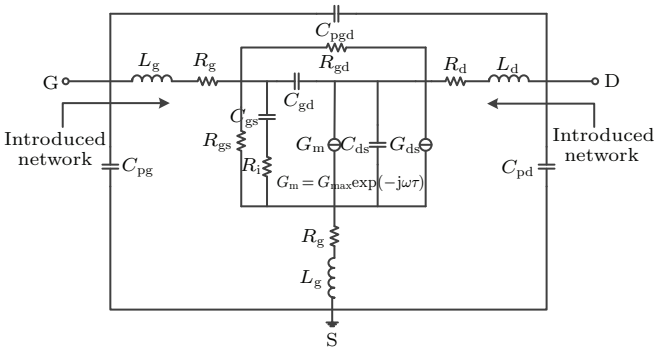


Fig. 5. Small signal equivalent circuit model of heterogeneous integration of InP HEMTs on quartz wafer.

The extrinsic parameters contain parasitic capacitances, parasitic inductances, and parasitic resistances. We calculate the parasitic capacitances and parasitic inductances through the S parameters of the open structure and the short structure. Then we extracte R_s by the YANG–LONG method and extracte R_g and R_d by the cold-FET method, and their expressions are as follows:

$$R_g = \mathrm{Re}\left(Z_{11} - Z_{12}\right), \tag{3}$$

$$R_d = \mathrm{Re}\left(Z_{22} - Z_{12}\right). \tag{4}$$

After all parasitic parameters are extracted, the intrinsic parameters are extracted. First, we obtain the S parameters of the intrinsic part of the device by using open-short de-embedding technology. Then according to the equivalent circuit structure of the intrinsic part, the intrinsic parameters are extracted through the Y parameters as shown below:

$$C_{gd} = -\frac{\mathrm{Im}\left(Y_{12}\right)}{\omega}, \tag{5}$$

$$C_{gs} = \frac{\left(1+D^2\right)}{\omega}\left(\mathrm{Im}\left(Y_{11}\right) + \mathrm{Im}\left(Y_{12}\right)\right), \tag{6}$$

$$R_i = \frac{D}{\left(1+D^2\right)\cdot\left(\mathrm{Im}\left(Y_{11}\right) + \mathrm{Im}\left(Y_{12}\right)\right)}, \tag{7}$$

$$g_m = \sqrt{\left(1+D^2\right)\cdot\left(\mathrm{Re}\left(Y_{21}\right)^2 + \left(\mathrm{Im}\left(Y_{21}\right) - \mathrm{Im}\left(Y_{12}\right)\right)^2\right)}, \tag{8}$$

$$\tau = -\frac{1}{\omega}\cdot\arctan\left(\frac{D\cdot\mathrm{Re}\left(Y_{21}\right) + \mathrm{Im}\left(Y_{21}\right) - \mathrm{Im}\left(Y_{12}\right)}{\mathrm{Re}\left(Y_{21}\right) - D\cdot\left(\mathrm{Im}\left(Y_{21}\right) - \mathrm{Im}\left(Y_{12}\right)\right)}\right), \tag{9}$$

$$g_{ds} = \mathrm{Re}\left(Y_{22}\right), \tag{10}$$

$$C_{ds} = \frac{\left(\mathrm{Im}\left(Y_{22}\right) + \mathrm{Im}\left(Y_{21}\right)\right)}{\omega}, \tag{11}$$

$$D = 1 + R_i^2\omega^2 C_{gs}^2. \tag{12}$$

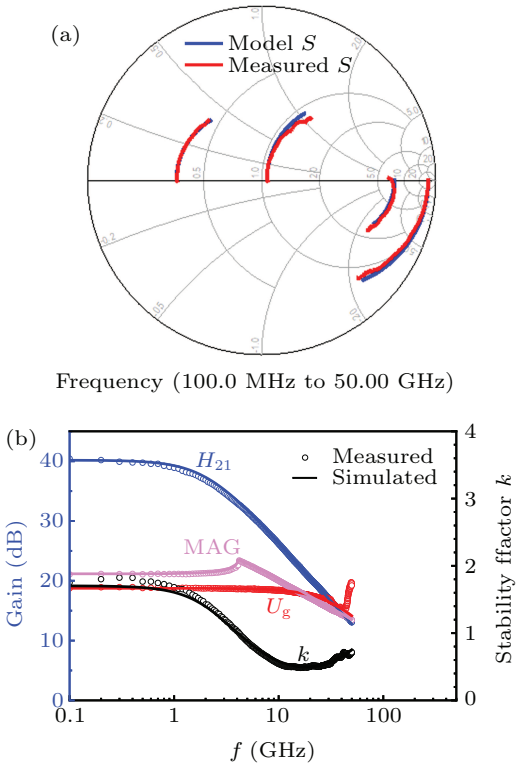


Fig. 6. Fitting result of (a) S parameters and (b) RF performances.

Finally, we obtain all the values of the parameters in our model. And then the small signal equivalent circuit model topology of heterogeneous integration of InP HEMTs on quartz wafer is built in the Agilent's advanced design system software (ADS), and the results are shown in Fig. 5. After that, the topology is simulated and all values of parasitic parameters and intrinsic parameters are tuned to fit the model

in ADS. The fitting result of S parameters for the model is demonstrated in Fig. 6. The parameters of small signal equivalent circuit of the device are given in Table 1. As we can see, the curved portion in the low frequency region of S parameters and high frequency region of S parameters can be fitted by the small signal equivalent circuit model, and the fitting results of H_{21}, MAG, and U_g and stability factor k are all excellent.

A summary of RF characteristics of InP-based HEMTs with the same gate lengths and channel but different substrates is given in Table 2. We can see that the value of f_T of this work is relatively high in Table 2 though our V_{DS} is smallest (just 0.8 V). If we increase the maximum V_{DS} of the device, the f_T will be higher and the RF performance of device will be better. The values of f_T and f_{max} of these devices are all outstanding, which means that the heterogeneous integrations of InP HEMTs on other substrates have a promising future because the heterogeneous integrated device can take the full advantages of various materials and structures.

Table 1. Parameters of small signal equivalent circuit of device biased at $f_{T,max}$.

Device	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_s (Ω)	R_d (Ω)	R_g (Ω)	R_{ds} (Ω)	R_{gs} (Ω)	R_{gd} (Ω)	R_i (Ω)	g_m (mS)	τ (s)	τ_{ds} (s)
This work	19.9	2.3	3.28	9.5	13.1	14.7	269	2697	15888	15.3	425	2×10^{-13}	2.3×10^{-13}

Table 2. Comparison aong published InP HEMTs on different substrates with gate length of 100 nm.

Reference	Year reported	Substrate/channel	L_g (nm)	f_T (GHz) (V_{DS} (V))	f_{max} (GHz) (V_{DS} (V))
[16]	2002	Si/$In_{0.53}Ga_{0.47}As$	120	185 (1)	280 (1)
[17]	2013	polyimide film/$In_{0.53}Ga_{0.47}As$	100	120 (1.2)	280 (1.2)
[18]	2017	GaAs/$In_{0.7}Ga_{0.3}As$	100	112.7 (1.5)	388.2 (1.5)
[19]	2021	InP/$In_{0.53}Ga_{0.47}As$	100	270 (1)	460 (1)
This work	2021	quartz/$In_{0.7}Ga_{0.3}As$	100	262 (0.8)	288 (0.8)

In Ref. [20], the aging of InP HEMT is influenced by a diffusion mechanism, the diffused impurities from gate electrode will reduce the carrier concentration in the epitaxial layer and cause device to age. Aging occurs in the gate area, so the change of the substrate has no effect on the aging caused by diffusion mechanism. As the thermal conductivity of quartz is much smaller than that of InP, the heat generated in the working process of the device will accumulate in the device and accelerate the aging of the device. In order to reduce this effect, MMIC structure with via holes and backside metal, such as CPWG, will be used to assist in heat dissipation.

4. Conclusions

In this work, the InP epitaxies grown in reverse order are used for heterogeneous integration with quartz wafers. The $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ HEMTs with 100-nm gate length and 2 μm×20 μm gate width on quartz substrates are successfully fabricated after BCB bonding. The HEMTs exhibit good DC and RF performances, each with a maximum drain current of 536.5 mA/mm, a maximum extrinsic transconductance $g_{m,max}$ of 855.5 mS/mm, a cut-off frequency of 262 GHz, and a maximum oscillation frequency of 288 GHz. In the end, the small signal equivalent circuit model is built to characterize the device performance; the fitting results of S parameters and the fitting results of RF performances are good. The excellent results of the heterogeneous integration of InP HEMTs show promising high frequency applications.

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References

[1] Kim D H and Alamo J A D 2010 *IEEE Electron Dev. Lett.* **31** 806
[2] Zhong Y H, Yang B, Chang M M, Ding P, Ma L H, Li M K, Duan Z Y, Yang J, Jin Z and Wei Z C 2020 *Chin. Phys. B* **29** 038502
[3] Kim D H, Brar B and Alamo J A D 2011 *Electron Devices Meeting*
[4] Sun S X, Wei Z C, Xia P H, Wang W B, Duan Z Y, Li Y X, Zhong Y H, Ding P and Jin Z 2018 *Chin. Phys. B* **27** 028502
[5] Sun S X, Chang M M, Li M K, Ma L H, Zhong Y H, Li Y X, Ding P, Jin Z and Wei Z C 2019 *Chin. Phys. B* **28** 078501
[6] Li J L, Cui S H, Xu J X, Cui X R, Guo C Y, Ma B, Ni H Q and Niu Z C 2018 *Chin. Phys. B* **27** 047101
[7] Liu W K, Lubyshev D, Fastenau J M, Wu Y, Bulsara M T, Fitzgerald E A, Urteaga M, Ha W, Bergman J, Brar B, Hoke W E, LaRoche J R, Herrick K J, Kazior T E, Clark D, Smith D, Thompson R F, Drazek C and Daval N 2009 *J. Cryst. Growth* **311** 1979
[8] Hayashi S, Goorsky M, Noori A and Bruno D 2006 *J. Electrochem. Soc.* **153** G1011
[9] Kim S, Ikku Y, Yokoyama M, Nakane R, Li J, Kao Y C, Takenaka M and Takagi S 2014 *Appl. Phys. Lett.* **105** 043504
[10] Zhou S X, Qi M, Ai L K, Xu A H, Wang L D, Ding P and Jin Z 2015 *Chin. Phys. Lett.* **32** 097101

[11] Huang J, Guo T Y, Zhang H Y, Xu J B, Fu X J, Yang H and Niu J B 2010 *Chin. Phys. Lett.* **27** 118502

[12] Wang L D, Ding P, Su Y B, Chen J, Zhang B C and Jin Z 2014 *Chin. Phys. B* **23** 038501

[13] Wang Q, Ding P, Su Y B, Ding W C, Muhammad A, Tang W and Jin Z 2016 *J. Semicond.* **37** 074003

[14] Zhong Y H, Li K K, Li M K, Wang W B, Sun S X, Li H L, Ding P and Jin Z 2018 *J. Infrared. Millim. Wave* **37** 163

[15] Zhong Y H, Wang W B, Yang J, Sun S X, Chang M M, Duan Z Y, Jin Z and Ding P 2020 *Solid State Electron.* **164** 107613

[16] Bollaert S, Wallaert X, Lepilliet S, Cappy A, Jalaguier E, Pocas S and Aspar B 2002 *IEEE Electron. Dev. Lett.* **23** 73

[17] Shi J, Wichmann N, Roelens Y and Bollaert S 2013 2012 *International Conference On Indium Phosphide And Related Materials* p. 233

[18] Sun B, Chang H, Wang S, Niu J and Liu H 2017 *Solid State Electron.* **138** 40

[19] Tong Z H, Ding P, Su Y B, Wang D H and Jin Z 2021 *Chin. Phys. B* **30** 018501

[20] Sasaki H, Yajima K, Yoshida N, Ishihara O and Mitsui S 1995 *7th International Conference on Indium Phosphide and Related Materials*, p. 745