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A 3D SiC MOSFET with poly-silicon/SiC heterojunction diode

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A three-dimensional (3D) silicon-carbide (SiC) trench metal–oxide–semiconductor field-effect transistor (MOSFET) with a heterojunction diode (HJD-TMOS) is proposed and studied in this work. The SiC MOSFET is characterized by an HJD which is partially embedded on one side of the gate. When the device is in the turn-on state, the body parasitic diode can be effectively controlled by the embedded HJD, the switching loss thus decreases for the device. Moreover, a highly-doped P^+ layer is encircled the gate oxide on the same side as the HJD and under the gate oxide, which is used to lighten the electric field concentration and improve the reliability of gate oxide layer. Physical mechanism for the HJD-TMOS is analyzed. Comparing with the conventional device with the same level of on-resistance, the breakdown voltage of the HJD-TMOS is improved by 23.4%, and the miller charge and the switching loss decrease by 43.2% and 48.6%, respectively.

Keywords: heterojunction diode, SiC MOSFET, switching loss, on-state resistance

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1. Introduction

Owing to its representative wide band-gap material and device performance, SiC metal–oxide–semiconductor field-effect transistor (MOSFET) is widely used in the power systems on account of the properties of low on-state resistance, high power density, outstanding switching characteristics, *etc*.[1–3] To obtain a high efficiency and a low power loss, it is important to increase the reliability of the SiC MOSFET and reduce the chip size. When the conventional SiC trench MOSFET (C-TMOS) is used in the power systems, a Schottky barrier diode (SBD) must be paralleled to prevent the aged deterioration,[4–7] which may result in high cost, extra power loss, and undesirable stray inductances. Several optimized structures such as the SiC trench MOSFET with a merged SBD have been studied, aiming at reducing the chip cost, enhancing the reverse recovery characteristics, and reducing the power loss,[8–12] *etc*. Additional fabrication and photolithography process are the main difficulties in commercializing these structures. The reliability of the gate oxide layer is also a major concern for the SiC MOSFET. Inserting a highly-doped P+ layer at the bottom of the trench gate oxide proves to be an effective method to improve the gate oxide reliability.

Heterojunction diode consisting of poly-silicon and SiC has a crucial influence on the reverse recovery time.[13,14] In this paper, a three-dimensional (3D) SiC MOSFET with an HJD embedded on one side of the gate oxide is presented and analyzed, which offers a new method to reduce the power loss and improve the electric characteristics for the SiC MOSFET.

2. Device structure and mechanism

Figures 1(a) and 1(b) show the device structures of the C-TMOS and the 3D HJD-TMOS, respectively. Compared with the conventional TMOS, the 3D HJD-TMOS has an HJD structure consisting of the poly-silicon/SiC, and the HJD is embedded in the z axis, which is an improvement based on the two-dimensional (2D) device.[15] Figure 1(c) shows the cross-section view and figure 1(d) shows the energy band diagram along the poly-silicon layer and the current spreading layer (CSL).

The valence band and conduction band for the HJD are 1.73 eV and 0.45 eV, respectively. The electron barrier height Φ_{BN} (about 1.48 eV) is determined by the Fermi-level E_f and the conduction band E_C. This barrier height can cause a small forward voltage (V_F) when the device is forwardly biased. On the contrary, it can cause a high breakdown voltage (BV) when the device is reversely biased. And the barrier height ΔE_C will control the parasitic diode in turn on state, creating a large on-voltage (V_{PN}). Furthermore, a highly-doped P+ layer is introduced into the structure encircling the gate oxide on the same side as the HJD and under the gate oxide to improve the gate oxide reliability.[16–18] It can lighten the electric field concentration around the regions near to the gate oxide and HJD, as well as reduce the overlapping between the gate layer region and the drift layer, realizing a high BV and a quick switching time.

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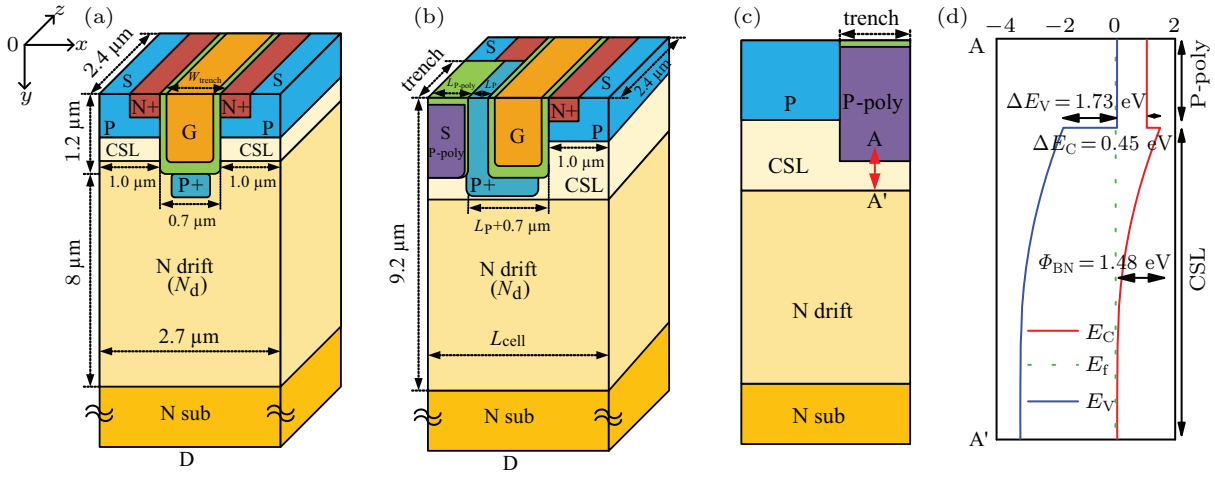


Fig. 1. Structure diagrams of (a) C-TMOS, (b) HJD-TMOS, (c) y–z cross-section view ($x = 0$), and (d) energy band among line AA′ for HJD-TMOS.

In this work, the P-poly and the P+ shielding layer extend along the whole z direction. In order to make a fair comparison, the two devices have the same major dimensions and doping concentrations. To get a BV above 650 V, the thickness and doping concentration for the channel layer are set to be 0.8 μm and 3×10^{17} cm^{-3}, respectively. The doping concentration of the drift layer (N_d) is 7.5×10^{15} cm^{-3}. The thickness of epitaxial layer from the N-substrate to the top surface of the device is 9.2 μm. The width (W_{trench}) and the depth for the trench gate are set to be 0.7 μm and 1.2 μm, respectively. The thickness of the gate oxide on the side and at the bottom are 60 nm and 120 nm, respectively. To simulate the device tape-out process, the traps are set with a doping concentration of 5×10^{12} eV^{-1}·cm^{-2}, which is located at the interface between SiO_2 and SiC. The CSL doping concentration is set to be 2×10^{16} cm^{-3}. The thickness of the CSL in HJD-TMOS set to be 0.8 μm, and in the C-TMOS has been optimized to obtain the same on-state resistance (R_{on}).

The Sentaurus TCAD tool is used to analyze the physical mechanisms for the SiC devices. The Shockley–Read–Hall (SRH), Auger, and Okuto–Crowell models are chosen in the recombination process. The mobility model contains incomplete ionization, high-field saturation, enormal, and doping-dependence.

3. Results and discussion

The key device parameters for the 3D HJD-TMOS are the width of the P-type poly-silicon (L_{P-poly}) and the distance between the poly-silicon trench and the gate trench (L_P). Figure 2 shows the influences of the L_{P-poly} and L_P on the electric field distributions and output performances for the HJD-TMOS.

As L_{P-poly} increases from 0.7 μm to 1.3 μm, the average electric field decreases slightly. While as L_P increases from 0.2 μm to 1.0 μm, the average electric field increases, which will significantly affect the breakdown voltage. Figure 2(b) shows that with a given L_P, the drain–source voltage V_{ds} increases with the L_{P-poly} rising when the I_{ds} reaches to 100 A/cm^2, which means that a smaller on-resistance can be obtained with a shorter L_{P-poly}.

Figure 3(a) shows the relation of the BV with L_P for three different values of L_{P-poly} for the HJD-TMOS. It is set that the device reaches to the breakdown point when the drain–source current I_{ds} rises to 10 μA/cm^2. The BV increases when L_P increases from 0.2 μm to 1.0 μm with the same L_{P-poly}. However, the BV decreases as L_{P-poly} increases from 0.7 μm to 1.3 μm with the same L_P. The relations of the R_{on} and the turn-on voltage of the body diode (V_{PN}), V_F with L_P and L_{P-poly} are shown in Fig. 3(b). When the cell pitch size increases as L_P and L_{P-poly} increase, the R_{on} increases as well. The V_F is almost a constant because it relates only to the HJD. The V_{PN} increases with the decrease of L_P or the increase of L_{P-poly}, and V_{PN} is 4.3 V with an L_{P-poly} of 0.7 μm and an L_P of 1.0 μm, which is still much larger than that of the conventional SiC pn junction (about 2.9 V). This indicates that the HJD-TMOS has a good control of the body diode in the turn-on state. Figure 3(c) shows the variation of R_{on} with the thickness of CSL in C-TMOS. With the increase of the thickness of CSL, the R_{on} changes in an opposite way. An L_P of 0.4 μm and an L_{P-poly} of 1.0 μm are chosen to analyze the device's performance for HJD-TMOS, and the R_{on} is about 1.89 mΩ·cm^2. In order to reach the same R_{on} level as the HJD-TMOS, the thickness of CSL in C-TMOS is set to be 0.36 μm, and an R_{on} of 1.88 mΩ·cm^2 is obtained just as shown in Fig. 3(c). The cell pitches of the two devices are 2.7 μm and 3.1 μm, respectively.

Figure 4(a) shows the I–V curves in the turn-off state for the two devices. The HJD-TMOS provides a higher BV. Figures 4(b) and 4(c) show the x–y cross-section electric field

distributions at $V_{ds} = 650$ V for the two devices. Owing to a wider L_P and a larger P+ shielding region, the peaks of the high electric fields in the corners of the gate oxide and P+ region are both smaller for the HJD-TMOS.

Figure 5 shows the electric field distributions in different cross-sections through the biggest electric field points for the two devices. It is obvious that in the x–z cross-section and x–y cross-section, the average electric fields are improved for the HJD-TMOS, which is the reason why the device has a larger BV.

Figure 6 shows the I–V performances for the two devices. Figure 6(a) displays the I–V relations in the turn-on state. The two devices have a similar on-state current except in the transition region because of the same level of R_{on}. From Fig. 6(b) it can be seen that HJD-TMOS has a much lower V_F than C-TMOS, resulting in prominent reduction of the dead-time loss. As shown in Fig. 6(c), the V_{PN} of the optimized HJD-TMOS increases to 4.6 V at $I_{dsH} = 10$ A/cm^2, while V_{PN} is 2.9 V for the C-TMOS, which means that it can better control the body diode in the turn-on state.

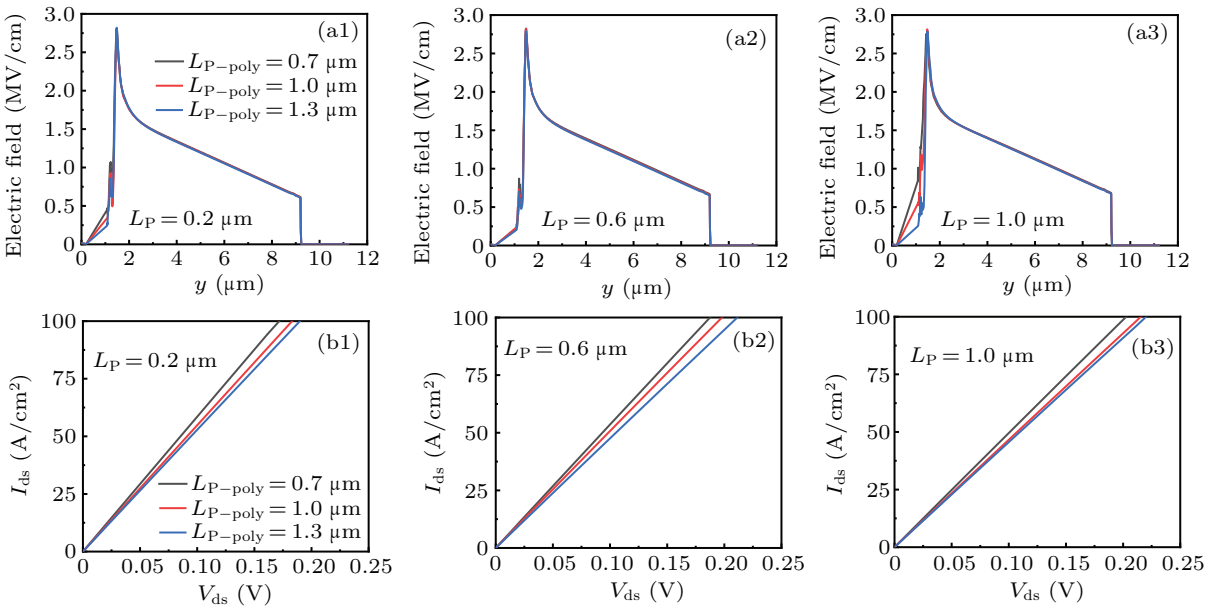


Fig. 2. (a1)–(a3) Vertical electric field distributions, (b1)–(b3) output I–V curves for some values of L_P and L_{P-poly}. Electric field distributions are chosen to be at their corresponding breakdown points.

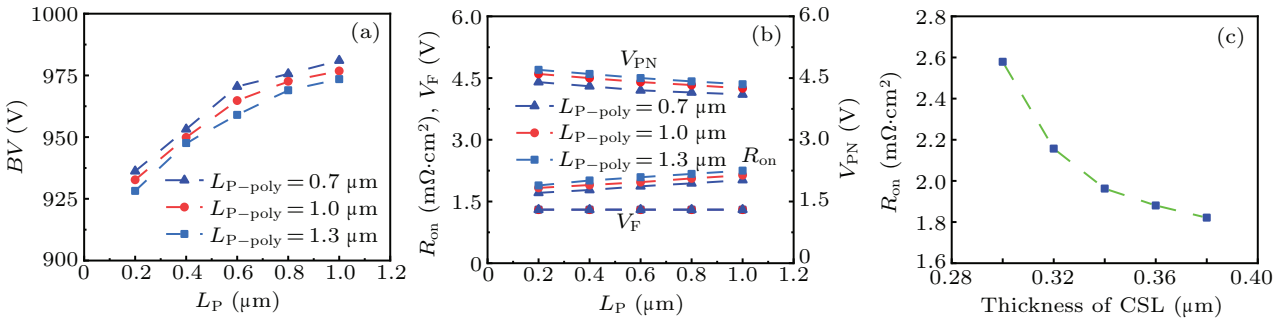


Fig. 3. (a) Curves of BV *versus* L_P for different values of L_{P-poly}; (b) curves of R_{on}, V_{PN}, and V_F for different values of L_{P-poly}; (c) curve of R_{on} *versus* thickness of CSL in C-TMOS.

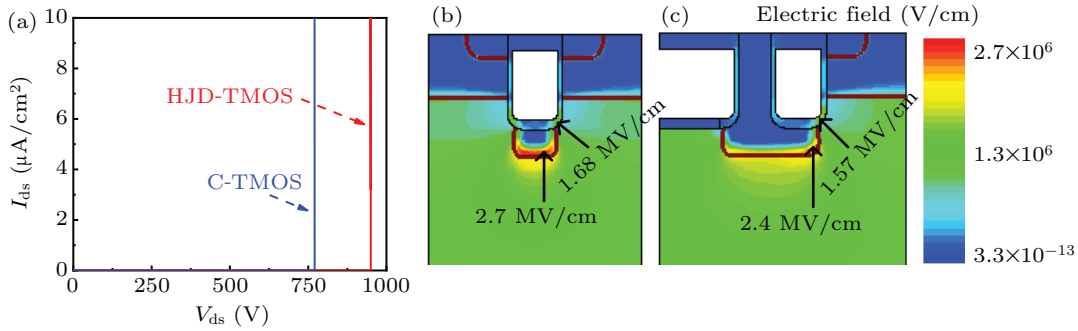


Fig. 4. Electric characteristics in the turn-off state for the two devices: (a) I–V curves, (b) x–y cross-section electric field in C-TMOS, (c) x–y cross-section electric field in HJD-TMOS, with electric field distributions chosen at $V_{ds} = 650$ V.

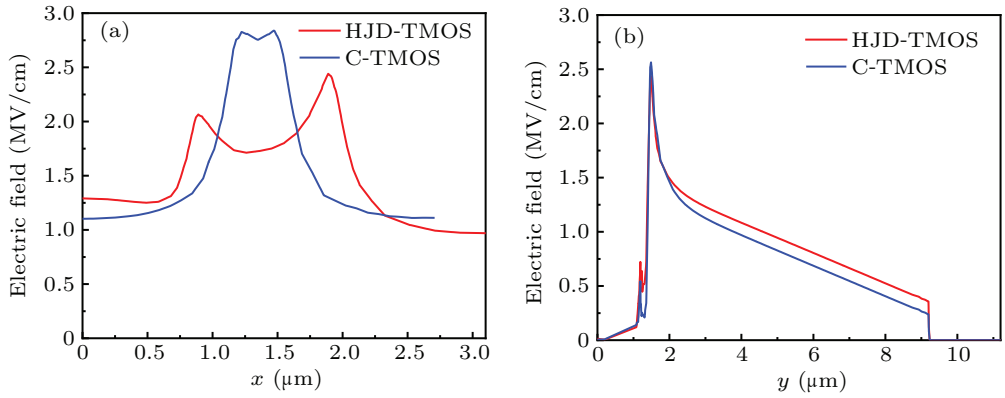


Fig. 5. Electric field distributions when breakdown occurs for two devices: (a) x–z cross-section electric field distributions, (b) x–y cross-section electric field distribution, with electric field distributions chosen at their corresponding breakdown points.

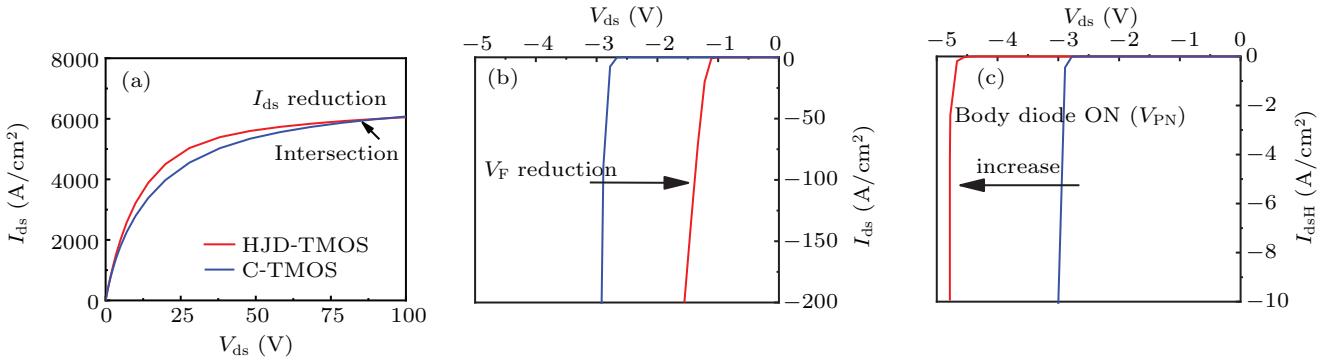


Fig. 6. Forward characteristics and reverse characteristics of two devices: (a) output curve (V_{gs} = 15 V), (b) V_F curves (V_{gs} = −5 V), and (c) V_{PN} curve (V_{gs} = −5 V).

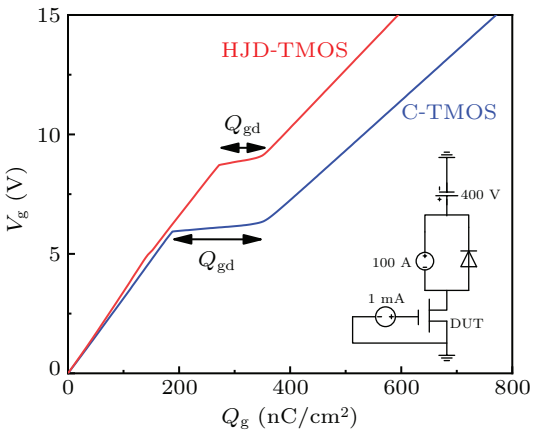


Fig. 7. Relations of gate voltage with gate charge for two devices, with insert showing test circuit.

Figure 7 shows the relations of the gate voltage (V_g) with gate charge (Q_g) for the two devices. Compared with the conventional device, the HJD-TMOS has a smaller miller plateau due to the smaller overlapping region between the gate layer region and the drift layer. The gate–drain charge (Q_{gd}) decreases down to 83 nC/cm^2, which is a 43.2% reduction from 150 nC/cm^2 of the C-TMOS. This indicates that the HJD-TMOS has a remarkable reduction of power loss.

Figures 8(a) and 8(b) show the switching waveforms and switching test circuit for the C-TMOS and the HJD-TMOS. Although the C-TMOS is anti-paralleled to the SiC SBD, the current spike of the HJD-TMOS is smaller in the turn-on state. Figure 8(c) shows the contrastive results of the switching loss for the two devices. The switching loss of the HJD-TMOS is reduced by 48.6% in comparison with the conventional one. The introduced HJD structure and the lower charge are the main factors that give rise to the lower switching loss and lead to the other excellent device performances at the same time as summarized in Table 1.

Table 1. Device parameters and characteristics.

Parameter	C-TMOS	HJD-TMOS
R_{on} (mΩ·cm^2)	1.88	1.89
BV (V)	770	950
Q_g (nC/cm^2)	770	598
Q_{gd} (nC/cm^2)	150	83
V_F (V)	2.9	1.2
FoM (MW/cm^2)	315.4	485
Switching loss (mJ/cm^2)	4.94	2.52

Figure 9 shows the variations of figure of merit (FoM) with length of HJD trench for different values of drift doping concentration (N_d) for the HJD-TMOS. The values of the mentioned C-TMOS and HJD-TMOS are both listed. It indicates that with N_d kept unchanged, the FoM increases as the trench length increases to 1.6 μm, at which the FoM is the largest. The FoM increases as the drift doping concentration decreases. When the drift doping concentration decreases

from 6×10^{15} cm^{-3} to 5.5×10^{15} cm^{-3}, the *FoM* increases slightly. The channel near the HJD plays a minor role in the whole structure when the trench length increases or the drift doping concentration decrease to a limited extent. And compared with the simulated C-TMOS, each of all partial HJD-TMOSs has its own better *FoM*.

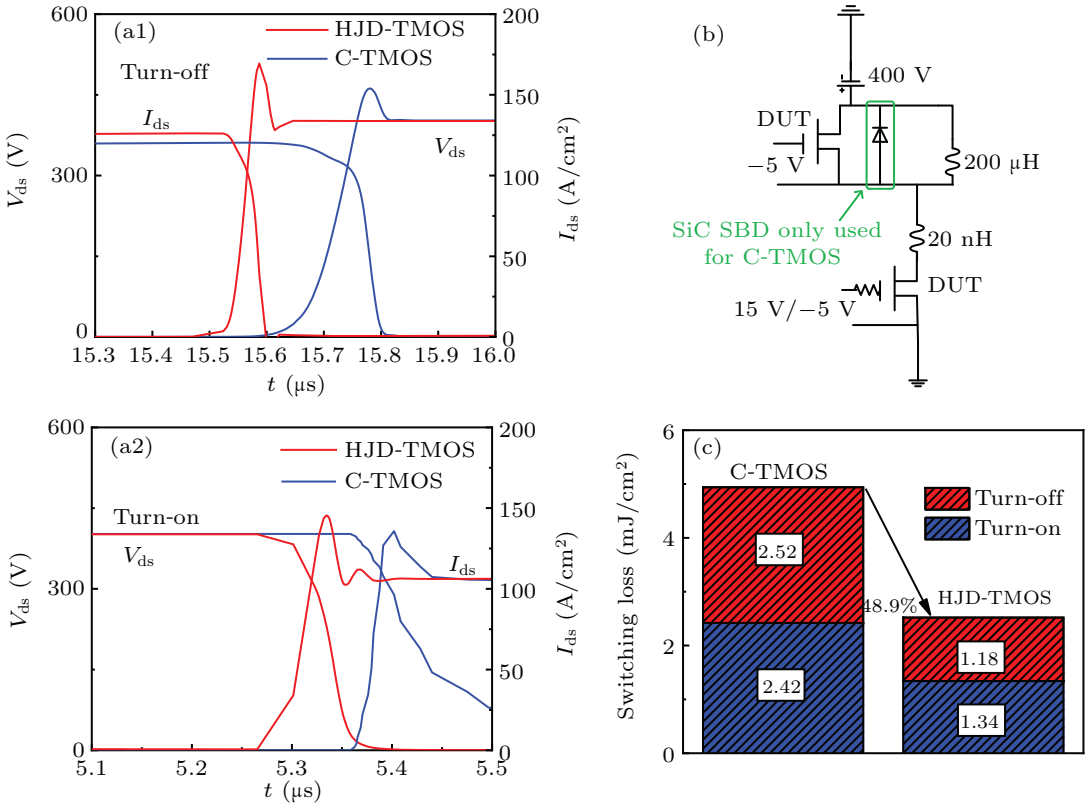


Fig. 8. (a1)–(a2) Switching waveforms of two devices, (b) test circuit, and (c) switching loss.

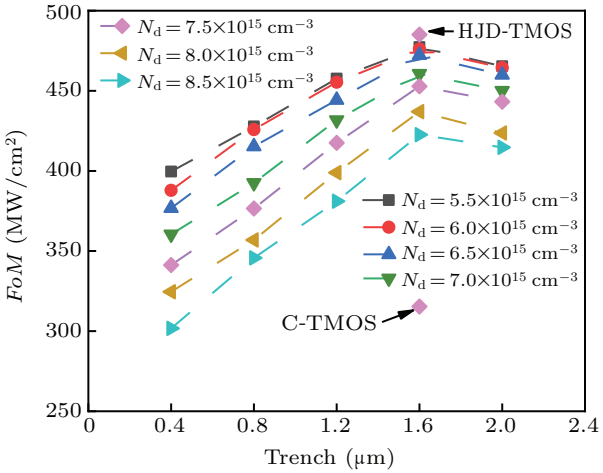


Fig. 9. Curves of *FoM versus* length of HJD trench at different values of N_d for HJD-TMOS, with L_P and L_{P-poly} being 0.4 μm and 1.0 μm, respectively.

4. Conclusions

A 3D SiC trench MOSFET embedded with an HJD structure is presented in this work. The embedding of HJD can suppress the parasitic body diode. The high-doped P+ shielding layer can reduce the strength of the electric field near the gate trench. The reverse recovery characteristic, the breakdown voltage and the switching property are all improved for the 3D SiC MOSFET, which has a great potential to be a great candidate in the power systems.

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