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Impact of O_2 post oxidation annealing on the reliability of SiC/SiO_2 MOS capacitors*

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The effects of dry O_2 post oxidation annealing (POA) at different temperatures on SiC/SiO_2 stacks are comparatively studied in this paper. The results show interface trap density (D_{it}) of SiC/SiO_2 stacks, leakage current density (J_g), and time-dependent dielectric breakdown (TDDB) characteristics of the oxide, are affected by POA temperature and are closely correlated. Specifically, D_{it}, J_g, and inverse median lifetime of TDDB have the same trend against POA temperature, which is instructive for SiC/SiO_2 interface quality improvement. Moreover, area dependence of TDDB characteristics for gate oxide on SiC shows different electrode areas lead to same slope of TDDB Weibull curves.

Keywords: SiC, O_2 post oxidation annealing, interface traps, MOS

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1. Introduction

Silicon carbide (SiC) is a promising material for power electronics because of its wide band gap and high thermal conductivity. Additionally, SiC is able to grow SiO_2 by thermal oxidation, a conventional way similar to silicon, which is one of the unique advantages of SiC over the other compound semiconductors.[1] At present, most of the world's leading semiconductor device manufacturers have made great progress in the production of SiC MOSFET devices. But for the oxidation treatment of SiC materials, too high or too low oxidation temperature leads to the existence of oxygen vacancy and residual carbon in gate oxide materials.

To reduce interface defects on SiC, although many progresses have been reported by using novel treatment methods, such plasma oxidation and ALD growth of high-k dielectrics,[2–6] thermal oxides with proper POA treatments, such as H_2, NO, N_2O, H_2O, N–O mixed plasma, H–Cl–N (10% HCl–N_2) mixed plasma, and so on, are still the main stream for dielectric growth on SiC because of their relatively high reliability.[7–14] Among the above various annealing ambient, O_2 is the most fundamental case to study carbon-related behaviors during POA treatment, because of no introduction of additional elements. Previously, it has been found that the gas flux, which is defined by the product of annealing time and pressure, is the main factor that affects the interface state for O_2 POA. In specific, an optimized process window at low pressure region ($\sim$ 0.1 bar, 1 bar = 10^5 Pa) is proposed to improve the interface quality of SiC MOS with applicable annealing duration (not too long or too short time span).[15] However, as another important factor except annealing time and pressure, the influence of temperature on the reliability of SiC/SiO_2 stacks needs further study. Furthermore, for O_2 POA, although there are several pioneering instructive works.[16–23] From the viewpoint of reliability, besides D_{it}, TDDB characteristics, gate-leakage density, breakdown field and their relationship still need to be further investigated.

In this work, we study the effect of dry O_2 annealing at different temperatures on the D_{it} of SiC/SiO_2 stacks, and further explore the effect of D_{it} of SiC/SiO_2 MOS stacks on the electrical properties of the oxide, such as J_g and TDDB characteristics. Moreover, the area dependence of TDDB characteristics for thermal gate oxide on SiC is studied.

2. Experiment

After standard RCA cleaning, SiO_2 was grown by dry O_2 oxidation of n-type 4H–SiC epitaxial layer at 1300 °C for 30 minutes followed by cooling down in N_2 gas with a rate of 10 °C/min. Note that before cooling down process, oxygen was pumped out from the chamber to less than 1 Pa within 10 seconds. Therefore, the as-oxidized sample can be regarded

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as the one without any POA treatments. The thickness was confirmed to be 50 nm by 1 MHz C–V measurement. The epitaxial layers were grown on (0001) Si face 4H–SiC substrate with a thickness of 12 μm, a 4°-off angle and an effective carrier density ($N_d - N_a$) of about 7.81×10^{15} cm^{-3}. POA treatments were carried out at 0.1-bar dry oxygen ambient for 5 minutes with a temperature range of 800 °C to 1000 °C, respectively. The details are listed in Table 1. After the thermal oxidation and POA treatments, 500-nm-thick aluminum top electrodes with areas of 0.68×10^{-2} mm^2, 1.83×10^{-2} mm^2, and 3.58×10^{-2} mm^2 (confirmed by optical microscope) were formed by thermal evaporation with metal mask. Then, after polishing the SiC substrate backside with a diamond-pen, aluminum with thickness of 500 nm was directly evaporated to achieve back ohmic contact. Keysight B1500A and E4990 LCR meters were used for I–V and C–V characterizations.

Table 1. Detailed POA conditions for SiC/SiO$_2$ stacks.

Group	Temperrature (°C)	Pressure (bar)	Time (min)
As-oxidized	As-oxidized		
Dry-800	800	0.1	5
Dry-900	900	0.1	5
Dry-1000	1000	0.1	5

3. Results and discussion

Figure 1 shows the typical time-zero dielectric breakdown (TZDB) breakdown behavior of as-oxidized SiO$_2$/SiC stacks (step = 0.1 MV·cm^{-1}·s^{-1}), which consists of soft breakdown and hard breakdown.[24] A large current jump corresponds to a hard breakdown event.[25] In general, gate J_g with a sudden jump exceeding 3 orders can be regarded as hard breakdown.[26] The soft breakdown part is the area where the J_g increases obviously without hard breakdown, and the electric field of gate oxide (E_{ox}) from 6 MV/cm to the intrinsic breakdown field (E_{int}) is the soft breakdown part.

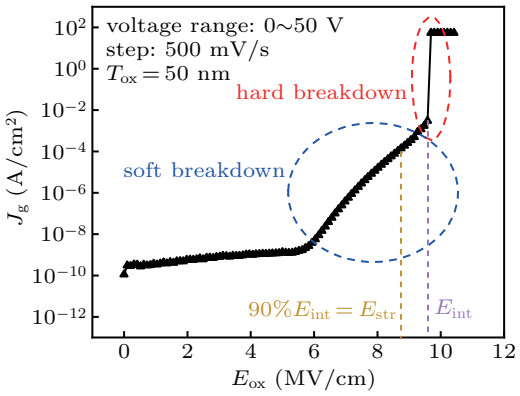


Fig. 1. Typical breakdown behavior of as-oxidized sample of thermal gate oxide on SiC. When J_g jumps suddenly, the value of the corresponding E_{ox} is the E_{int}. The E_{int} can guide us to determine the range of E_{str}, usually 90% of the E_{int} is taken as the E_{str}.

The gate oxide is tested by TDDB with constant stress electric field (E_{str}) which is determined by TZDB test. The statistics of gate oxide TDDB tests are usually described by the Weibull distribution[27]

$$F(x) = 1 - \exp(-(x/\alpha)^{\beta}), \tag{1}$$

where β is called the slope parameter. This Weibull slope β is an important parameter to determine the homogeneity level when evaluating gate–oxide reliability. β has a useful property such that if the area is increased by a factor (A_1/A_2), then the distribution is shifted by a factor of $\ln(A_1/A_2)$, and the characteristic lifetime α_1 would be decreased to α_2 according to the following expression:[28]

$$(\alpha_2/\alpha_1) = (A_1/A_2)^{1/\beta}. \tag{2}$$

Figure 2(a) shows time-to-breakdown (T_{bd}) distributions obtained from TDDB test of SiC MOS capacitors with three electrode areas. For each area, the plots can be divided into two regions: the initial failure region and the random failure region according to the bathtub curve analysis.[29] Figure 2(b) just shows the data related to random failure, where the data with failure rate of $F < 63.2\%$ are attributed to initial failure and therefore can be eliminated.

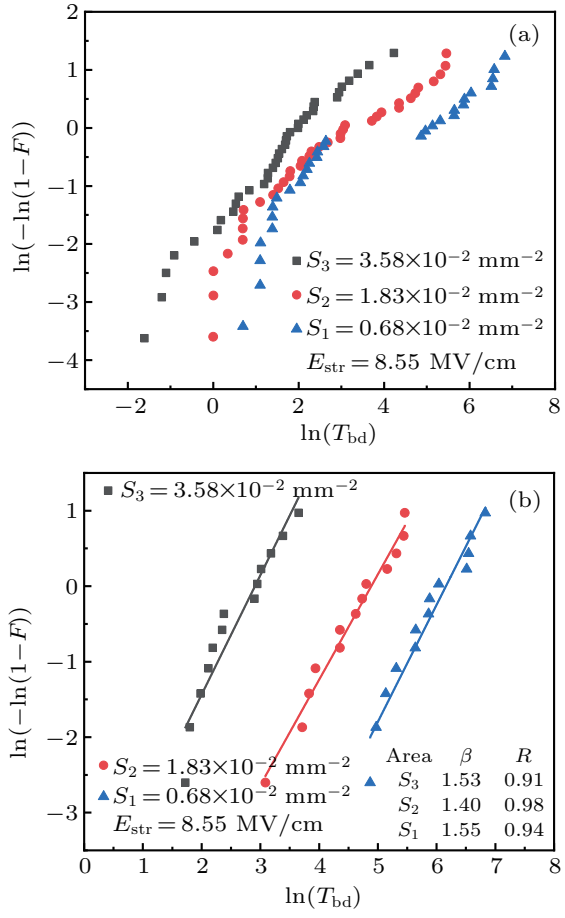


Fig. 2. TDDB Weibull distribution of as-oxidized sample of thermal gate oxide on SiC with fixing E_{str} = 8.55 MV/cm and varying electrode area. (a) Initial failure and random failure; (b) just random failure.

With the decrease of electrode area from 3.58×10^{-2} mm^2 to 0.68×10^{-2} mm^2, the corresponding Weibull slopes are 1.53, 1.40, and 1.55, respectively. Within the error range of 10%, the three Weibull curves are nearly parallel. The ratio between initial failure samples and total samples in T_{bd} are 24/37, 23/36, and 17/30 respectively, which are obtained according to the number of the same electrode area T_{bd} in Figs. 2(b) and 2(a). The larger the area of MOS capacitor gate, the larger the proportion of initial failure in T_{bd} distributions. Hatakeyama *et al.* suggested that the surface defects are one of the major causes of initial failure.[30] With the change of the electrode area, the Weibull slope β does not change, but the characteristic lifetime α changes. In specific, the smaller the electrode area, the larger the characteristic lifetime α.

Figures 3(a)–3(d) are J_g–E_{ox} diagrams of as-oxidized, dry-800, dry-900, and dry-1000 samples respectively. For each figure, the data are plotted from 5 samples with the same condition. Obviously, from initial to soft breakdown, five curves are nearly overlapped, suggesting the good uniformity of the sample, making it possible for the following comparison on J_g and E_{int}. As depicted in Figs. 3(a)–3(d), the E_{int} from small to large is dry-800, as-oxidized, dry-1000 and dry-900.

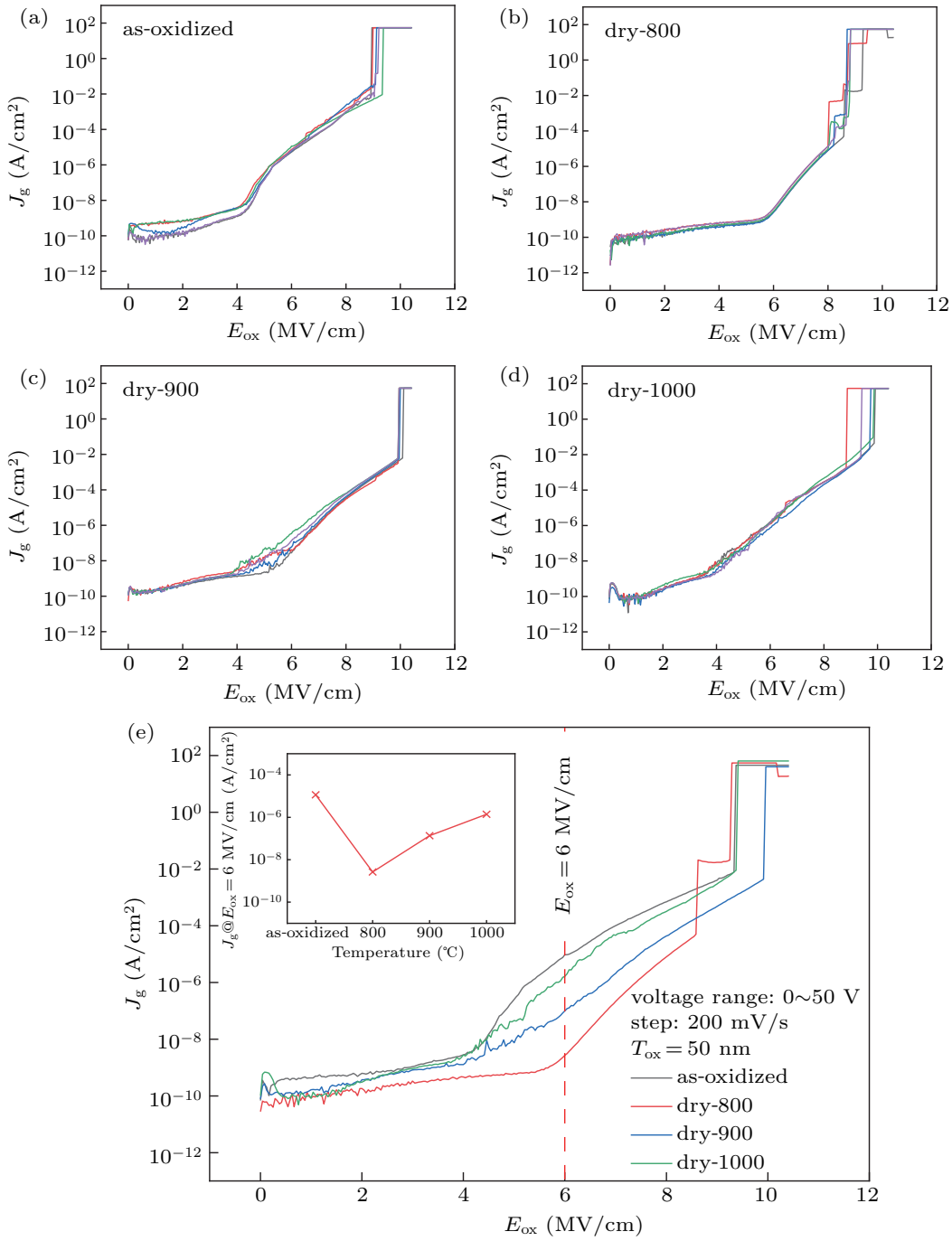


Fig. 3. (a)–(d) J_g–E_{ox} curves of TZDB of MOS capacitor of samples as-oxidized and samples re-oxidized at different temperatures. (e) Direct comparison of the typical TZDB curves of the four groups of samples: as-oxidized, dry-800, dry-900, dry-1000. The inset shows the comparison of leakage current density in soft breakdown region of the four groups of samples.

Figure 3(e) shows the soft breakdown region J_g of four groups of samples at E_{ox} of 6 MV/cm. The inset shows that the J_g meets the following trend, J_g (dry-800) $<$ J_g (dry-900) $<$ J_g (dry-1000) $<$ J_g (as-oxidized). Compared with the J_g from as-oxidized sample, the ones annealed at 800 °C, 900 °C, and 1000 °C show relatively lower J_g, indicating that POA treatment is beneficial for enhancing the dielectric quality and suppressing the gate leakage. When elevating the POA temperature from 800 °C to 1000 °C, J_g is found to increase, suggesting that the quality is sensitive to POA temperature.

For Fig. 3(b), it is noted that a common phenomenon with "step-like" current jump near the hard breakdown field exists when compared with those in Figs. 3(a), 3(c), and 3(d), suggesting that a bilayer continuous breakdown might occur for 800-°C POA sample. In order to further investigate the effect during POA at 800 °C, it is necessary to study the interface characteristic by considering D_{it}. This will be discussed in next section.

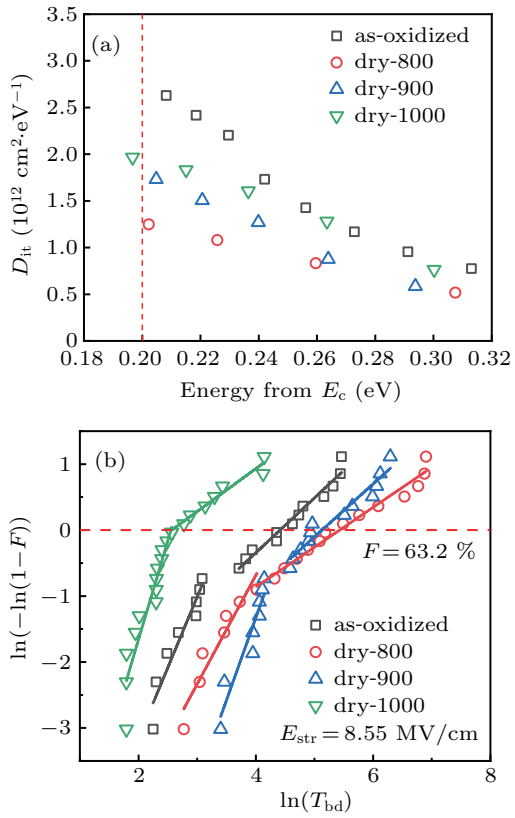


Fig. 4. (a) D_{it} of SiC MOS capacitors at different POA temperatures with 0.1-bar pressure for 5 minutes as a function of the surface potential. (b) TDDB Weibull distributions (only random failure) of thermal gate oxide on SiC at different POA temperatures with a fixed electrode area.

Figure 4(a) shows the D_{it} profiles extracted by conductance method from SiC/SiO_2 MOS capacitors with different POA conditions. As shown in Fig. 4(a), at the energy level of 0.2 eV below the conduction band edge of SiC, D_{it} (dry-800) $<$ D_{it} (dry-900) $<$ D_{it} (dry-1000) $<$ D_{it} (As-oxidized). Compared with the D_{it} from as-oxidized sample, the ones annealed at 800 °C, 900 °C, and 1000 °C show relatively lower D_{it}, indicating that POA treatment is beneficial for eliminating interface states in the temperature range of 800 °C to 1000 °C. However, with the increase of POA temperature, the reduction of D_{it} is decreasing. The above-mentioned trade-off behavior seems to be related to the phenomenon in Fig. 3(e).

Figure 4(b) shows the TDDB Weibull distribution of thermal gate oxide on SiC at different POA temperatures with a fixed electrode area of 1.83×10^{-2} mm^2. TDDB is limited only by the quality of the oxide and the interface, and not by the intrinsic properties of the SiC.[31] So the two different Weibull slopes β which are extracted by linear fitting the two regions in Fig. 4(b) represent the breakdown characteristics of the transition layer and SiO_2 layer respectively. Concerning the reason for the two slopes, it can be explained by considering the distribution of residual carbon across the interfacial transition layer and the SiO_2 film. Compared with SiO_2, the interfacial SiO_xC_y transition layer is a carbon-rich one, therefore the breakdown field of the interfacial transition layer should be lower, because residual carbon is the major origin of interface traps.[32,33]

Moreover, from the aspect of POA temperature dependence, as shown in Fig. 4(b), the sample annealed at 800 °C shows the longest T_{bd} when compared with the as-oxidized one and the ones annealed at higher temperature. According to Figs. 3(e), 4(a), and 4(b), similar trade-off distributions against POA temperature are demonstrated, suggesting that J_g, D_{it}, and T_{bd} are strongly correlated. Therefore, starting from the consistency in Figs. 3(e), 4(a), and 4(b), the data are summarized and re-plotted in Fig. 5(a) for comparison. Figure 5(a) shows the J_g, the inverse median lifetime of TDDB ($1000/\tau$) and the D_{it} values at $E_c - 0.2$ eV with different POA conditions. Note the median lifetime τ of TDDB is obtained from Fig. 4(b) at $F = 63.2\%$, and the inverse value of τ is used here for direct comparison because all the three parameters are required to be low for gate stack quality improvement. Compared with the other three conditions, the POA treatment at 800 °C is obviously the lowest in the above three key indicators. In order to explain the three trade-offs in Fig. 5(a), a plausible model is proposed in Fig. 5(b) by considering two competing reactions and a critical temperature T_c as follows.

For the two competing reactions, one is related to the reaction with interstitial carbon atom and oxygen vacancy, and the other one is related to the reaction with C–Si bond, both of them are oxidation reactions, this is consistent with the previous research by Zhu *et al.* and Kita *et al.*[22,34]

On the one hand, the increase of POA temperature is beneficial to removing the residual carbon in the transition layer and reducing the density of interface states. During POA treatment, as reported by Wang group,[22,23] carbon releases from SiO_xC_y in the form of CO or CO_2 and the SiO_xC_y transformation into higher oxidation states, thus reducing the SiO_xC_y

content and the interface transition region thickness. On the other hand, it enhances the reaction between oxygen atoms and SiC, and increases the density of interface states. This is consistent with the model proposed by Song et al. and the experimental results by Goto *et al.*[35,36] SiC/SiO_2 becomes less stable at high temperature, and tends to form oxygen vacancies and residual carbon.[37]

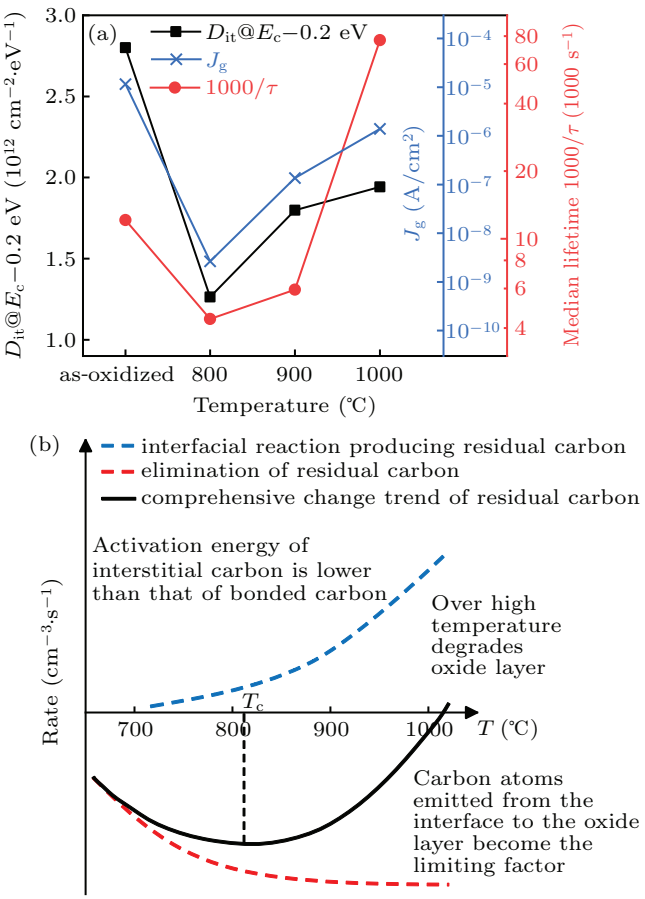


Fig. 5. (a) The J_g, the inverse median lifetime of TDDB (1000/τ), and the D_{it} values at 0.2 eV energy level below the edge of SiC conduction band for sample as-oxidized, dry-800, dry-900, and dry-1000. (b) Two competing reactions: generation of residual carbon and elimination of residual carbon.

Two competing effects occur simultaneously during annealing, the removal of carbon from the interfacial region and the oxidation of SiC to produce more carbon clusters.[38] According to the SiC oxidation model by Goto and Hijikata, carbon and silicon atoms are emitted from the interface into the oxide layer during thermal oxidation.[39] And the emitted carbon atoms become interstitial carbon in SiO_2. Since the interaction between interstitial carbon and surrounding SiO_2 network is much weaker than the strong covalent C–Si bond, the activation energy of interstitial carbon reaction with oxygen is lower than that of bonded carbon reaction with oxygen. Note that 800 °C is sufficiently low temperature to neglect the additional growth of oxide, which does not contribute to the interface deterioration by the low-temperature oxidation.[34]

For MOS capacitor, the D_{it}, J_g, and $1/\tau$, are all related to the amount of defects in the oxide and at the interface. In this work, we can roughly use the difference of reaction rate between the above mentioned two reactions to evaluate the amount of defects in SiO_2 and SiO_2/SiC interfaces. For both reactions, the reaction rate (R) can be approximately written in the following expression, $R = F \times \exp(-E_a/k_BT)$, where F is a pre-factor that depends on the reactant concentration, E_a is the reaction activation energy, T is the temperature, and k_B is the Boltzmann constant. For the reaction that repairs the SiO_2 network and SiO_2/SiC interface, F is mainly determined by the interstitial carbon and oxygen vacancy concentration. While for the latter one, it is related to the atomic density of SiC. Compared with the former one, since both interstitial carbon and oxygen vacancy are defects in the thermal oxide, the atomic density of SiC should be significantly larger. In order to make the discussion clearer and easier, we assume that in a short period of time, F of each reaction is a fixed value. And for comparison of activation energies, as mentioned above, E_a of reaction corresponding to network repairment should be much lower than the one corresponding to oxide growth at the interface during POA. Since the temperature is involved as $\exp(-E_a/k_BT)$ in the rate expression, as the POA temperature increases, rate grows faster for the reaction corresponding to higher E_a. Therefore, as the POA temperature increases, the rate difference between network repairment and oxide growth becomes smaller, and thus results in less improvement of gate stack quality including D_{it}, J_g, and $1/\tau$ in higher POA temperature region. In this work, although only 800 °C–1000 °C has been investigated, we infer that such trend can be slightly extended to higher temperature ($\sim$ 1100 °C or more), because the reaction mechanism does not change. While for the case of POA at $<$ 800 °C, although the oxide growth that degrades the interface nearly stops, the POA effect on gate stack improvement also becomes quite limited in short time span such as 5 min in this study, which is consistent with the results by Yin *et al.* and Kita *et al.*[33,34]

Therefore, by considering the above-mentioned tradeoffs, we believe a critical temperature T_c should exist. For the POA temperature lower than T_c, the removal rate of residual carbon increases with the increase of temperature, while for the POA temperature higher than T_c, it decreases with the increase of temperature, even with a net increase of residual carbon.

In the POA treatment, some residual carbon can be eliminated by oxidizing and repairing the interface, which helps to reduce the D_{it}. And when the temperature is higher than T_c, the rate of residual carbon produced by oxidation increases more with the increase of temperature. At this time, the net elimination rate of carbon residue decreases, leading to the decrease of improvement effect, and finally leading to degradation of D_{it}, reliability and gate leakage. This trend further confirms the inference about the existence of T_c.

Concerning the step-like jump in TZDB tests of 800-°C POA samples, since 800 °C is close to T_c based on our model, thus it is reasonable to believe that the uniformity and breakdown electric field of the interfacial layer at this condition is relatively higher, which makes the TZDB curves different from the other three ones, and causes the segmental breakdown of the two layers.

4. Conclusion

The effect of the O_2 POA temperature on the gate oxide quality is studied, in terms of gate leakage current density, interface trap density, and TDDB reliability, where trade-off distributions with the same optimized temperature ($\sim$ 800 °C) have been demonstrated. A plausible model is proposed by considering two competing reactions, *e.g.*, the removal of carbon from the interfacial region and the oxidation of SiC to produce more residual carbon, and a critical temperature T_c, which can well explain all the results in this work and strongly indicating that O_2 POA treatment near T_c is effective in improving the oxide quality on SiC for high performance and reliability devices.

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