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Device topological thermal management of β-Ga_2O_3 Schottky barrier diodes*

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The ultra-wide bandgap semiconductor β gallium oxide (β-Ga_2O_3) gives promise to low conduction loss and high power for electronic devices. However, due to the natural poor thermal conductivity of β-Ga_2O_3, their power devices suffer from serious self-heating effect. To overcome this problem, we emphasize on the effect of device structure on peak temperature in β-Ga_2O_3 Schottky barrier diodes (SBDs) using TCAD simulation and experiment. The SBD topologies including crystal orientation of β-Ga_2O_3, work function of Schottky metal, anode area, and thickness, were simulated in TCAD, showing that the thickness of β-Ga_2O_3 plays a key role in reducing the peak temperature of diodes. Hence, we fabricated β-Ga_2O_3 SBDs with three different thickness epitaxial layers and five different thickness substrates. The surface temperature of the diodes was measured using an infrared thermal imaging camera. The experimental results are consistent with the simulation results. Thus, our results provide a new thermal management strategy for high power β-Ga_2O_3 diode.

Keywords: β-Ga_2O_3 Schottky barrier diode, thermal management, TCAD simulation, infrared thermal imaging camera

PACS: 73.40.Mr, 84.30.Jc, 85.30.De, 85.30.Kk **DOI:** 10.1088/1674-1056/abeee2

1. Introduction

Ultra-wide bandgap (UWBG) β-gallium oxide (β-Ga_2O_3) has attracted numerous attention because of its higher Baliga's figure of merit and lower cost of large-sized substrates in comparison to other wide bandgap semiconductors like 4H-SiC and GaN.[1–5] All these properties enable β-Ga_2O_3 to be preferable for various power future electronic applications such as energy-saving electronic systems and efficient semiconductor switches, in which the thermal property plays a critical role for their operation.[6–8] At room temperature, the highest thermal conductivity of β-Ga_2O_3 is 27 W/m·K along the (010) crystalline direction, which is still one order of magnitude lower than that of 4H-SiC and GaN.[9–13] The self-heating effect (SHE) seriously affects the reliability and stability of the devices, such as the reduction of electron mobility and saturation velocity, owing to the rise of the device temperature.[14,15] Thus the poor thermal conductivity of β-Ga_2O_3 limits its application in the field of high temperature and high voltage.[16,17]

To overcome the poor thermal property of β-Ga_2O_3, a series of methods have been proposed including heterogeneous integration,[18–22] embedded cooling micro-channels,[23] top-side air-jet impingement,[24] and so on.[25,26] Impressively, ion cutting technology was applied to transfer 2-inch β-Ga_2O_3 film to SiC substrate with better heat dissipation,[27–29] but this method probably degraded the quality of the thin film. Researchers also found that about 30% of the total heat was generated near the interface of anode/β-Ga_2O_3 due to the resistive nature of the Schottky contact.[30] It was the concentrated heat dissipation and low thermal conductivity of β-Ga_2O_3 that resulted in a large temperature gradient near the Schottky contact. Thus, previous works indicate that the structure parameters of power devices play significant roles in thermal management. Although β-Ga_2O_3 SBDs are approaching commercialization, there is still no comprehensive simulation or experimental study on their heat dissipation.

In this work, the impact of device structure on peak temperature of β-Ga_2O_3 SBDs has been studied by both TCAD simulation and experiment. We simulate the internal temperature distribution with the crystal orientation, work function, anode area, and thickness, suggesting that the thickness of β-Ga_2O_3 plays a key role in reducing the peak temperature of the diode. Hence, β-Ga_2O_3 diodes based on various thickness epitaxial and substrates were fabricated, and the surface temperatures of the diodes were tested using an infrared thermal imaging camera. The experimental results show that it is an effective method to reduce the peak temperature of the device by thinning the thickness of the drift layer.

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2. Simulations

The device simulations were carried out using a commercial Silvaco TCAD software and a 2D device non-isothermal device model, so that they were more close to the real fact. Material parameters of β-Ga_2O_3 were mostly adopted from Ref. [31]. The constant thermal conductivity and low-field mobility model were assumed. Moreover, the LAT.TEMP parameter was added to the model, in order to consider heat flow in the device. The temperature-dependent lattice temperature coefficient of electron mobility is set as $\tau = 2.0$ as in the equation

$$\mu_{n0} = \mu_0 \times (T_L/300)^{\tau}, \quad (1)$$

where μ_{n0} is the adjusted electron mobility for lattice temperature, μ_0 is the initial input mobility, T_L is the lattice temperature, and τ is the temperature dependence coefficient. Through the Silvaco TCAD simulation software, we compared the internal temperature distributions of devices with different parameters under the same working conditions, and extracted the peak temperature in the device when the device reached thermal equilibrium. Then we can find which condition makes advantageous contribution to the device thermal management from these simulation data.

At room temperature, the thermal conductivities of β-Ga_2O_3 are different for different crystal orientations. Theoretically, the substrate, which has a higher thermal conductivity, can accelerate the heat dissipation from the device to the environment under the same work condition. Therefore, we simulated β-Ga_2O_3 SBDs on three different crystal orientation (100)/(–201)/(010) substrates, as illustrated in Fig. 1(a). These structures have a good geometrical symmetry, and the dotted line PP' in Fig. 1(a) is perpendicular to the device. The substrate thickness, doping concentration, and anode area of these three devices were 300 μm, 1.0×10^{16} cm^{-3}, and 100 μm^2, respectively. Platinum (Pt) and titanium (Ti) were set as Schottky and Ohmic contacts, respectively. A range of voltages from 0 V to 5 V with a step of 0.01 V were applied to these three devices, and the current–voltage (I–V) characteristics are shown in Fig. 1(b). The intersection of the orange dotted line and these solid lines indicates the same power density of 42.3 W/mm^2. In order to ensure that the devices were working at the same power density, the biases of 5/4.95/4.86 V were needed on the (100)/(–201)/(010) crystal orientation related devices. Figures 1(c)–1(e) are the temperature distributions of these three different devices under the same power density when the devices reached thermal equilibrium. The temperature rises of the three different devices along PP' are shown in Fig. 1(f), and the rise of (100) is the highest of 21.9 °C, followed by (–201) of 16.2 °C, and (010) is the lowest of 8.3 °C. Thus, it is important to fabricate device on the substrates with high thermal conductivity. But limited by the type of samples, we did not conduct the experiments with different substrate orientations.

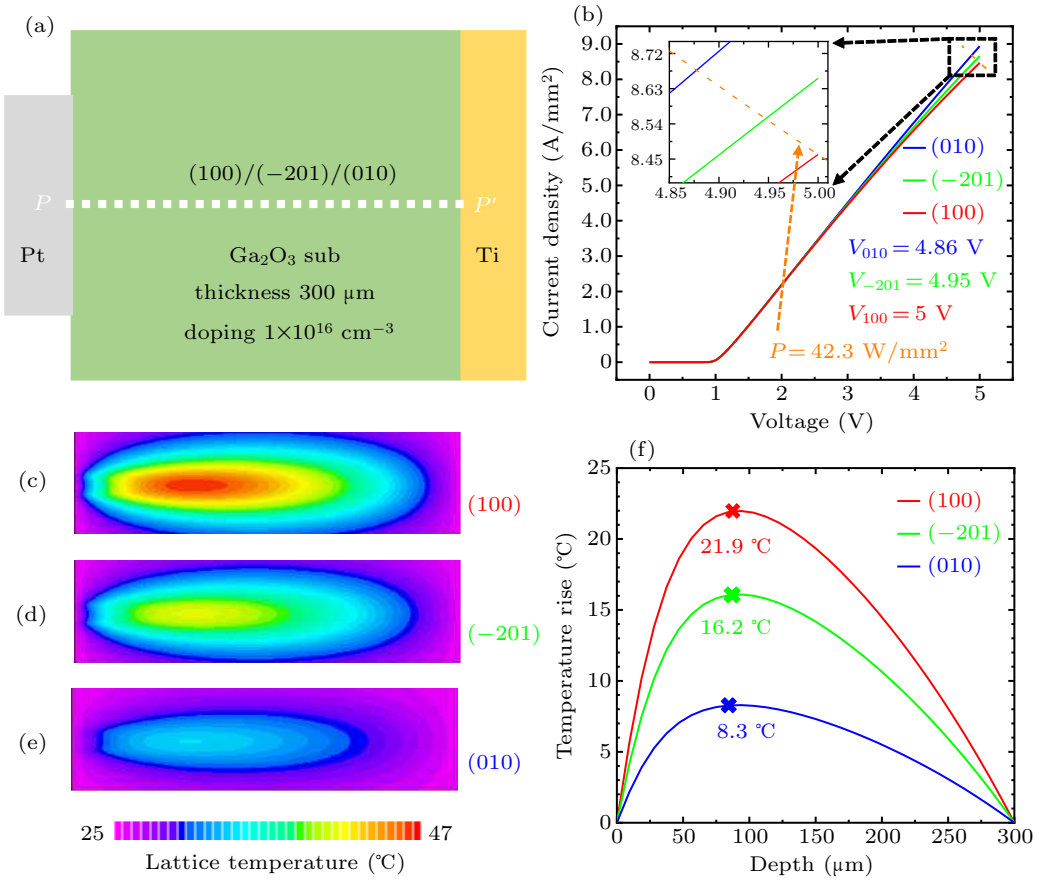


Fig. 1. TCAD simulation of crystal orientation dependence of thermal profile in SBDs. (a) Schematic of the device structure. (b) Comparison of the I–V characteristics for SBDs with (100)/(–201)/(010) orientation. (c)–(e) The temperature distribution of (100)/(–201)/(010) orientation substrate based device. (f) The temperature rises of the three different devices along PP'.

The heat of β-Ga_2O_3 SBDs is relatively concentrated at the Schottky junction, thus we simulated the temperature distribution with different Schottky contacts as respect of the area of the Schottky electrode and the work function of the contact metal. Figure 2(a) is the *I*–*V* curves under different electrode areas (100/200/300/400/500 μm^2). In order to make sure that the devices work at the same power density, the applied voltages of different areas are 3.37/4.08/4.49/4.79/5 V, respectively. The temperature rises of five devices along *PP*′ are shown in Fig. 2(b). When the area is 100 μm^2, the device temperature rise inside the device is the lowest one about 7.9 °C. As the anode area increases, the temperature rise goes up as well. The highest temperature rise is about 29.6 °C for the 500 μm^2 electrode area.

Figure 2(c) shows the *I*–*V* curves under different work functions (4.8/5.0/5.3 eV) of the Schottky metal, and the applied voltages corresponding to these work functions are 4.74/4.85/5 V, respectively. The temperature rises of the three different devices along *PP*′ are shown in Fig. 2(d). When the work function is 5.3 eV, the temperature inside the device is the minimum, and the temperature rise is about 21.1 °C. The maximum temperature rise is about 23.5 °C for the device with the work function of 4.8 eV. The probable reason is that higher work function means higher Schottky barrier height and larger contact resistance at the interface between the metal and the semiconductor substrate, resulting in more heat generated in the junction rather than in the substrate. It is noteworthy that the heat generated in the junction can be delivered to the air much more easily than the heat generated in the substrate. Hence the Schottky electrode with higher work function not only reduces the reverse leakage current, but also improves the heat dissipation of SBD devices.

At the same time, the heat generation of the substrate accounts for 70% of the SBD device.[30] Under different β-Ga_2O_3 substrate thicknesses, the heat distribution inside the device is studied in Fig. 3. The substrate thicknesses are 650/550/450/350/250 μm, respectively, as shown in Fig. 3(a). The area and the work function of the Schottky electrode are 100 μm^2 and 5.23 eV. The *I*–*V* comparison of the five devices is shown in Fig. 3(b), and the power density is approximately 32.6 W/mm^2, meaning that the applied voltages are set as 5/4.86/4.72/4.55/4.29 V, respectively. Figures 3(c)–3(g) are the temperature distributions of the five different Ga_2O_3 substrates, and the temperature rises along *PP*′ are shown in Fig. 3(h). The thinner substrate means the lower resistance in diode, which is certainly conducive to suppressing the generation of heat.

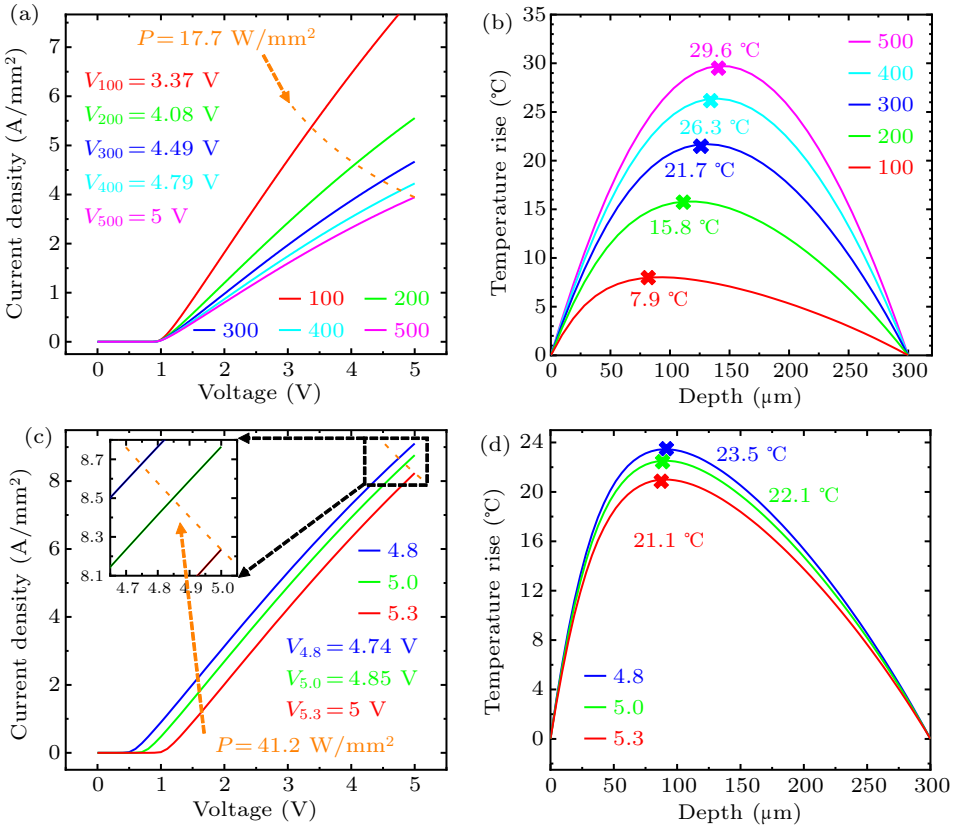


Fig. 2. TCAD simulation of anode area and work function. (a) Comparison of the *I*–*V* characteristic and (b) the temperature rises along *PP*′ for SBDs with five different anode areas of 500/400/300/200/100 μm^2. (c) Comparison of the *I*–*V* characteristic and (d) the temperature rises along *PP*′ for SBDs with three different work functions of 5.3/5.0/4.8 eV.

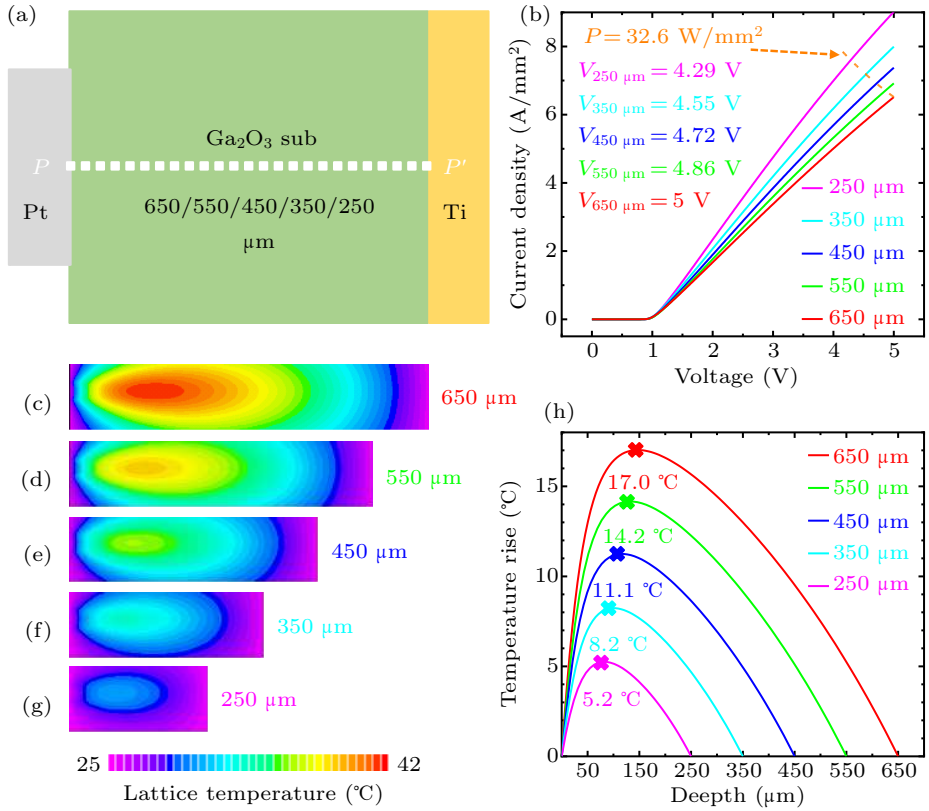


Fig. 3. TCAD simulation of substrate thickness dependence of thermal profile in SBDs. (a) Schematic of the device structure. (b) Comparison of the *I*–*V* characteristics for SBDs with substrate thicknesses of 650/550/450/350/250 μm. (c)–(g) The temperature distribution in diodes with substrate thicknesses of 650/550/450/350/250 μm. (f) The temperature rises of five different devices along *PP*′.

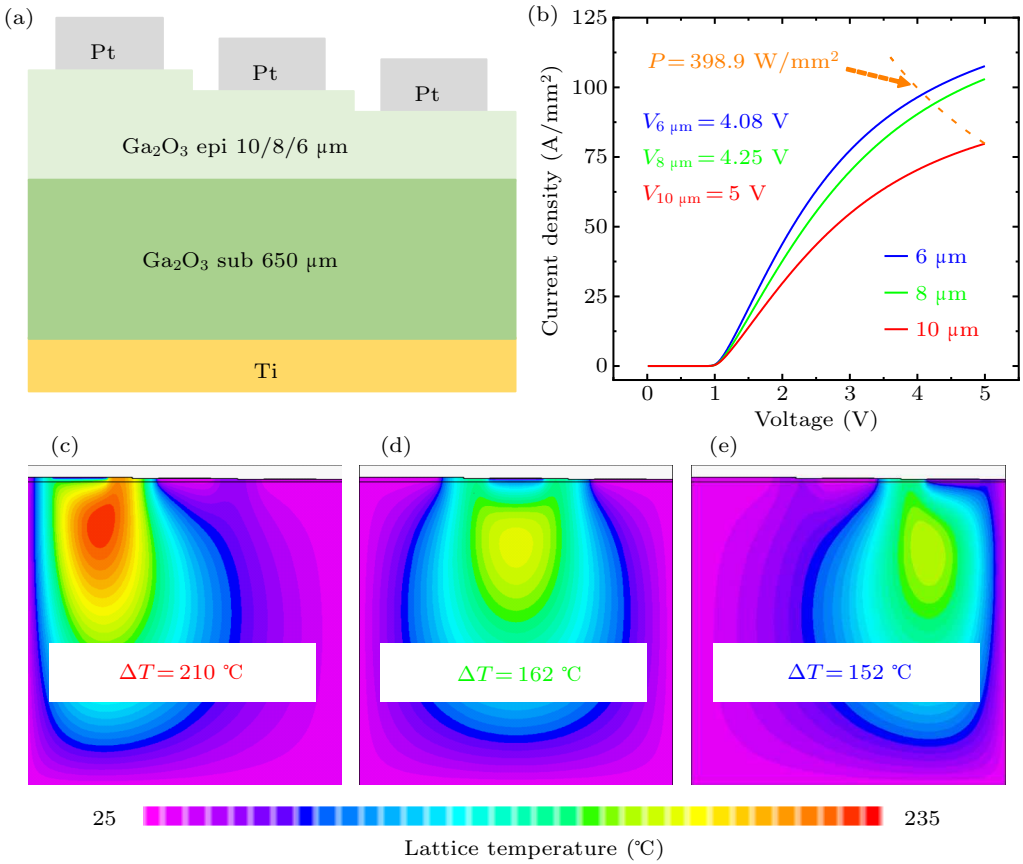


Fig. 4. TCAD simulation of epitaxial thickness dependence of thermal profile in SBDs. (a) Schematic of the device structure. (b) Comparison of the *I*–*V* characteristic for SBDs with 10/8/6 μm thickness epitaxial layer. (c)–(e) The temperature distribution in 10/8/6 μm epitaxial layer based diodes.

The substrate with HVPE epitaxial layer is the main platform to fabricate high performance SBD. The epitaxial layer of β-Ga_2O_3 SBD is low-doped and high-resistance compared to the substrate, which is the primary source of heat generation theoretically. As shown in Fig. 4(a), the thicknesses of the epitaxial layer were set as 10 μm, 8 μm, and 6 μm, respectively, and the thickness of the substrate was 650 μm. The doping concentrations of the β-Ga_2O_3 substrate and the epitaxial layer were set as 5.3×10^{18} and 2×10^{16} cm^{-3}, respectively. The crystal orientation we chosen was (100), and the thermal conductivity was 11 W/m·K, which are consistent with the actual SBD device. As shown in Fig. 4(b), the applied voltages were 5 V, 4.25 V, and 4.08 V, respectively. Figures 4(c)–4(e) show the three devices' different internal temperature distributions under the same power density. When the thickness is 10 μm, the peak temperature inside the device is the highest, and the temperature rise is about 210 °C as shown in Fig. 4(c), followed by the 8 μm thickness device about 162 °C in Fig. 4(d). The minimum temperature rise is about 152 °C with the 6 μm thickness as shown in Fig. 4(e). Theoretically for the need of 1.2 kV blocking voltage, the 3 μm epitaxial layer is enough for β-Ga_2O_3, in which the critical electric field can reach up to 8 MV/cm. In our experiment, the thinnest epitaxial layer is 6 μm, which means the breakdown voltages of all samples is above 1.2 kV. Therefore, thinning thickness has little impact on the device performance.

3. Experiments

The five SBDs on 5 mm × 7.5 mm unintentionally n-type doped (–201) β-Ga_2O_3 substrate with different substrate thicknesses (650/550/450/350/250/150 μm) were fabricated. The substrates were manufactured by Novel Crystal Technology, Inc. using edge-defined film-fed growth (EFG) method. Using the photoresist to protect the obverse side of the substrate, we thinned the substrate thickness by chemical mechanical polishing (CMP). After cleaning the substrate, etching the backsides surface through inductively coupled plasma (ICP) was definitely necessary to improve the ohmic contact before the ohmic electrode of Ti/Al/Ni/Au (10/80/50/100 nm) grown by E-beam evaporation equipment. Then the samples were put in the atmosphere of N_2 and annealed at 470 °C for 1 min to further improve the ohmic contact. Finally, after soaking in the BOE liquor, the Schottky electrode Ni/Au (40/200 nm) was deposited on the front side by E-beam evaporation.

The SBDs with different epitaxial layers were fabricated on a 640 μm substrate, also provided by Novel Crystal Technology, Inc. The doping concentrations of the substrate and the epitaxial layer are 5.3×10^{18} cm^{-3} and 2×10^{16} cm^{-3}, respectively. By using NR9-3000 photoresist as a mask, firstly two-third area of the left epitaxial layer was etched by ICP etching machine. The etching gas is BCl_3 with the etching time of 21 min. Secondly, we covered up the two-third area of the right epitaxial surface and etched the rest area by ICP with the same gas and the same time. Finally, the ohmic and Schottky contacts shared the same processes with the above mentioned single crystal substrate sample. The current–voltage and capacitance–voltage characteristics were measured by Keysight B1500A semiconductor device analyzer.

The infrared image is a quick, visual way to tell the temperature distribution of the working device. It should be noted that the surface temperature of transparent or specular materials cannot be accurately measured because of the working principle of infrared camera. The power was applied on the diodes by Kethley 2450 sourcemeter. It should mention that the same power was chosen by varying the voltage between 4 V and 5 V, at which the diodes normally work on. In order to improve the accuracy of measurement, we sprayed black, insulating, and washable lacquer on the sample surface.

4. Results and discussion

Figure 5(a) is the real chip image of the five single crystal substrate SBDs. Figure 5(b) is the thickness mapping scanned by a profiler of five different substrates. The forward *I*–*V* curve as shown in Fig. 6(a) is fundamentally in consistence with what has been simulated in Fig. 3(b). The *C*–*V* curve as shown in Fig. 6(b) indicates that the interfacial damage is not very severe.

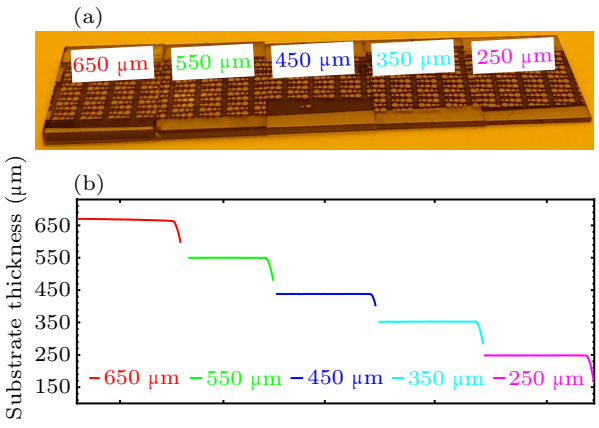


Fig. 5. (a) Photo of the devices with 650/550/450/350/250 μm substrate, (b) the step mapping of the five devices' surface.

The infrared images were taken by Fluke TiX580 infrared thermal camera at the same power density and the surface temperature distributions are shown in Figs. 6(c)–6(g). The peak surface temperature of the five devices' surface is 56.3 °C, 51.6 °C, 50.7 °C, 50.3 °C, and 49.5 °C, respectively, indicating the decrease of temperature rise with thinning the single crystal substrate.

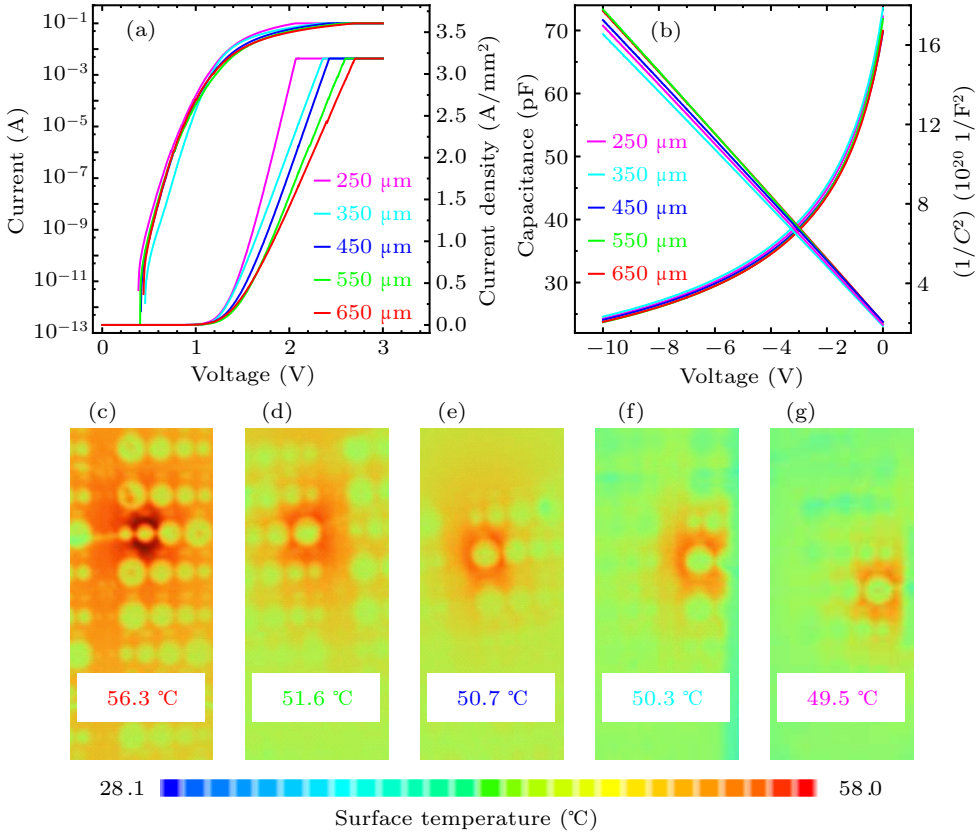


Fig. 6. Comparison of the (a) *I*–*V* and (b) *C*–*V* characteristics for SBDs with 650/550/450/350/250 μm thickness substrate. (c)–(g) The temperature distributions of five devices' surfaces.

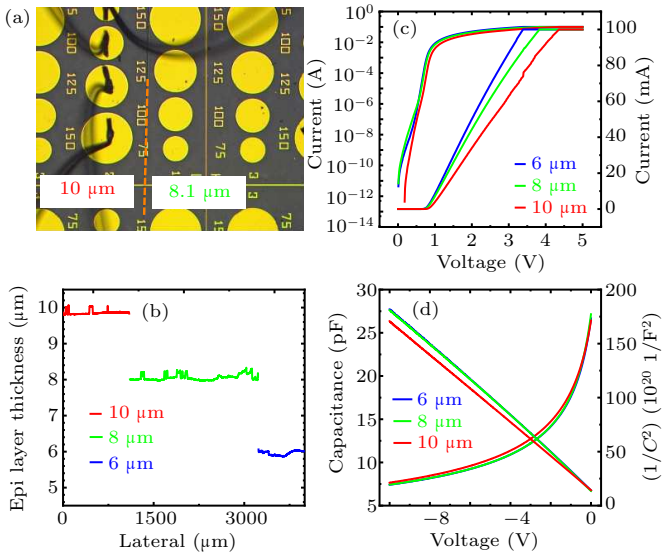


Fig. 7. (a) Photo of the devices with 10/8/6 μm epitaxial layer, (b) the step mapping of the five device's surfaces. Comparison of the (c) *I*–*V* and (d) *C*–*V* characteristics of SBDs with different thickness epitaxial layers.

Figure 7(a) is the schematic diagram of the actual device structure with a 650 μm thickness β-Ga_2O_3 substrate and a 10 μm or 8.1 μm thickness epitaxial layer. This diagram was taken after wire bonding, and the shading in it is the gold wire used in bonding. Figure 7(b) is epitaxial thickness mapping scanned by the profiler after twice etching and washing. Actually, these two etching depths are 1.9 μm and 2.1 μm, respectively. It is one possible reason that the etching rate of ICP gets slower and slower as time goes on. The forward *I*–*V* curve as shown in Fig. 7(c) is fundamentally in consistence with what has been simulated in Fig. 4(b). The *C*–*V* curve as shown in Fig. 7(d) indicates that the quality of the Schottky interface keeps similar after etching.

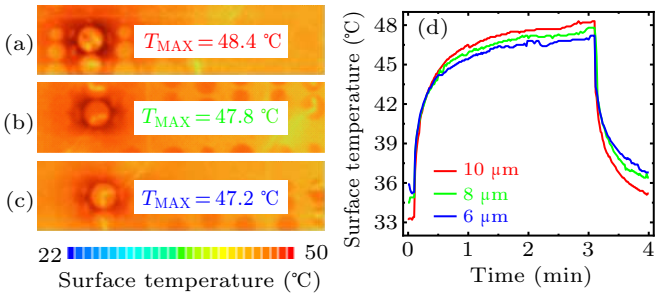


Fig. 8. Infrared imaging test of devices. (a)–(c) Temperature distribution of three devices' surface, and (d) the temperature rises with the time of applied voltage.

The infrared images were taken by Fluke TiX580 infrared thermal camera at the same power density and the surface temperature distributions are shown in Figs. 8(a)–8(c). The peak surface temperatures of the three devices are 48.4 °C, 47.8 °C, and 47.2 °C, respectively, indicating the decrease of temperature rise with thinning the epitaxial layer. From Fig. 8(d), the temperature rise trend agrees with the simulation results. But there is a big difference of peak temperature between the simulation data and the experiment data. This distinction stems from the different temperatures between simulation and ex-

periment, where the internal peak temperature was calculated in simulation, but the interface temperature was measured in experiment.

5. Conclusion

In this work, we simulated SBDs with different crystal orientations, Schottky contacts, substrates, and epitaxial layer thicknesses systematically. The simulation results indicate that β-Ga_2O_3 should be with (010) crystal orientation, a smaller anode area, larger work function metal, thinner substrates and epitaxial layers for reducing the self-heating effect inside the diodes. In addition, five SBDs with different substrate thicknesses were fabricated on a (–201) β-Ga_2O_3 single-crystal substrate and three SBDs with different epitaxial layer thicknesses were fabricated on a (001) substrate in our study. The devices show good forward electrical characteristics, which are almost consistent with the simulations. The experiments data verifies the decrease of temperature rise by thinning the substrate thickness and epitaxial layer. This work opens a new route to overcome the issue of low thermal conductivity for β-Ga_2O_3 power electronic applications.

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