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# Simulations of monolayer SiC transistors with metallic 1T-phase $MoS_2$ contact for high performance application*

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We preform a first-principles study of performance of 5 nm double-gated (DG) Schottky-barrier field effect transistors (SBFETs) based on two-dimensional SiC with monolayer or bilayer metallic 1T-phase $MoS_2$ contacts. Because of the wide bandgap of SiC, the corresponding DG SBFETs can weaken the short channel effect. The calculated transfer characteristics also meet the standard of the high performance transistor summarized by international technology road-map for semiconductors. Moreover, the bilayer metallic 1T-phase $MoS_2$ contacts in three stacking structures all can further raise the ON-state currents of DG SiC SBFETs in varying degrees. The above results are helpful and instructive for design of short channel transistors in the future.

**Keywords:** Schottky-barrier field effect transistor, SiC, band structure, short channel effect

**PACS:** 71.15.Mb, 73.20.–r, 73.63.–b, 73.40.–c **DOI:** 10.1088/1674-1056/abeee0

## 1. Introduction

In the past few decades, design and development of advanced low dimensional materials in general for electronic applications of post-silicon era have been an extensive research topic.[1,2] Graphene and graphene-like two-dimensional (2D) materials have become some of the most promising candidates to replace the traditional silicon-based materials due to their unique physical, chemical, and electronic properties.[3–10] So far, fabrication and simulation of field effect transistors (FETs) based on 2D materials are one of the latest research focuses in recent years.[11–16] More importantly, with progress of advanced fabrication and measurement technology, sizes of the above 2D FETs are gradually reduced, and the performance is becoming more and more excellent. The recent studies show that the lateral transition-metal dichalcogenides Schottky-barrier FETs (SBFETs) can provide the best performance and meet the standard of the high-performance (HP) transistor summarized by international technology road-map for semiconductors (ITRS) (international technology road-map for semiconductors, 2013 version).[17,18] However, evaluation of their potential applications to work in sub-5 nm size is still in its infancy due to lack of effective methods overcoming the short channel effect.

If we would further improve the application of 2D materials in FETs, we must explore more diversified methods to overcome the short channel effect.[19,20] Recently, an effective way to solve this problem is to select wide band gap 2D materials as the channel of FETs. The SiC SBFET with Pd contact can effectively reduce the leakage current and just meet the standard of the HP 5 nm transistor.[21] Although the performances of this SiC SBFET can be improved by the gate-source/drain underlap, the channel size has changed a lot, and it is indeed not really a 5 nm FET.[22] Therefore, how to improve the ON-state current of 5 nm FETs as much as possible becomes an important issue for applications of the FETs. Motivated by recent advances in 2D vertical van der Waals heterojunctions,[23–29] in this paper, we preform a first-principles study of 5 nm double-gated (DG) SBFETs based on 2D SiC with monolayer (ML) or bilayer (BL) 1T-phase $MoS_2$ contacts. The calculated transfer characteristics also meet the standard of the high performance transistor summarized by international technology road-map for semiconductors (ITRS, 2013 version).

## 2. Model and methods

Figure 1 shows the DG SBFETs based on 2D SiC. The source and the drain are monolayer or bilayer metallic 1T-phase $MoS_2$, which was successfully synthesized

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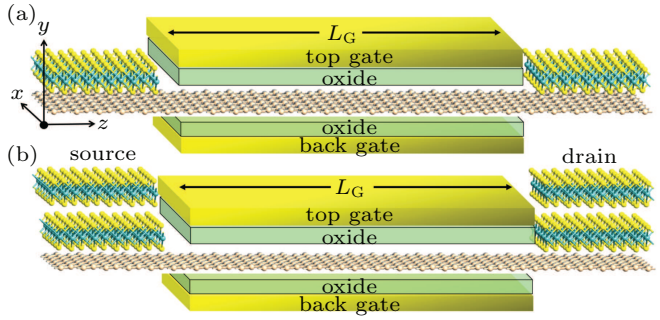



**Fig. 1.** The detailed structures of DG 5 nm SBFETs based on 2D SiC with (a) monolayer or (b) bilayer 1T-phase $MoS_2$ contacts.

experimentally. The channel is 2D SiC and its length ($L_G$) is 5 nm. The corresponding effective oxide thickness (EOT) of each dielectric region was set to 0.41 nm. The supply voltage ($V_{DD}$) is 0.64 V, which is the bias voltage between the source and the drain. The transfer characteristics are calculated using the density-functional theory (DFT) coupled with the non-equilibrium Green's function (NEGF) formalism implemented in the QuantumATK code.[30] The exchange and cor-relations were described by the Perdew–Burke–Ernzerhof (PBE) functional under the generalized gradient approximation (GGA) with van der Waals (vdw) correction proposed by Grimme (DFT-D2). The Landauer formula

$$I(V_{ds},V_g) = \frac{2e}{h}\int \{T(E,V_{ds},V_g) \times [f_S(E-\mu_S) - f_D(E-\mu_D)]\}\,dE$$

is used to calculated the current.[31] Here, $T(E,V_{ds},V_g)$ is the transmission coefficient at given gate voltage $V_g$ and bias voltage $V_{ds}$, $f_{S/D}$ are the Fermi–Dirac distribution functions of the source/drain electrodes, and $\mu_{S/D}$ are the electrochemical potential of the source/drain electrode.

## 3. Results and discussion

The band structures of the rectangular unit cells of 2D SiC 1T-phase $MoS_2$ and SiC/1T-phase $MoS_2$ stacking system are present in Fig. 2. The corresponding rectangular geometric structures are supplied in the figure. In Fig. 2(a), the band gap of rectangular unit cell of 2D SIC is 2.64 eV, which accords with the former experimental and theoretical results.[21,22,32] In Fig. 2(b), the Bravais vector of the hexagonal lattice of 1T-phase $MoS_2$ is 3.15 Å, and the calculated band structure shows a metal behavior. A rectangular cell of 1T-phase $MoS_2$ are easily adjusted to a rectangular cell of SiC with a small amount of mismatch due to their very similar lattices. The valence bands and the conduction bands of SiC are slightly distorted due to the weak band hybridization in SiC/1T-phase $MoS_2$ contacts, as can be seen in Fig. 2(c). The Fermi level of 1T-phase $MoS_2$ nearly crosses the center of the SiC band gap, indicating the similar electron Schottky barrier height (SBH) and hole SBH.

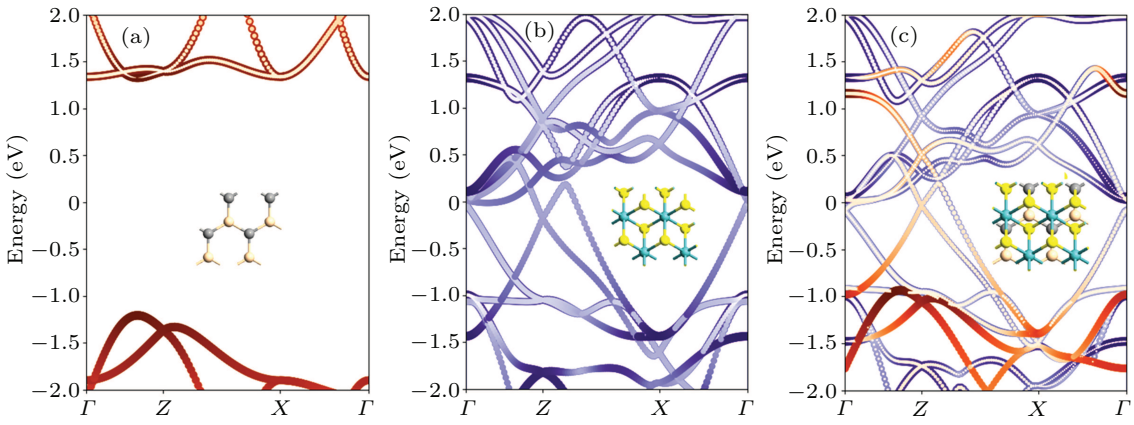



**Fig. 2.** Band structures of the rectangular unit cells of (a) SiC, (b) 1T-phase $MoS_2$ and (c) SiC/1T-phase $MoS_2$.

The corresponding transmission spectra of DG SBFETs based on 2D SiC with ML and BL 1T-phase $MoS_2$ contacts are shown in Fig. 3. The gate and bias voltages are set as zero. The detail geometric structures of AA-stacked, AB-stacked and AC-stacked BL 1T-phase $MoS_2$ are shown in Figs. 3(b)–3(d). One can find that there is a energy gap of 2.64 eV in every transmission spectrum, which originates from the band gap of 2D SiC (2.64 eV). Moreover, transmission coefficients around the valence band maximum (VBM) of four DG SBFETs are obviously larger than that around the conduction band minimum (CBM). The energy differences between the Fermi level of 1T-phase $MoS_2$ and the VBM of the 2D SiC in the transmission spectrum can be considered as the hole SBH of the DG SBFET.[33] In Fig. 3(a), the hole SBH of DG 5.1 nm SBFET based on 2D SiC with monolayer 1T-phase $MoS_2$ contact is 1.52 eV. In Fig. 3(b), the transmission spectrum shifts to left relative to the Fermi level of the AA-stacked BL 1T-phase $MoS_2$ resulting in the increase of hole SBH to 1.64 eV. For the DG 5.1 nm SBFETs based on 2D SiC with AB-stacked and AC-stacked BL 1T-phase $MoS_2$ contacts, the transmission spectra move further to the left by the approximate value resulting in the hole SBH increasing to 1.88 eV and 1.87 eV,

as shown in Figs. 3(c) and 3(d). In addition, the transmission coefficients around the CBM will also show the significant reductions. In other words, bilayer 1T-phase $MoS_2$ contacts will greatly affect the SBH and the electronic transport properties of devices compared to ML 1T-phase $MoS_2$ contact. The main reason for the changes of the SBH is the different Fermi levels of the bilayer 1T-phase MoS2 contacts under different stacked structures.

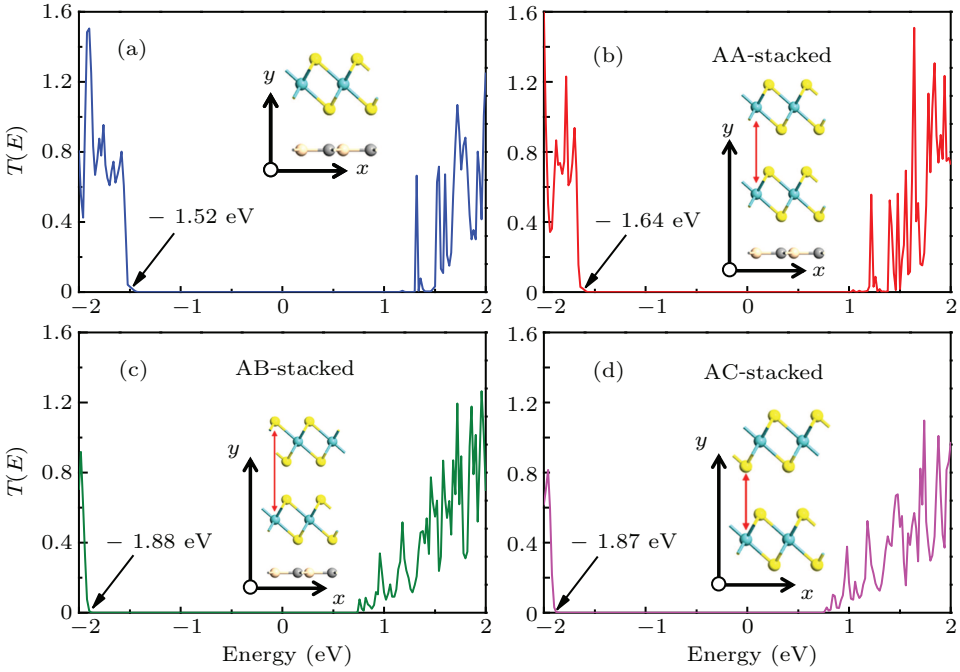



**Fig. 3.** (a) Zero bias transmission spectrum of DG SBFET based on 2D SiC with ML 1T-phase $MoS_2$ contact. Zero bias transmission spectra of DG SBFETs based on 2D SiC with (b) AA-stacked, (c) AB-stacked and (d) AC-stacked BL 1T-phase $MoS_2$ contacts.

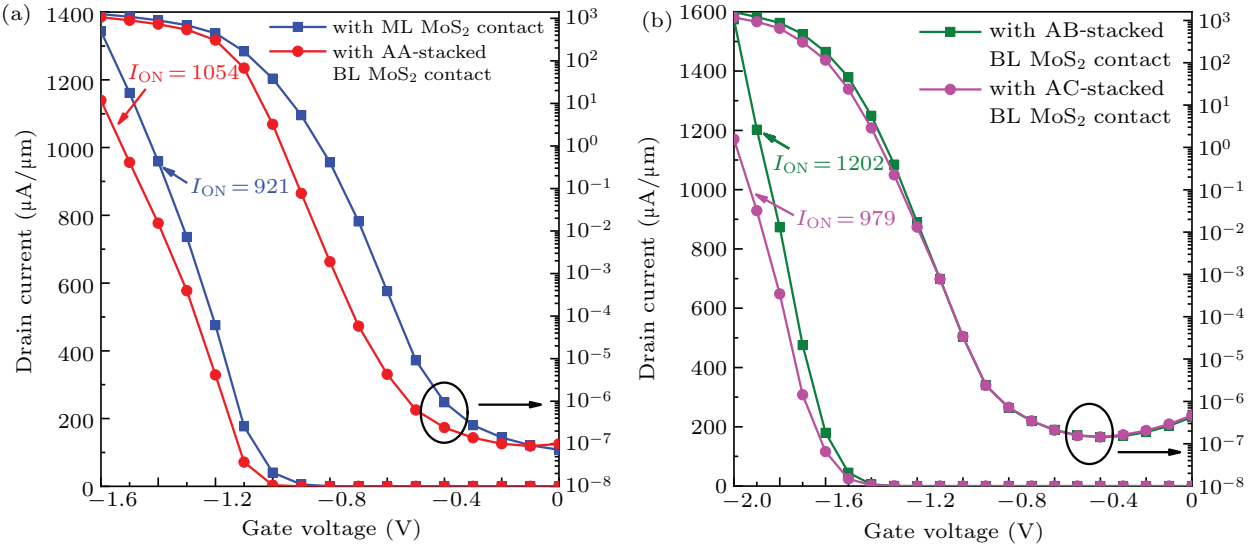



**Fig. 4.** (a) Transfer characteristics of DG SBFETs based on 2D SiC with ML 1T-phase $MoS_2$ contact and AA-stacked BL 1T-phase $MoS_2$. (b) Transfer characteristics of DG 5 nm SBFETs based on 2D SiC with AB-stacked and AC-stacked BL 1T-phase $MoS_2$. ON-state currents are shown in all the figures.

Figure 4 shows the transfer characteristics in linear and logarithmic forms of all DG SBFETs based on 2D SiC with ML or BL 1T-phase $MoS_2$ contacts. OFF current ($I_{OFF}$) is set at 0.1 μA/μm, and ON-state current ($I_{ON}$) must be larger than 900 μA/μm following the stander required by ITRS (2013 version). In the transfer characteristics, the ON-state current corresponds to the current at the gate voltage of $V_{ON}$ ($V_{ON} = V_{OFF} + V_{DD}$). $V_{OFF}$ is the gate voltage of $I_{OFF}$ and $V_{DD}$ is the supply voltage (0.64 V). In Fig. 4(a), the drain current of DG SBFETs based on 2D SiC with monolayer $MoS_2$ contact is lower than $10^{-7}$ μA/μm on zero gate voltage. After applying negative gate voltage, the drain currents will increase slowly first and then rise rapidly after −0.3 V gate voltage. The ON-state current is 921 μA/μm, is slightly higher than the standard required by HP application (900 μA/μm). In addition, the drain currents of DG SBFETs based on 2D SiC with AA-stacked BL 1T-phase $MoS_2$ contact also increase slowly first and then rise rapidly after −0.5 V gate voltage.

In Fig. 4(a), one can find that the threshold swing value (describing the gate-control ability) of DG SBFETs with AA-stacked BL 1T-phase $MoS_2$ contact is obviously lower than that of DG SBFETs with ML 1T-phase $MoS_2$ contact. Thus, the corresponding ON-state current is 1054 μA/μm, which is higher than that of DG SBFETs with ML 1T-phase $MoS_2$ contact. However, in Fig. 4(b), the threshold swing values of DG SBFETs with AB-stacked and AC-stacked BL 1T-phase $MoS_2$ contacts are nearly same with each other. The corresponding ON-state currents are slightly different, even though they have the similar hole SBHs. The ON-state current of DG SBFET with AB-stacked BL 1T-phase $MoS_2$ contact is 979 μA/μm. The ON-state current of DG SBFET with AC-stacked BL 1T-phase $MoS_2$ contact is 1202 μA/μm, which is largest in four DG SBFETs. Although the BL metallic 1T-phase $MoS_2$ contacts in three stacked structures have different effects on the transfer characteristics of DG 2D SiC SBFETs, they all can further raise the ON-state currents of DG SiC-SBFETs compared to the device with the ML 1T-phase $MoS_2$ contact.

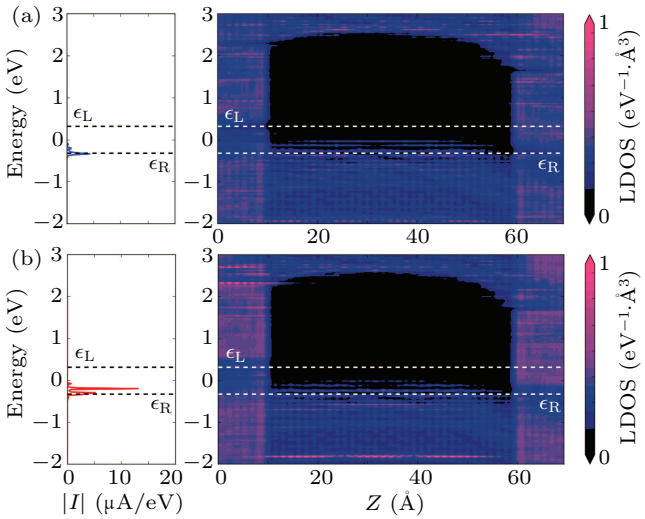



**Fig. 5.** Spectral currents and LDOS of DG SBFETs based on 2D SiC with (a) monolayer 1T-phase $MoS_2$ contact and (b) AA-stacked BL 1T-phase $MoS_2$ at ON-state gate voltages.

In order to explore the different transfer characteristics of DG SBFETs based on 2D SiC with ML and BL 1T-phase $MoS_2$ contacts, we perform analyses on their spectral currents and local density of state (LDOS) at ON-state gate voltages in Figs. 5 and 6. Here, one can see that there is the obvious direct tunneling through the barriers resulting in the drain currents. So, one can find there are three spectral current peaks in the region between the $E_F$(S) and $E_F$(D) leading to the high currents in Fig. 5(a). Although the DG SBFET based on 2D SiC with AA-stacked BL 1T-phase $MoS_2$ contact has a larger hole SBH compared to that of the DG SBFET based on 2D SiC with ML1T-phase $MoS_2$ contact, the corresponding three spectral current peaks are higher than that of the DG SBFET based on 2D SiC with ML 1T-phase $MoS_2$ contact as shown in Fig. 5(b). Consequently, the DG SBFET based on 2D SiC with AA-stacked BL 1T-phase $MoS_2$ contact has a larger ON-state current (1054 μA/μm) than the ON-state current of the DG SBFET based on 2D SiC with ML 1T-phase $MoS_2$ contact (921 μA/μm). The reason for the increase of ON-state current is that the AA-stacked BL 1T-phase $MoS_2$ contact has the larger DOS which can provide more incoming wave functions from the source region to the drain region.

For the DG SBFET based on 2D SiC with AB-stacked and AC-stacked BL 1T-phase $MoS_2$ contacts, there are two direct tunneling passageways around $E_F$(D) to dominate the drain currents at the ON state resulting in two spectral current peaks in the region between the $E_F$(S) and $E_F$(D) as can be seen from Fig. 6. In Fig. 6(a), two spectral current peaks are nearly the same as high values leading to the big ON-state current (1202 μA/μm) for the DG SBFET based on 2D SiC with AB-stacked BL 1T-phase $MoS_2$ contact. Although there still two spectral current peaks for the DG SBFET based on 2D SiC with AC-stacked BL 1T-phase $MoS_2$ contact in the region between the $E_F$(S) and $E_F$(D), one of them has a similar large value and the other has a small value compared to that of the DG SBFET based on 2D SiC with AB-stacked BL 1T-phase $MoS_2$ contact as shown in Fig. 6(b). As a result, the ON-state current (979 μA/μm) is lower than the ON-state current of DG SBFET based on 2D SiC with AB-stacked BL 1T-phase $MoS_2$ contact. In other words, the AB-stacked BL 1T-phase $MoS_2$ contact has the larger DOS than that of AC-stacked BL 1T-phase $MoS_2$ contact, which can provide more incoming wave functions from the source to the drain resulting in the higher ON-state current. The bilayer metallic 1T-phase $MoS_2$ contacts in three stacking structures all can further raise the ON-state currents of DG SiC-SBFETs in varying degrees.

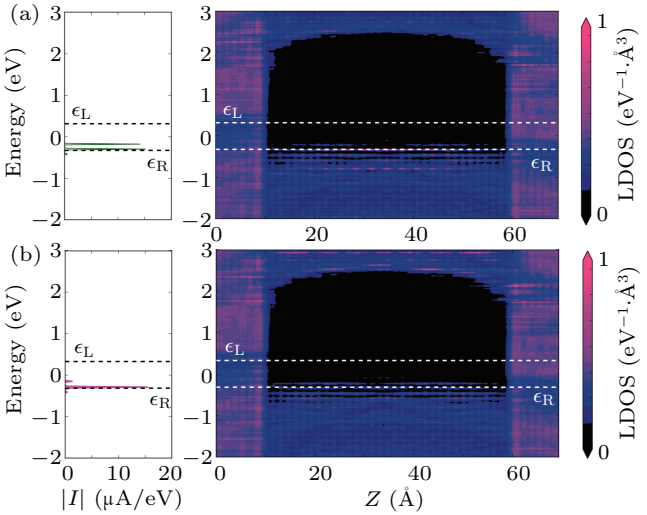



**Fig. 6.** Spectral currents and LDOS of DG SBFETs based on 2D SiC with (a) AB-stacked and (b) AC-stacked BL 1T-phase $MoS_2$ at ON-state gate voltages.

Benchmarks of performance of DG SBFETs based on 2D SiC with ML and AA-stacked, AB-stacked, AC-stacked BL 1T-phase $MoS_2$ contacts are shown in Table 1. ON-state

currents ($I_{ON}/I_{OFF}$) of DG SBFETs based on 2D SiC with ML and AA-stacked, AB-stacked, AC-stacked BL 1T-phase $MoS_2$ contacts are 921 μA/μm ($9.21\times10^3$), 1054 μA/μm ($1.054\times10^4$), 1202 μA/μm ($1.202\times10^4$), and 979 μA/μm ($9.79\times10^3$), which all overstep the stander of HP FET for the production year 2028. The intrinsic gate capacitance $C_g$ is calculated from the equation of $C_g = \partial Q_{ch}/\partial V_G$.[34] Table 1 shows that the $C_g$ values of four DG SBFETs are 0.181 fF/μm, 0.206 fF/μm, 0.235 fF/μm, and 0.186 fF/μm. This shows that parameters $C_g$ of four FETs are also very satisfactory. In addition, the dynamic power indicator (DPI) and the intrinsic transistor delay time $\tau$ are considered as the two other important FET parameters of merit, reflecting the energy and time the FET needs to switch. The DPI per width is calculated by the formula of DPI $= (C_g \times V_{dd}^2)/W$, where $W$ is the channel width.[34] The intrinsic transistor delay time $\tau$ can be calculated by the formula $\tau = (C_g \times V_{dd})/I_{ds}$.[34] One can see from Table 1 that the DPIs of four DG SBFETs are 0.074 fJ/μm, 0.084 fJ/μm, 0.096 fJ/μm, and 0.077 fJ/μm, respectively. Although there are slight differences from each other, the DPIs of four DG SBFETs are far below the standard of the ITRS requirement. The intrinsic transistor delay times of four SBFETs are 0.126 ps, 0.125 ps, 0.125 ps, and 0.122 ps, which are all less than the ITRS (2013 version) requirement of HP FET (0.423 ps). Moreover, one can see that the intrinsic transistor delay times of four SBFETs are nearly same with each other. In other words, the intrinsic transistor delay time is a stable parameter for DG SBFETs based on 2D SiC whatever with ML 1T-phase $MoS_2$ contact or with BL 1T-phase $MoS_2$ contacts under the different stacked structures.

**Table 1.** Benchmarks of performance for DG SBFETs based on 2D SiC with ML and AA-stacked, AB-stacked, AC-stacked BL 1T-phase $MoS_2$ contacts relative to the HP devices standers of the next decades.

| | $I_{ON}$ (μA/μm) | $I_{ON}/I_{OFF}$ | $C_g$ (fF/μm) | DPI (fJ/μm) | $\tau$ (ps) |
|---|---|---|---|---|---|
| ITRS HP (2028) | 900 | $9.0\times10^3$ | 0.595 | 0.243 | 0.423 |
| SiC-SBFET with ML $MoS_2$ contact | 921 | $9.21\times10^3$ | 0.181 | 0.074 | 0.126 |
| With AA-stacked BL $MoS_2$ contact | 1054 | $1.054\times10^4$ | 0.206 | 0.084 | 0.125 |
| With AB-stacked BL $MoS_2$ contact | 1202 | $1.202\times10^4$ | 0.235 | 0.096 | 0.125 |
| With AC-stacked BL $MoS_2$ contact | 979 | $9.79\times10^3$ | 0.186 | 0.077 | 0.122 |

## 4. Conclusion

In summary, we have preformed a first-principles study of performances of 5 nm double-gated (DG) Schottky-barrier field effect transistors (SBFETs) based on two-dimensional SiC with monolayer or bilayer metallic 1T-phase $MoS_2$ contacts. Because of the wide bandgap of SiC, the corresponding DG SBFETs of 2D SiC with monolayer 1T-phase $MoS_2$ contact can weaken the short channel effect. The calculated transfer characteristics also meet the standard of the high performance transistor summarized by ITRS. The corresponding ON-state current is 921 μA/μm, which is slightly higher than the standard required by HP application (900 μA/μm). Moreover, the bilayer metallic 1T-phase $MoS_2$ contacts in three stacking structures all can further raise the ON-state currents of 5 nm DG SiC-SBFETs in varying degrees. The ON-state current of DG SBFET with AC-stacked BL 1T-phase $MoS_2$ contact is 1202 μA/μm, which is largest in four DG SBFETs. The intrinsic gate capacitance, the dynamic power indicator and the intrinsic transistor delay time of our 2D SiC DG SBFETs are all better than the standard summarized by ITRS. Hence, the above results are very helpful and instructive for the design of short channel transistors in the future.

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