

A super-junction SOI-LDMOS with low resistance electron channel

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A super-junction SOI-LDMOS with low resistance electron channel

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A novel super-junction LDMOS with low resistance channel (LRC), named LRC-LDMOS based on the silicon-on-insulator (SOI) technology is proposed. The LRC is highly doped on the surface of the drift region, which can significantly reduce the specific on resistance ($R_{on,sp}$) in forward conduction. The charge compensation between the LRC, N-pillar, and P-pillar of the super-junction are adjusted to satisfy the charge balance, which can completely deplete the whole drift, thus the breakdown voltage (BV) is enhanced in reverse blocking. The three-dimensional (3D) simulation results show that the BV and $R_{on,sp}$ of the device can reach 253 V and 15.5 mΩ·cm^2, respectively, and the Baliga's figure of merit ($FOM = BV^2/R_{on,sp}$) of 4.1 MW/cm^2 is achieved, breaking through the silicon limit.

Keywords: LDMOS, breakdown voltage (BV), specific on resistance ($R_{on,sp}$), figure of merit (FOM)

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1. Introduction

THE silicon-on-insulator lateral double-diffused metal–oxide–semiconductor (SOI-LDMOS) is widely adopted in power ICs due to its voltage control and high switching frequency characteristics.[1–3] For example, RF power LDMOS is widely used in wireless communication.[4] The breakdown voltage (BV) of reverse blocking and the specific on resistance ($R_{on,sp}$) of forward conduction are essential properties for the LDMOS, and the Baliga's figure of merit (FOM) is proposed to evaluate the trade-off relationship between the BV and the $R_{on,sp}$. Many advanced structures are proposed to improve the FOM in recent years.[5–11] Specifically, the super-junction (SJ) technology is one of the most widely used methods. It can not only effectively reduce the $R_{on,sp}$ but also increase the BV, and the FOM is significantly improved.[12–18] In the design of LDMOS, SJ is used in many structures. For example, the BSD-SJLDMOS proposed by Duan Baoxing *et al.*[19] And, MFBL-SJLDMOS proposed by Cao *et al.*[20] In addition, We realize the structure with lateral width variation using super-junction technology and call it VLW-LDMOS.[21,22]

In this paper, a SOI-LDMOS based on the super-junction technology with low resistance channel (LRC) is proposed. The charge compensation between the LRC and the super-junction are optimized to further improve the FOM.

2. Device structure and parameters

The structure of the proposed LRC-LDMOS is shown in Fig. 1. Compared with the conventional SJ SOI-LDMOS, a low resistance channel (LRC) is introduced on the surface of the drift region, which can significantly reduce the $R_{on,sp}$ of the device during the forward conduction state. At the same time, an SJ structure is designed directly below the LRC. In the reverse blocking state, it can not only completely deplete the LRC but also can optimize the surface and bulk electric field in the drift region.

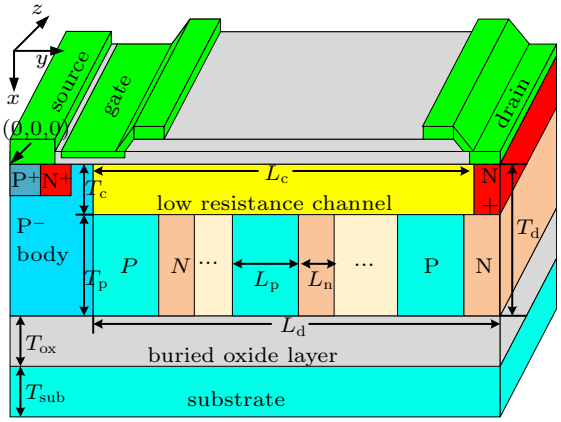


Fig. 1. Structure for the proposed LRC-LDMOS.

The key parameters of the conventional LDMOS (CON-LDMOS), conventional SJ LDMOS (CON-SJLDMOS), variation of lateral width LDMOS (VLW-LDMOS), and the proposed LRC-LDMOS are designed to be the same. The thickness and length of the N-drift T_d are 5 μm and 16 μm, respectively. The doping concentration, thickness T_{sub} of p-type substrate are 8×10^{14} cm^{-3} and 2 μm, respectively. In addition, thickness T_{ox} of buried oxide layer is 2 μm. For the CON-LDMOS, the doping concentration of the N_{drift} is set as

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2×10^{15} cm^{-3}. For the CON-SJLDMOS, the width and doping of the N-pillar and P-pillar are set to be the same with 0.5 μm and 1×10^{16} cm^{-3}. For the VLW-LDMOS, the doping concentration of the N_{sj} is set as 1.0×10^{16} cm^{-3}. For the LRC-LDMOS, the doping N_{sj} and thickness T_p of the N-pillar and P-pillar both are 5×10^{14} cm^{-3} and 4 μm, respectively. The length L_n of N-pillar and L_p of P-pillar are 0.7 μm and 1.3 μm. The thickness T_c and doping concentration N_c of the LRC are 1 μm and 1×10^{16} cm^{-3}, respectively. The electrical characteristics of the device are designed and investigated with TCAD SENTAURUS. The physical and electrical models, including the mobility, ionization, and the recombination models are adopted in the simulation.

3. Electrical characteristics

3.1. The reverse breakdown voltage *BV*

Figure 2 shows the relationship between breakdown voltage and doping concentration in drift region of CON-LDMOS, CON-SJLDMOS, and VLW-LDMOS. Figure 3 shows the equi-potential contours and the depletion layers of the LDMOSs at breakdown state, the source, gate, and the P-substrate are shorted to the ground, and the drain is applied with positive voltage. For the CON-SJLDMOS, the equi-potential contours are sparse in the N-drift when the device breaks down at the voltage of 215 V as shown in Fig. 3(b). For the CON-LDMOS, the device will breakdown at the drain voltage of 231 V, and the equi-potential contours get much denser both at the surface and in the bulk of the N-drift as shown in Fig. 3(a). For the VLW-LDMOS, the device will breakdown at the drain voltage of 237 V, the equi-potential contours get much denser both at the surface and in the bulk of the N-drift as shown in Fig. 3(c). For the proposed LRC-LDMOS, the LRC, N-pillar, and P-pillar are exhausted each other, and the device will breakdown at the drain voltage of 253 V. The equi-potential lines are dense and more uniformly distributed in the drift region as shown in Fig. 3(d). From the point view of the depletion layers, the whole N-drift are completely depleted at the breakdown state, which indicate that the maximum *BV* are achieved for all the devices.

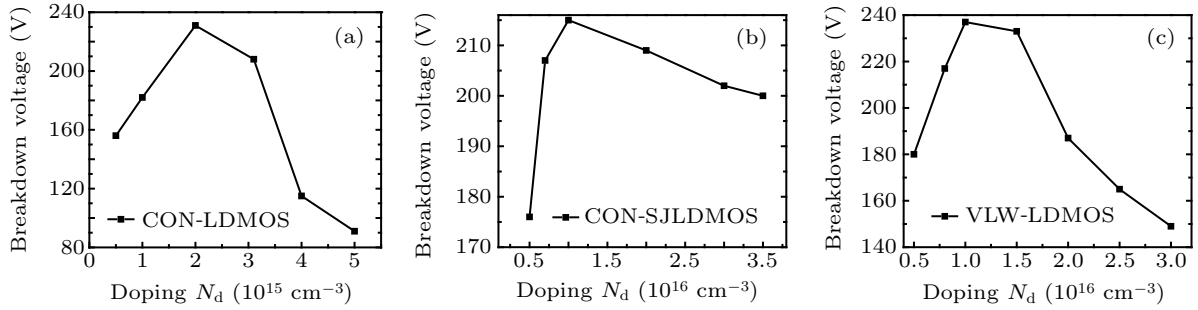


Fig. 2. The breakdown voltage changes with doping concentration in drift region for (a) CON-LDMOS, (b) CON-SJLDMOS, and (c) VLW-LDMOS.

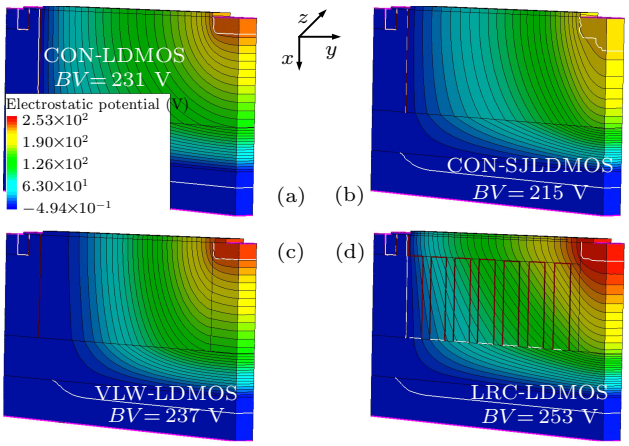


Fig. 3. Equi-potential contours and depletion layers for (a) conventional LDMOS, (b) conventional super-junction LDMOS, (c) VLW-LDMOS, and (d) LRC-LDMOS.

Figure 4 provides the surface, bulk, and bottom electric field distributions along the lateral direction for the devices. In Fig. 4(a), the surface peak electric fields E_{peak} of CON-LDMOS, CON-SJLDMOS, and VLW-LDMOS appear at the contact surface between the drain and N-drift region with values of 3.8×10^5 V/cm, 3.5×10^5 V/cm, and 2.9×10^5 V/cm, respectively. The surface E_{peak} with value 3.4×10^5 V/cm of LRC-LDMOS appears at the P-body/N-drift junction. Furthermore, the average electric field intensity of the entire N-drift region is enhanced because of the charge compensation between the LRC and the SJ. The bulk E_{peak} of the four devices at $x = 1.0$ μm is shown in Fig. 4(b), the E_{peak} of CON-LDMOS, CON-SJLDMOS, VLW-LDMOS, and LRC-LDMOS appear at the drain region with values of 3.4×10^5 V/cm, 3.1×10^5 V/cm, 3.2×10^5 V/cm, 3.0×10^5 V/cm, respectively. Moreover, the average bulk E_{peak} of LRC-LDMOS is much higher than that of the other three devices. The bulk E_{peak} of the four devices at $x = 3.0$ μm is shown in Fig. 4(c), and the bottom E_{peak} at $x = 5.0$ μm between the N-drift and the BOX is shown in Fig. 4(d). It can be seen that not only the average bulk electric distribution but also the bottom electric of the LRC-LDMOS are higher than that of the other three devices.

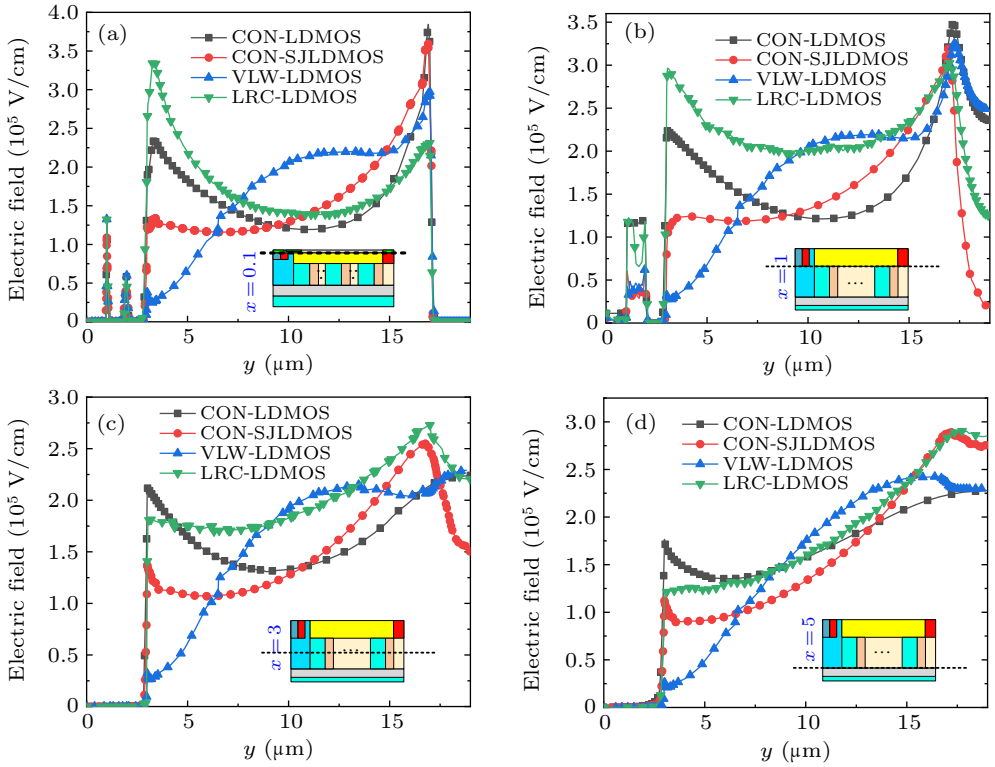


Fig. 4. The surface, bulk, and bottom electric field distributions along the lateral direction for the CON-LDMOS, CON-SJLDMOS, VLW-LDMOS, and the LRC-LDMOS: (a) surface, $x = 0.1$ μm; (b) bulk, $x = 1.0$ μm; (c) bulk, $x = 3.0$ μm; (d) bottom, $x = 5.0$ μm.

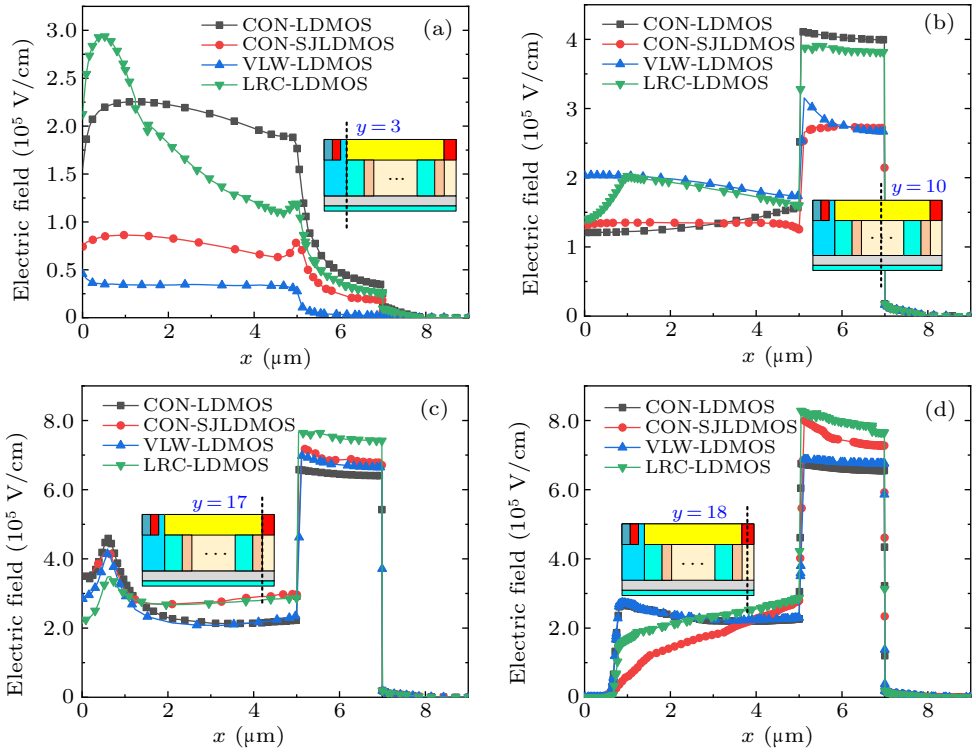


Fig. 5. The electric field distributions along the vertical direction for the CON-LDMOS, CON-SJLDMOS, VLW-LDMOS, and the LRC-LDMOS at the cutline: (a) $y = 3$ μm, (b) $y = 10$ μm, (c) $y = 17$ μm, (d) $y = 18$ μm.

Figure 5 shows the the electric field distribution along the vertical direction of the devices. At the cutline $y = 3$μm as shown in Fig. 5(a), the maximum E_{peak} is improved from 2.2×10^5 V/cm for CON-LDMOS to 2.9×10^5 V/cm for LRC-LDMOS. At the cutline $y = 10$ μm as shown in Fig. 5(b), the E_{peak} in the drift region increased from 1.2×10^5 V/cm for CON-LDMOS, 1.3×10^5 V/cm for CON-SJLDMOS, and 2.0×10^5 V/cm for LRC-LDMOS to 2.0×10^5 V/cm for VLW-LDMOS. At the cutline $y = 17$ μm as shown in Fig. 5(c), the E_{peak} in the N-drift region of LRC-LDMOS is smaller than

that of the other three devices. The electric field distribution at $y = 18$ μm is shown in Fig. 5(d), it can be seen that the electric field at the drain of LRC-LDMOS is smaller than that of CON-LDMOS and VLW-LDMOS, and larger than that of CON-SJLDMOS.

3.2. Specific on resistance $R_{on,sp}$

Figure 6(a) shows the current voltage characteristics of the LDMOSs at forward conduction state. The source and the P-substrate are shorted to the ground, the gate electrode V_g is set at 10 V. The currents are increased linearly with the drain voltage for the devices, and the current of the LRC-LDMOS is significantly larger than the CON-LDMOS and VLW-LDMOS due to the LRC structure, which is basically equal to that of CON-SJLDMOS. Figure 6(b) shows the transfer characteristic curves of the devices, the threshold voltage V_{th} are almost 4.8 V.

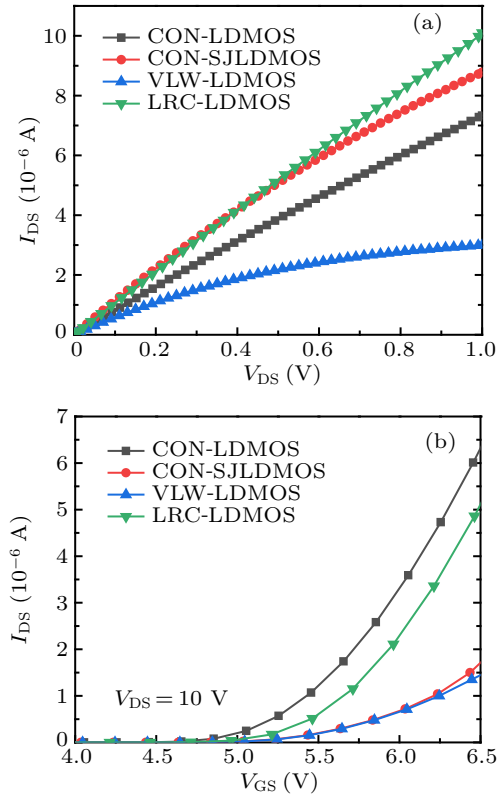


Fig. 6. The *I*–*V* curve of the four LDMOSs: (a) forward conduction characteristic curve and (b) transfer characteristic curve.

Figure 7 shows the corresponding specific on resistance $R_{on,sp}$ of the LDMOSs at forward conduction state, it can be seen that the $R_{on,sp}$ of the LRC-LDMOS is much lower than the CON-LDMOS and VLW-LDMOS, which is basically equal to that of CON-SJLDMOS.

Figures 8 and 9 show the electron current density diagrams of the four devices. Combining with Figs. 8 and 9, it can be seen that the electron current density of the CON-LDMOS is obviously lower than that of the other three structures, but there is electron current in the drift region of the CON-LDMOS. It can be seen from Figs. 8 and 9 that there is little difference in electron current density among CON-SJLDMOS, VLW-LDMOS, and LRC-LDMOS, but their conductive regions are different.

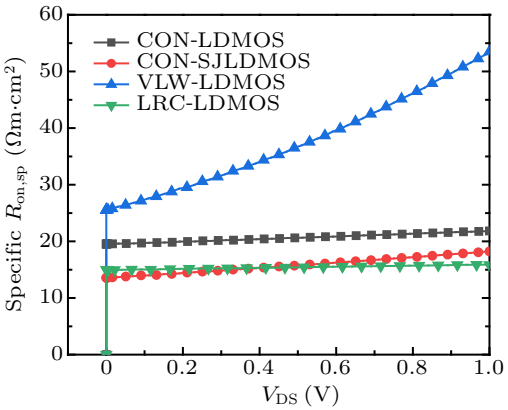


Fig. 7. The specific on resistance $R_{on,sp}$ of the LDMOSs.

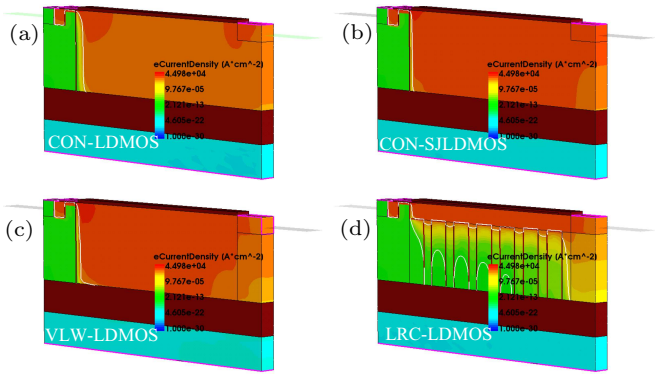


Fig. 8. Electron current density ($V_{GS} = 10$ V, $V_{DS} = 1$ V), (a) CON-LDMOS, (b) CON-SJLDMOS, (c) VLW-LDMOS, (d) LRC-LDMOS.

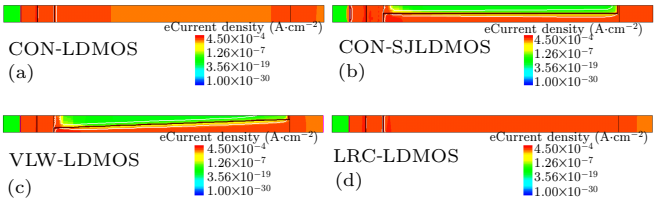


Fig. 9. Cross section of electron current density ($V_{GS} = 10$ V, $V_{DS} = 1$ V), (a) CON-LDMOS, (b) CON-SJLDMOS, (c) VLW-LDMOS, (d) LRC-LDMOS.

3.3. Key parameters influence on *BV* and $R_{on,sp}$

Figure 10 shows the effect of the thickness T_c and doping concentration N_c of the low resistance electron channel on the *BV* and $R_{on,sp}$. In Figs. 10(a) and 10(b), the $R_{on,sp}$ is decreased linearly with the increase of T_c and N_c due to the conduction capability of the LRC being enhanced. However, the *BV* is increased linearly and then decreased with the increase of T_c and N_c, it reaches the maximum value $BV = 253$ V when $T_c = 1.0$ μm and $N_c = 1.0 \times 10^{16}$ cm^{-3}. It is because the LRC should be completely depleted by the P-pillar, at the same time the charge compensation is satisfied between the N-pillar, LRC and P-pillar.

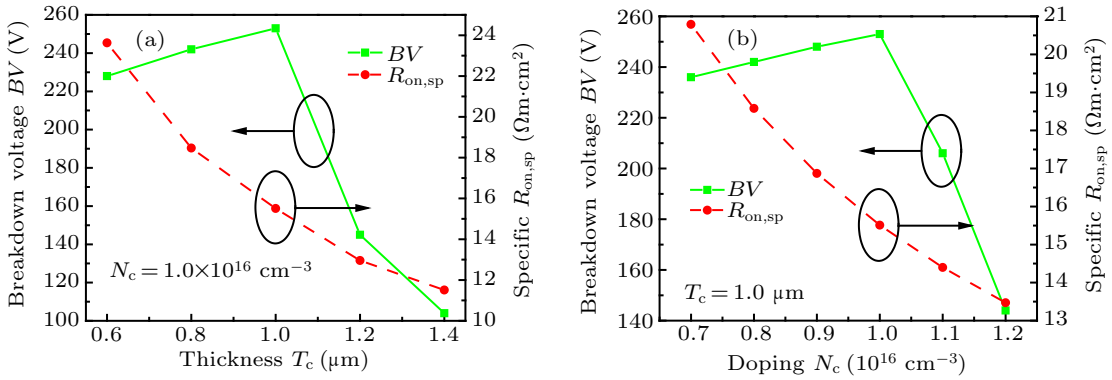


Fig. 10. The BV and $R_{on,sp}$ are functions of the low resistance electron channel for the LRC-LDOMS: (a) the thickness T_c of the low resistance electron channel and (b) the doping N_c of the low resistance electron channel.

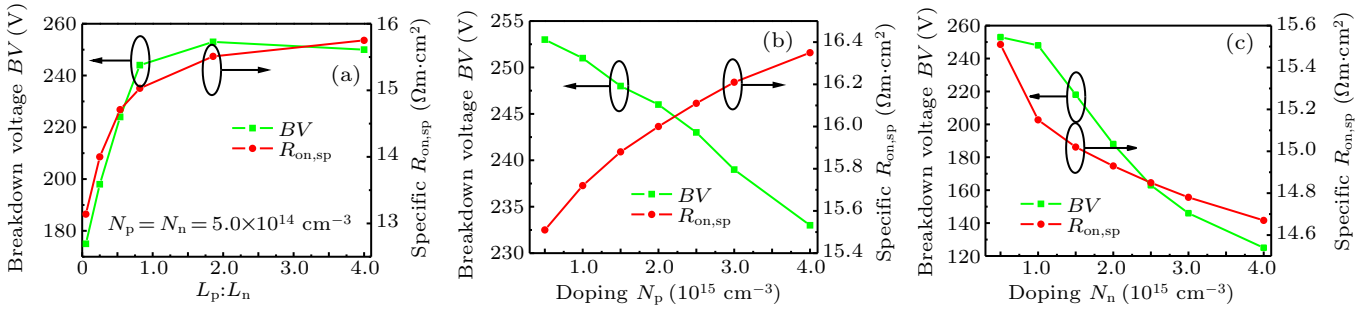


Fig. 11. The BV and $R_{on,sp}$ are functions of the N-pillar and P-pillar for the LRC-LDOMS (a) the length ratio $L_p : L_n$ of the SJ, (b) the doping N_p of the P-pillar, (c) the doping N_n of the N-pillar.

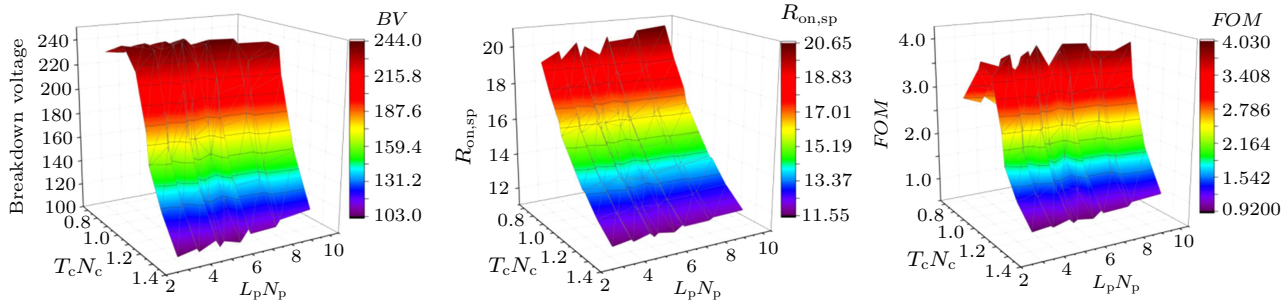


Fig. 12. Effect of doping concentration and thickness of LRC and P-pillar on device performance: (a) breakdown voltage, (b) specific $R_{on,sp}$, and (c) FOM.

Figure 11 shows the influence of the width ratio and doping concentration of the SJ on BV and $R_{on,sp}$. The SJ under the LRC is divided into 7 sections. In Fig. 11(a), the $R_{on,sp}$ is increased rapidly with the increase of L_p:L_n, and then it reaches almost saturation at L_p:$L_n = 1.85$. The BV is optimized to a maximum value by adjusting the width ratio $L_p : L_n = 1.85$ to satisfy the charge balance. Figure 11(b) shows that the $R_{on,sp}$ is increased gradually with the increase of N_p of the P-pillar, and it is decreased gradually with the increase of N_n of the N-pillar as shown in Fig. 11(c). However, the BV reaches its maximum value when the N_p and N_n of super-junction concentration are 5.0×10^{14} cm^{-3}.

Figure 12 shows the breakdown voltage, $R_{on,sp}$ and FOM of the device when various parameters of LRC-LDMOS change.

3.4. Baliga's figure of merit

Figure 13 shows the ideal silicon limit of the RESURF LDMOS given in Ref. [22] and the $R_{on,sp}$ *versus* the BV relationship of the LRC-LDMOS. It is apparent that the performance of the proposed LDMOS breaks through the silicon limit. The Table 1 shows the main performance parameters of LDMOS with the experimental and simulated data reported previously in Refs. [9,16,18]. The FOM (Baliga's figure of merit) is defined as $BV^2/R_{on,sp}$ to describe the trade-off performance of the devices. It can be seen that the FOM is 4.1 MW/cm^2 with the BV of 253 V and $R_{on,sp}$ of 15.5 mΩ·cm^2 for the LRC-LDMOS, compared the CON-LDMOS with 0.28 MW/cm^2 and the CON-SJLDMOS with 2.38 MW/cm^2, the FOM is improved almost 146.4% and 172%, respectively. In addition, compared with VLW-LDMOS and CBSLOP-LDMOS, the FOM of LRC-LDMOS has increased by 131%

and 138%, respectively.

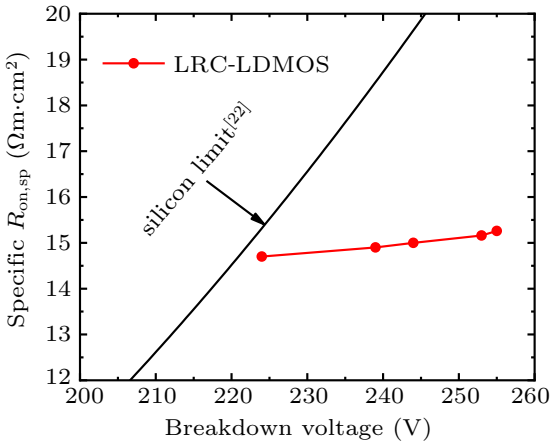


Fig. 13. Specific $R_{on,sp}$ *versus BV* relationship for the LDMOS device with the experimental and simulated data reported previously.

Table 1. *BV*, $R_{on,sp}$, and *FOM* of the proposed devices.

Devices	*BV* (V)	$R_{on,sp}$ (mΩ·cm^2)	*FOM* (MW/cm^2)	Ref.
CON-LDMOS	270	252	0.28	[16]
CON-SJLDMOS	169	12	2.38	[18]
CBSLOP-LDMOS	300	31	2.9	[9]
VLW-LDMOS	618	125	3.05	[16]
LRC-LDMOS	253	15.5	4.1	this work

4. Conclusion and perspectives

A novel LRC-LDMOS with low resistance channel based on the SJ structure is proposed. The LRC is highly doped to provide an electron current channel at the forward conduction state, which significantly decreases the specific $R_{on,sp}$. The surface and bulk electric fields are modulated by adjusting the charge compensation between the LRC, N-pillar, and P-pillar, which obviously increases the *BV*. Finally the tradeoff performance of the LRC-LDMOS breaks through the ideal silicon limit with superior *FOM*.

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