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Extended-source broken gate tunnel FET for improving direct current and analog/radio-frequency performance*

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The various advantages of extended-source (ES), broken gate (BG), and hetero-gate-dielectric (HGD) technology are blended together for the proposed tunnel field-effect transistor (ESBG TFET) in order to enhance the direct-current and analog/radio-frequency performance. The source of the ESBG TFET is extended into channel for the purpose of increasing the point and line tunneling in the device at the tunneling junction, and then, the on-state current for the ESBG TFET increases. The influence of the source region length on the direct-current and radio-frequency performance parameters of the ESBG TFET is analyzed in detail. The results show that the proposed TFET exhibits a high on-state current to off-state current ratio of 10^{13}, large transconductance of 1200 μS/μm, high cut-off frequency of 72.8 GHz, and high gain bandwidth product of 14.3 GHz. Apart from these parameters, the ESBG TFET also demonstrates high linearity distortion parameters in terms of the second- and third-order voltage intercept points, the third-order input interception point, and the third-order intermodulation distortion. Therefore, the ESBG TFET greatly promotes the application potential of conventional TFETs.

Keywords: extended-source, broken gate, radio-frequency performances, tunnel field-effect transistor

PACS: 85.30.Mn, 81.05.Ea, 85.30.Tv **DOI:** 10.1088/1674-1056/abe372

1. Introduction

As the size of metal-oxide-semiconductor field-effect transistors (MOSFETs) scales down continuously, the power dissipation, limitation of subthreshold swing (SS) of 60 mV/decade of current at room temperature, and significant increase of the off-state current I_{off} have become critical issues. However, in next-generation technology nodes, novel devices with low power, high on-chip packing density, and high speed are of great demands. Therefore, tunnel field-effect transistors (TFETs) have been proposed to replace conventional MOSFETs in order to overcome the shortcomings of MOSFETs. In contrast to the thermal injection of carriers for MOSFETs, the working mechanism of TFETs is band-to-band tunneling (BTBT).[1] The BTBT mechanism can reduce the values of SS, various researches have proved that SS is lower than 60 mV/decade at 300 K.[2–4] Moreover, the BTBT mechanism produces a large tunneling barrier for the current carriers when the device is operated in the off-state, which makes I_{off} smaller. As a result, the power dissipation of TFETs is lower than that of MOSFETs. However, in spite of the above-mentioned advantages for TFETs, conventional TFETs suffer from ambipolar behavior and small on-state current I_{on}. Therefore, many papers have extensively boosted I_{on} and reduced ambipolar behavior. For the purpose of suppressing ambipolar behavior, many technologies have been used, such as low doping levels in the drain region,[5] underlap and overlap of gate-drain.[6–8] Furthermore, in order to enhance I_{on}, many novel architectures of TFETs such as T-shape,[9,10] nanowire,[11,12] L-shape,[2,13] U-shape,[14] nanotube,[15,16] are proposed. Moreover, the materials with small energy bandgap,[17–19] high-k gate dielectrics,[20] high doping levels in the source region as well as abruptness at the source-channel tunnel junction are need to design. As is well known, the tunneling barrier decreases with the energy bandgap decreasing, so the tunneling rate increases, which results in a large I_{on}. Moreover, a sharp abrupt junction between the source region and channel region should be formed in order to increase the generation efficiency of BTBT as much as possible, and as a result, I_{on} is boosted. Thus, many researchers have concentrated on how to form an abrupt source-channel junction based on the process technology.

Furthermore, for better applications from the perspective of low-power and analog/rf circuits, the performance parameters of TFETs such as low SS, small threshold voltage V_{th}, high on-state current to off-state current ratio I_{on}/I_{off}, large transconductance g_m, high cut-off frequency f_T, high gain bandwidth product (GBP), and large transconductance frequency product (TFP) should be obtained. Miscellaneous techniques have been reported in the literature to improve the dc and analog/rf performance parameters.[21–28] Puja *et al.* reported a ferroelectric TFET with SS of 40 mV/decade, I_{on}/I_{off} of 8.4×10^{11}.[29] Tripuresh *et al.* reported an extended-source double-gate TFET (ESDG TFET) with V_{th} of 0.42 V, SS of 12.24 mV/decade, I_{on}/I_{off} of 10^{12}, f_T of 37.7 GHz, GBP of 3.4 GHz.[30] Rounak *et al.* proposed a broken gate TFET

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(BG TEFT), which combines the advantages of the double gate TFET (DG TFET) and the L-shaped TFET (L TFET).[31] Moreover, superior characteristics such as small ambipolar current, low SS, and large I_{on} are achieved for BG TFET. In this paper, a novel TFET named as the ESBG TFET, which is an amalgamation between the ESDG TFET and the BG TFET in order to enhance the dc and analog/rf performance.

2. Device structure

The structure of the ESBG TFET is shown in Fig. 1. The source region is extended into the channel for the purpose of enhancing the point and line tunneling probabilities at the tunneling junction. The gate dielectrics near the source region and near the drain region are hafnium dioxide (HfO_2) and silicon dioxide (SiO_2) in order to reduce ambipolarity. It should be noted that the device is called the ESBG TFET (HfO_2) when the gate dielectrics near the source and drain regions are HfO_2. Similarly, when the gate dielectrics are silicon dioxide (SiO_2), the device is called the ESBG TFET (SiO_2). The length and height of the p^+ source region is L_s and T_s, respectively. The silicon thicknesses near the gate and near the drain are T_1 and T_2, respectively. The lengths of gate and gate 2 are L_1 and L_3, respectively. The distance between gate and gate 2 is L_2. The parameters for the ESBG TFET are listed in Table 1.

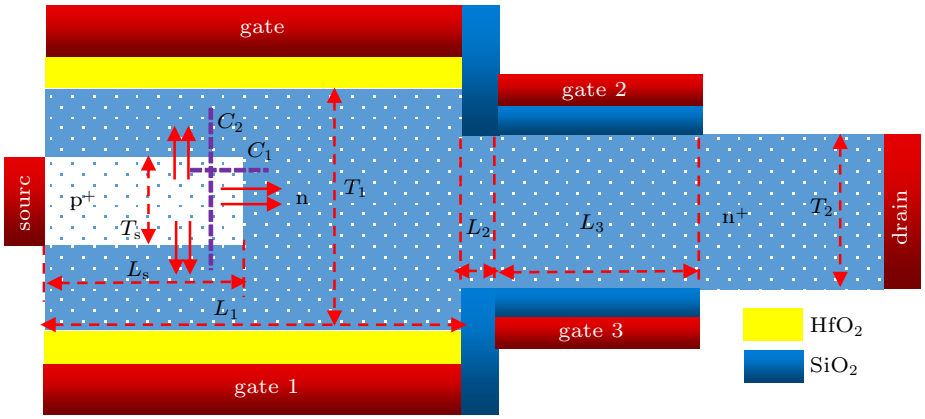


Fig. 1. Structure of the extended-source broken gate TFET.

Table 1. Parameters of the ESBG TFET used in this paper.

Device parameters	Value
Silicon thicknesses near the gate (T_1)	16 nm
Silicon thicknesses near the drain (T_2)	10 nm
Height of the p^+ source region (T_s)	6 nm
Gate length (L_1)	45 nm
Gate-2 length (L_3)	43 nm
Distance between gate and gate 2 (L_2)	2 nm
Gate (gate 1) work function	4.0 eV
Gate 2 (gate 3) work function	4.7 eV
Gate oxide thickness	2 nm
Source doping concentration	10^{20} cm^{-3}
Drain doping concentration	10^{19} cm^{-3}
Channel doping concentration	10^{17} cm^{-3}

The performance parameters of the ESBG TFET are simulated using the silvaco atlas simulator,[32] and the nonlocal band-to-band tunneling (BTBT) model, the auger recombination model, the shockley-read-hall (SRH) model as well as the fermi-dirac statistics model are used. The material parameters such as tunneling mass of electron (me.tunnel) and tunneling mass of hole (mh.tunnel) are used in the nonlocal tunneling model. Moreover, the tunneling current of the TFET is exponentially related to the values of me.tunnel and mh.tunnel. In our simulations, the values of me.tunnel and mh.tunnel are set as 0.21 and 0.16 for the purpose of calibrating the simulation models with the experimental results.[30,32] It should be noted that the gates for the ESBG TFET are simultaneously provided with the same gate-source voltage for all the simulations and analysis presented in this paper.

3. Results and discussions

3.1. Direct-current analysis for the ESBG TFET

Figure 2(a) shows the comparisons of transfer characteristics for the conventional dual material gate (DMG) TFET and the ESBG TFET with an L_s of 25 nm. It is evident from Fig. 2(a) that the ESBG TFET shows an improvement in the I_{off} by seven orders in comparison to the DMG TFET. Moreover, I_{on} is also enhanced for the ESBG TFET due to increase of the line and point tunneling probabilities at the source-channel junction. I_{on} and I_{off} defined at gate-source voltage of V_{gs} fixed at 1 V and 0 V, respectively, have been calculated with the drain-source voltage of V_{ds} fixed at 0.5 V. $I_{on} \sim 3.26 \times 10^{-5}$ A/μm and $I_{off} \sim 1.84 \times 10^{-18}$ A/μm have been obtained for the ESBG TFET with an L_s of 25 nm. Moreover, the transfer characteristic curves of the proposed device and the ESBG TFET (HfO_2) are almost coincided, but I_{off} of the proposed device is less than that of the ESBG TFET (HfO_2). However, I_{on} for the ESBG TFET (SiO_2) is very small because of the large tunneling width. Figure 2(b) shows the

variation of I_{ds} with V_{ds} for the DMG TFET and the ESBG TFET. The curves depicts that with increase in V_{ds}, I_{ds} saturates to a constant value as the barrier width becomes independent of V_{ds}. Moreover, the ESBG TFET exhibits superior drain current in comparison with the other three devices.

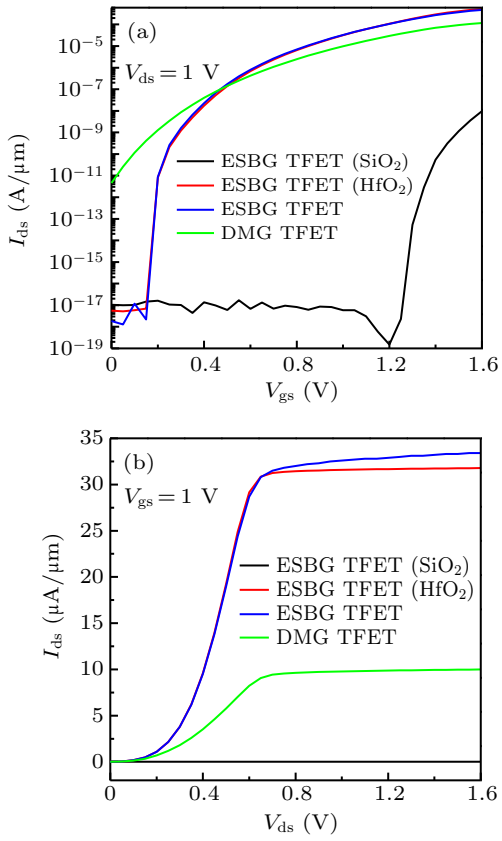


Fig. 2. (a) Transfer characteristics and (b) output characteristics comparison for the ESBG TFET and the DMG TFET.

Figure 3(a) shows the variation in the electric field along the cutline C_1 (as shown in Fig. 1). The peak electric field is lied at the corners due to the point tunneling in the device. The variation in the electric field is reflected in the energy band along the cutline C_1, as observed in Fig. 4(a). It is obvious that the value of energy band range over which tunneling takes place and the value of the average tunneling width varies with L_s, the higher the value of energy band range over which tunneling takes place, the lower the value of the average tunneling width, the higher the charge carrier transmission probability, and hence I_{on} is enhanced. Moreover, it is obvious from Fig. 3(b) that the peak electric field at the source corners along the cutline C_2 (as shown in Fig. 1) is higher, which infers the line tunneling in the ESBG TFET. Figure 4(b) shows the variation in the energy band at the source corners along the cutline C_2. More energy band bending at the source corners along the cutline C_2 will result in a higher I_{on}. However, the differences of electric field and energy band along the cutline C_2 between $L_s = 15$ nm and $L_s = 25$ nm are not obvious.

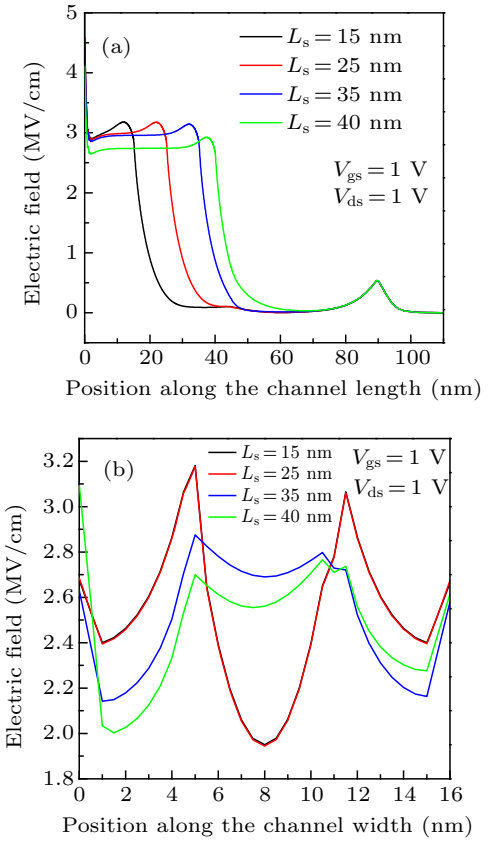


Fig. 3. Electric field variation along the cutline (a) C_1 and (b) C_2 for the ESBG TFET with different L_s.

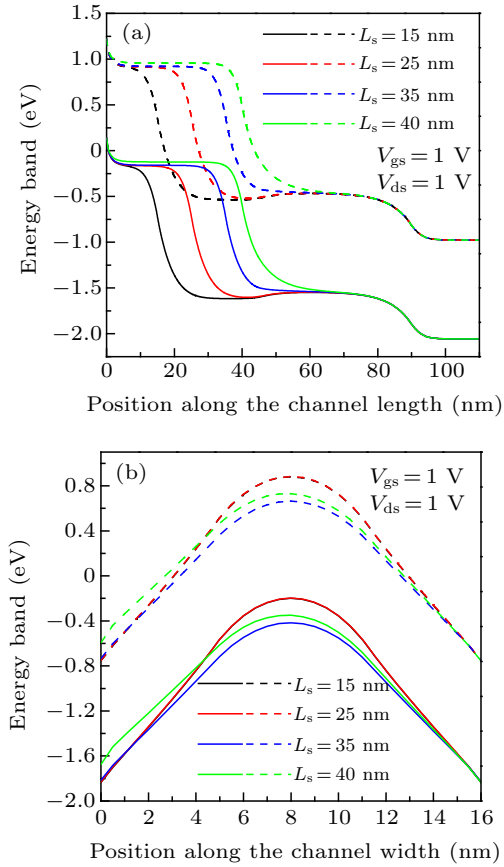


Fig. 4. Energy band variation along the cutline (a) C_1 and (b) C_2 for the ESBG TFET with different L_s.

Figure 5(a) shows the effects of L_s on I_{on} and I_{on}/I_{off} for the ESBG TFET. The I_{on} increases with increase in L_s when the value of L_s is lower than 35 nm, but I_{on} degrades after L_s of 35 nm. Moreover, the I_{on}/I_{off} degrades rapidly when L_s is larger than 15 nm due to the increase in I_{off}. Therefore, in terms of enhanced I_{on} and I_{on}/I_{off}, the optimum value of L_s is set to 25 nm for the ESBG TFET. Figure 5(b) shows the output characteristics for the ESBG TFET with four values of L_s. The ESBG TFET with L_s of 35 nm exhibits improved drain current in comparison with other three L_s values.

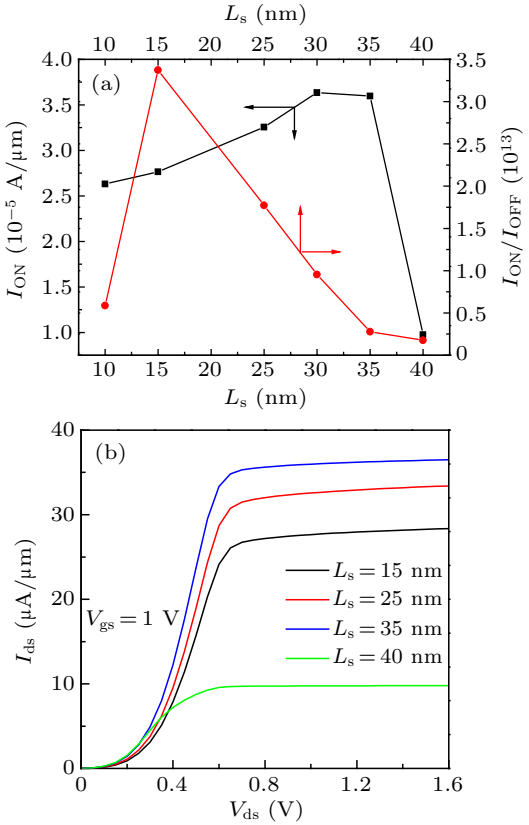


Fig. 5. (a) I_{on}, I_{on}/I_{off} and (b) output characteristics for the ESBG TFET with different L_s.

3.2. Parasitic capacitance and radio-frequency performance for the ESBG TFET

Parasitic capacitances impact the performances of TFET significantly at high frequency since they establish a feedback path between output and input, which leads to parasitic oscillations as well as signal distortion. These parasitic capacitances contain gate-to-source capacitance C_{gs}, gate-to-drain capacitance C_{gd}. The dependences of C_{gs}, C_{gd}, and transconductance (g_m) on V_{gs} for the ESBG TFET with different L_s are illustrated in Fig. 6. It is obvious that for the ESBG TFET with $L_s = 15$ nm, C_{gs} is lower than C_{gd} when V_{gs} is larger than 0.3 V. C_{gd} increases rapidly due to the fact that a large number of electrons are accumulated in the channel at the gate interface, while C_{gs} remains almost unaffected with rise in V_{gs}. The gate capacitance C_{gg} is the sum of C_{gs} and C_{gd}. Therefore, the main component of the gate capacitance C_{gg} is C_{gd}. However, because of the increase of the overlap between the gate and the source regions for the ESBG TFET with $L_s = 35$ nm, C_{gs} is larger than C_{gd} when V_{gs} is less than 1.3 V. Therefore, C_{gg} is mainly determined by C_{gs} for most of the V_{gs} range at larger L_s. However, C_{gd} is also the main component of C_{gg} when V_{gs} is larger than 1.3 V, which is due to the fact that the increase of the electron concentration in the channel leads to C_{gd} increasing rapidly with V_{gs}. However, the values of C_{gs} and C_{gd} are very large for the ESBG TFET with $L_s = 40$ nm when V_{gs} is larger than 1.3 V, which will deteriorate the high-frequency characteristics of TFET. Also, g_m is an important parameter for analogue applications of the TFET which converts the gate-source voltage into the drain-source current. It is obvious from Fig. 6(c) that g_m for the ESBG TFET with $L_s = 35$ nm is larger than that of the ESBG TFET with $L_s = 15$ nm, 25 nm and 40 nm. The higher the g_m of the ESBG TFET, the better the sensitivity for the conversion of gate-source voltage into drain-source current, the better the linearity and high-frequency characteristics.

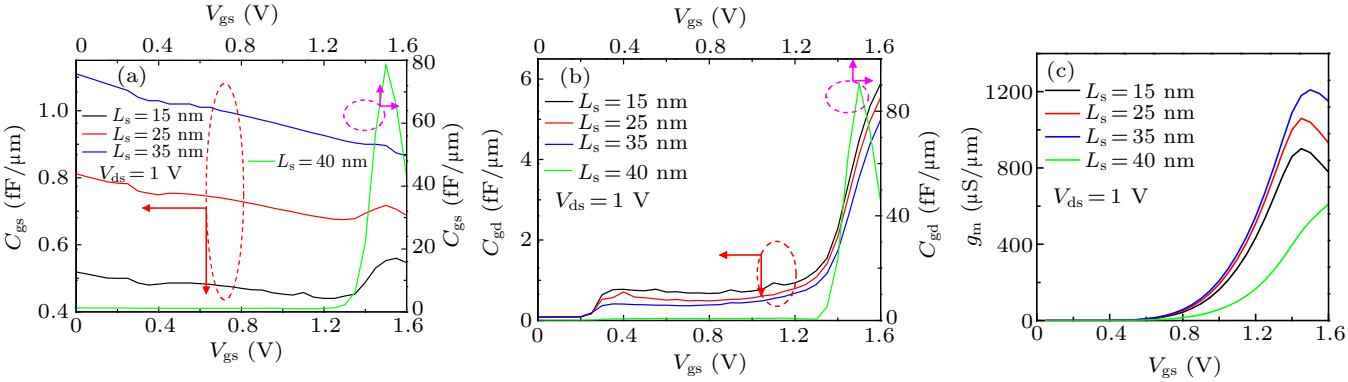


Fig. 6. (a) C_{gs}, (b) C_{gd}, and g_m for the ESBG TFET with different L_s.

A comparison of the ESBG TFET with different L_s has been made, concerning cut-off frequency (f_T), gain bandwidth product (GBP), and transconductance frequency product (TFP). Here, f_T and GBP are expressed as $g_m/\left[2\pi\left(C_{gd}+C_{gs}\right)\right]$ and $g_m/\left(2\pi\times10\times C_{gd}\right)$, respectively. It is obvious that f_t and GBP of the proposed device with three

L_s reach a peak value, since the change in g_m is predominant over the minor change in $(C_{gd}+C_{gs})$ and C_{gd}. However, the limitation of g_m and the increase of the parasitic gate capacitance lead to the reduction of f_T and GBP as V_{gs} increases. Moreover, the proposed device with L_s fixed at 35 nm obtains a maximum f_T of 72.8 GHz. TFP represents a trade-off between bandwidth and power, which is defined as $g_{m*}f_t/I_{ds}$. Similarly, TFP also increases before inversion region for the ESBG TFET with different L_s and after attaining a maximum value, it starts decreasing for higher V_{gs}.

The performance parameters of the ESBG TFET about I_{on}/I_{off}, g_m, f_T and GBP as compared with those of the recently reported TFET structures are given in Table 2. The proposed structure provides higher I_{on}/I_{off}, and larger g_m than those of other reported TFET structures. Moreover, the ESBG TFET offers two times improvement in f_T and four times increase in GBP as compared to the recently reported ESDG TFET.

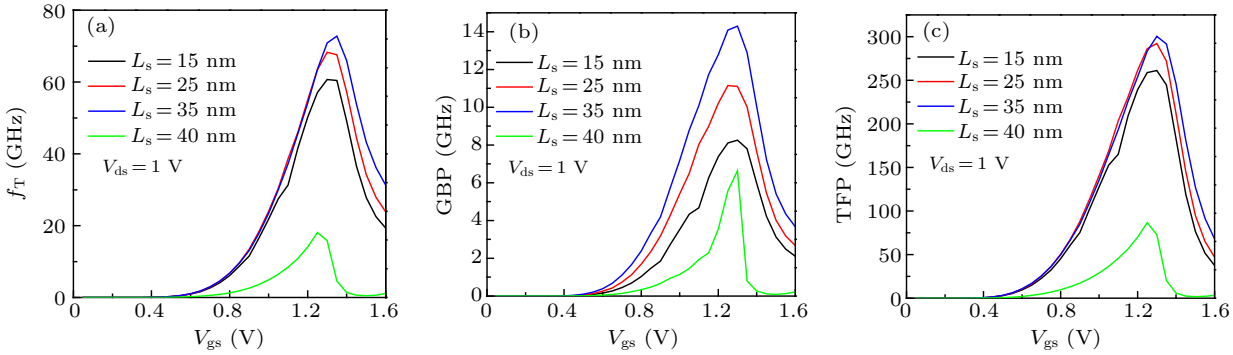


Fig. 7. Characteristics of (a) f_T, (b) GBP, and TFP for the ESBG TFET with different L_s.

Table 2. Comparison of performance parameters of the ESBG TFET with the recently reported TFETs.

Performance parameters	I_{on}/I_{off}	the maximum value of g_m (μS/μm)	the maximum value of f_T (GHz)	the maximum value of GBP (GHz)
TG TFET[33]	$\sim 10^{10}$	232	11.9	2.3
V-TFET-WNP[34]	6.87×10^{11}	54	13	1.6
V-TFET-WP[34]	7.5×10^{11}	66	46	7
L TFET[35]	9.5×10^{10}	7	0.7	0.4
HGDG TFET[36]	$\sim 10^{10}$	4.4	5	1.8
ESDG TFET[30]	$\sim 10^{12}$	238	37.7	3.4
ESBG TFET with Ls fixed at 35 nm	2.8×10^{12}	1200	72.8	14.3

The variation of the second and third-order voltage intercept points (V_{IP2}, V_{IP3}), the third-order input interception point (I_{IP3}), and the third-order intermodulation distortion (I_{MD3}) with V_{gs} for the proposed device with different L_s are analyzed. The equations of these parameters can be written as follows:

$$V_{IP2} = 4\times g_{m1}/g_{m2}, \tag{1}$$

$$V_{IP3} = \sqrt{24\times g_{m1}/g_{m3}}, \tag{2}$$

$$I_{IP3} = 2/3\times g_{m1}/\left(g_{m3}\times R_S\right), \tag{3}$$

$$I_{MD3} = \left(4.5\times\left(V_{IP3}\right)^3\times g_{m3}\right)^2\times R_S. \tag{4}$$

The transconductance and its coefficients (i.e., higher-order harmonics of transconductance) are evaluated as $g_{mn} = 1/n!\times\frac{\partial^n I_{ds}}{\partial V_{gs}^n}$, and R_S is usually set as 50 Ω. It is needed that larger values of V_{IP2}, V_{IP3}, and I_{IP3} as well as a lower value of I_{MD3} are obtained for the purpose of higher linearity performance and lower distortion operation. From Fig. 8(a), it is observed that the proposed device with L_s fixed at 25 nm shows an enhancement in V_{IP2}. The peak of V_{IP3} for the proposed device reflects the cancelation of the internal feedback around the second-order nonlinearity and the third-order nonlinearity coefficient. From Fig. 8(b), it can be seen that the ESBG TFET with L_s fixed at 25 nm obtains a peak at low V_{gs} and exhibits considerable enhancement in the V_{IP3} peak. I_{IP3} is another important parameter for the determination of linearity. When V_{gs} is lower than 1.3 V, the ESBG TFET with L_s fixed at 25 nm has a better I_{IP3} as compared to the device with the others L_s thus making the proposed device more reliable, as shown in Fig. 8(c). I_{MD3} as shown in Fig. 8(d) is called the third-order intermodulation distortion at which the first- and third-order harmonic powers are equal. When L_s is increased from 15 nm to 35 nm, I_{MD3} is almost unaffected by L_s.

The second- and third-order harmonic distortions (HD_2, HD_3) are analyzed in order to understand the distortion characteristics of the device, and the equations about HD_2 and HD_3 can be written as

$$HD_2 = \frac{1}{2}\times V_a\times\frac{\partial g_{m1}}{\partial V_{gs}}\left(2\times g_{m1}\right)^{-1}, \tag{5}$$

$$HD_3 = \frac{1}{4}\times V_a^2\times\frac{\partial^2 g_{m1}}{\partial V_{gs}^2}\left(6\times g_{m1}\right)^{-1}, \tag{6}$$

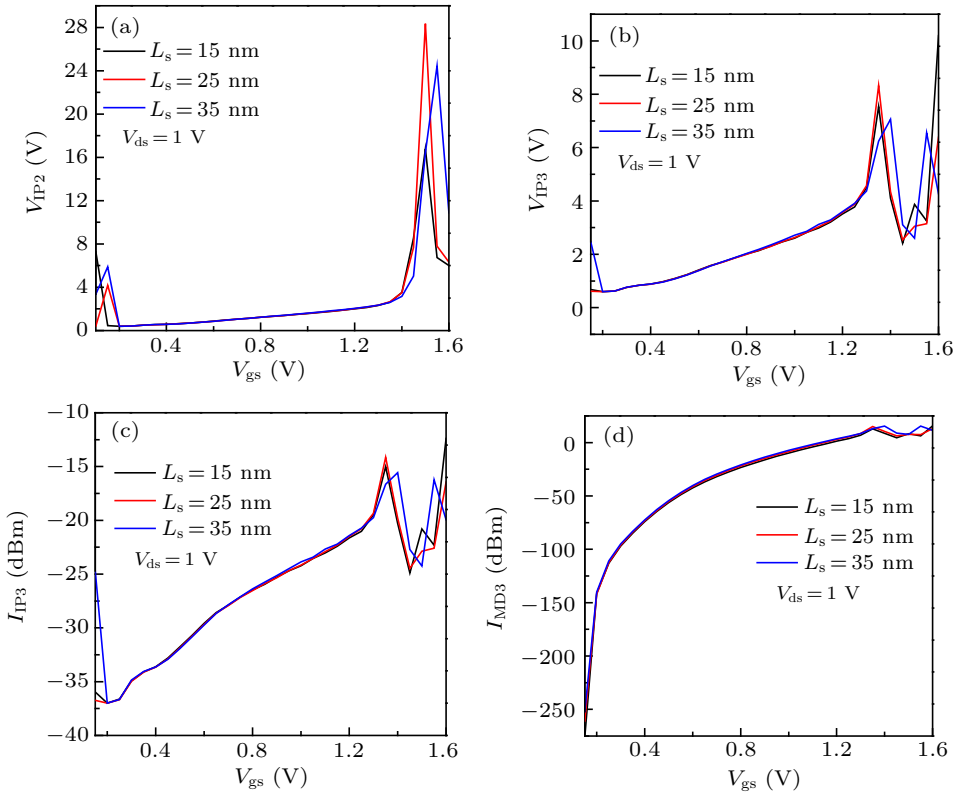


Fig. 8. (a) V_{IP2}, (b) V_{IP3}, (c) I_{IP3}, and (d) I_{MD3} for the ESBG TFET with different L_s.

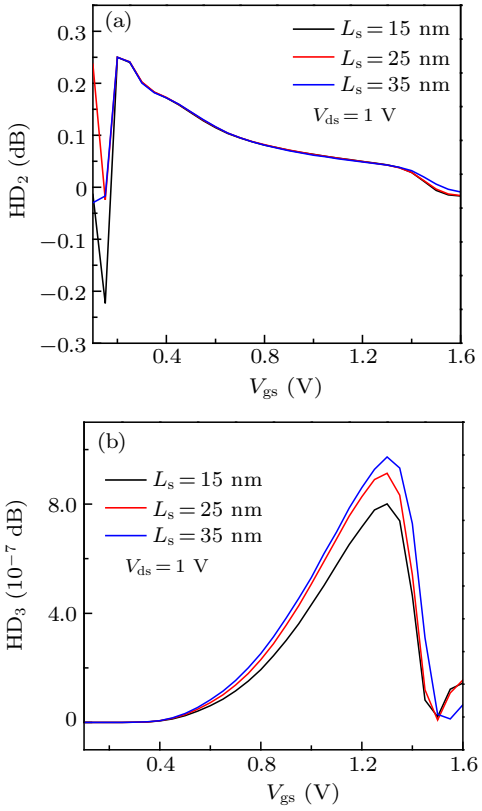


Fig. 9. (a) HD_2 and (b) HD_3 for the ESBG TFET with different L_s.

where V_a is the amplitude of the input signal, which is fixed at 50 mV. It is obvious that the proposed device with L_s fixed at 15 nm provides less HD_2 and HD_3 than the device with the other length of L_s. Therefore, the noise in the proposed device with L_s fixed at 15 nm will be less. Consequently, it can be concluded that the proposed device with L_s fixed at 15 nm is more linear with higher reliability.

4. Conclusions

The dc characteristics, analog/rf parameters and linearity parameters for ESBG TFET are analyzed. The results shows that the ESBG TFET can achieve significant improvement in parameters like I_{on}/I_{off}, g_m, f_T, GBP, and TFP. The length of the source region for ESBG TFET is optimized to increase the point and line tunneling at the tunneling junction. It can be concluded that the optimum value of L_s is set to 25 nm in terms of enhanced I_{on} and I_{on}/I_{off} of 10^{13}. However, the parameters such as g_m, f_T, GBP, and TFP are slightly enhanced when L_s is set to 35 nm. Moreover, the ESBG TFET offers two times improvement in f_T and four times increase in GBP as compared to the recently reported ESDG TFET, thus the ESBG TFET shows better analog/rf characteristics. Furthermore, the linearity distortion parameters in terms of V_{IP2}, V_{IP3}, I_{IP3}, I_{MD3}, HD_2, and HD_3 for the ESBG TFET with different L_s are analyzed in order to address the nonlinearity issue.

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