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Realization of simultaneous balanced multi-outputs for multi-protocols QKD decoding based on silica-based planar lightwave circuit*

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Silica-based planar lightwave circuit (PLC) devices can reduce transmission loss and cost in a quantum key distribution (QKD) system, and have potential applications in integration and production. A PLC-based quantum decoding integrated chip for multi-protocols is designed and fabricated, which is composed of variable optical splitters (VOSs), asymmetric Mach–Zehnder interferometers (AMZIs), and variable directional couplers (VDCs). Balanced pulse-pairs of four outputs are obtained simultaneously with measured delay times of 405 ps and 402 ps, respectively. The chip has advantages in achieving high interference visibility and low quantum bit error rate (QBER).

Keywords: quantum key distribution (QKD), planar lightwave circuit (PLC), multi-protocols, decoder

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1. Introduction

Quantum communication is one of rapidly developing fields in quantum technologies, and it has potential applications in innovating telecommucations. Since it can solve security problems in principle, quantum communication is regarded as an effective means to counter quantum computer. Quantum key distribution (QKD) is the basis of quantum communication which is most widely used and studied in depth.[1–3] The first protocol, which was put forward by Bennett and Brassard as early as 1984, is protocol-BB84.[4] With the development of research and the change of demand, more protocols have been proposed like differential phase-shift (DPS), coherent one-way (COW).[5–8]

In the past, QKD quantum communication systems were mostly composed of discrete bulk optical devices, which was generally unstable and had high losses which limited the effective transmission distance severely.[9–12] In recent years, researchers have designed different stable, compact and robust platforms to implement optical quantum information integrated devices.[13–16] The mainstream integrated QKD material platforms include SOI, InP, SiO_xN_y, and silica.[17] For quantum decoding integrated chips, platforms based on silica and SiO_xN_y planar lightwave circuit (PLC) have been demonstrated, and can achieve a high density integration.[18–20] For silica PLC, it has the advantages of low-loss, low-cost, stability, mature fabrication processing, and compatibility with micro-electronics.

Although QKD has advanced from simple proof-of-principle experiments toward robust long-term demonstrations, it has not been used on a large scale.[21] One key problem is the compatibility of multi-protocols.

In this paper, we design a decoding chip based on silica-based PLC platform with 2.0% refractive index difference which can be compatible with different quantum protocols. Because the devices based on silica have low thermo-optic effect modulation rate, passive decoding mode is chosen on decoder. Meanwhile, this mode can exclude the influence caused by optical phase modulators and clock synchronization in receiver. In this chip, we use one variable optical splitter (VOS) to choose different protocols, two other VOSs to compensate for the different loss caused by asymmetric Mach–Zehnder interferometer (AMZI). Decoding chips need to output the balanced pulse-pairs at the same time to fit for different protocols, therefore four variable directional couplers (VDCs) are designed to adjust output splitting ratio to make balanced outputs. This chip can eliminate the interference of fabrication error effectively, and reduce the cost and loss in the actual application of QKD.

2. Design and analysis

The QKD multi-protocols decoding integrated chip is fabricated based on silica PLC platform with a 2.0% refractive index difference, whose structure diagram is shown in Fig. 1. The core refractive index and cladding layers of the waveg-

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uide are 1.4745 and 1.4447, respectively, and its cross section is 4 μm×4 μm. The chip is composed of three VOSs, two AMZIs, each of which contains a thermo-optic phase modulator (TOPM) and a 400-ps delay line (DL), and four VDCs, each of which contains a directional coupler (DC) and heating electrodes.

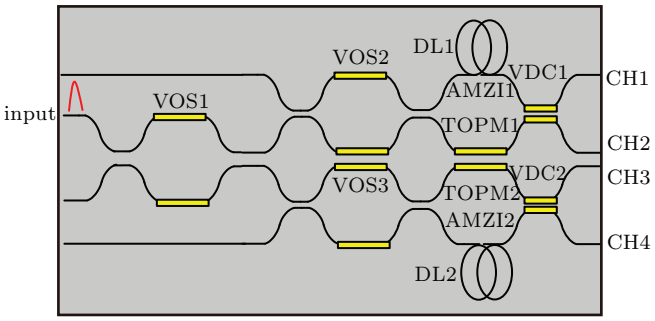


Fig. 1. Structure diagram of the decoding chip.

According to the different QKD protocols, the unit on chip will be configured differently.

(i) BB84–phase

Quantum states are prepared in encoder, the same power carrying double pulses of which the delay time is 400-ps transfers into this chip through optical fiber. When passing through VOS1, light pulses are divided into VOS2 and VOS3 respectively. Then pulses are divided into AMZI1 and AMZI2 which has the same delay time as encoder. Different voltages are added onto TOPM1 and TOPM2, and different basis (X and Y) are held. Interference happens when pulses are transferred through AMZI1 and AMZI2. Pulses are outputted from CH1 to CH4. The interfered pulse is shown to be an increased state or a decreased state and transferred into single photon detector which corresponds to a different quantum state.

(ii) BB84-time bin

Two bases (Y and Z) are prepared in encoder, the same power carrying double pulses of which the delay time is 400 ps transfers into this chip through optical fiber. Encoder needs to inform the decoder of the the message of choosing basis via classic channel. For Y basis, light pulses are guided into VOS2 through VOS1. In VOS2, pulses are divided into AMZI1 which has the same delay time as encoder. Appropriate voltages are added onto TOPM1, and Y basis is held. Pulses are outputted from CH1 to CH2. The interfered pulse are shown to be increased or decreased state and transferred into single photon detector which is corresponding to different quantum states. For Z basis, light pulses are guided into VOS3 through VOS1. In VOS3, pulses are divided into AMZI2 which has the same delay time as encoder. Appropriate voltages are added onto TOPM2, and Z basis is held. Pulses are outputted from CH3 to CH4. The interfered pulses are detected by single photon detector, which is correspond to different quantum states.

(iii) Differential-phase-shift

Quantum states are prepared in encoder, the same power carrying double pulses of which the delay time is 400 ps transfers into this chip through optical fiber. When passing through VOS1, light pulses are divided into VOS2. In VOS2, pulses are divided into AMZI1 which has the same delay time as encoder. Interfered pulses are outputted from CH1 to CH2, which correspond to different quantum states.

(iv) Coherent-one-way

Quantum states are prepared in encoder, same power carried double pulses which delay time is 400 ps transfers into this chip through optical fiber. When passing through VOS1, light pulses are divided into VOS2 (large part) and VOS3 (small part). In VOS2, pulses are divided into short arm of AMZI1, and pulses are guided into single photon detector from CH1 or CH2. The first pulse of a period represents different quantum states. For the decoy period, the ends of detector are random and can be abandoned. In VOS3, pulses are divided into AMZI2 which has the same delay time as encoder. Different voltages are added to TOPM2 to adjust phase difference between pulses. When two adjacent pulses whose intensities are not zero pass through VDC2, interference can be happened and outputted from CH3 or CH4, detected by single photon detector. Ideally, the same detector can respond to all interferences. However, when the messages are eavesdropped, another detector can respond to the interference.

2.1. VOS

The structure diagram of VOS is shown in Fig. 2, it is an AMZI, which is composed of two directional couplers (DC) and a couple of symmetric arms, which are covered by heating electrodes.

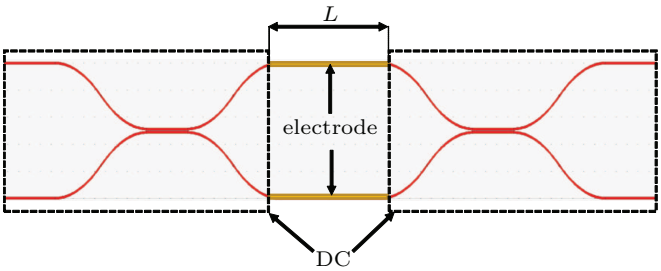


Fig. 2. Structure diagram of VOS.

The VOS has two functions in this chip, one is to choose different protocols, and the other is to compensate for different losses caused by DL1 and DL2. Because the two arms of adjoined AMZI have different lengths, the loss of the pulse in the long arm will be larger than in the short arm, which will make the pulse-pairs unbalanced. These two functions are both based on thermo-optic effect, through adjusting the voltage between electrodes, the difference in refractive index difference between the two arms of VOS is changed. Therefore, the spectral ratio in outputs can be changed to achieve these two functions.

The structure diagram of DC is shown in Fig. 3, where larm represents the length of the coupling zone and gap refers to the distance between the coupling waveguides. The distance between input waveguides is 100 μm, which is the same as that between output waveguides, and their bending radii are both 10000 μm. To analyze coupling condition and tolerance, the dependence of two outputs' powers on gap and larm are simulated by beam propagation method (BPM), respectively, as shown in Figs. 4 and 5. The 50/50 splitting ratio of DC can be realized while larm is 370 μm and gap is 2 μm, and the tolerance of gap is smaller than that of larm.

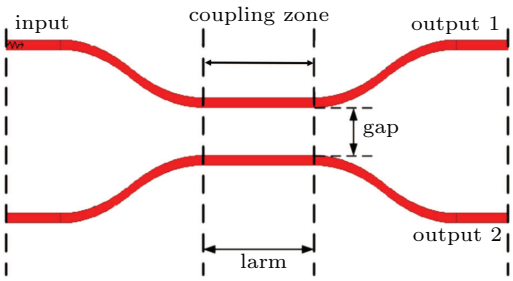


Fig. 3. Structure diagram of DC.

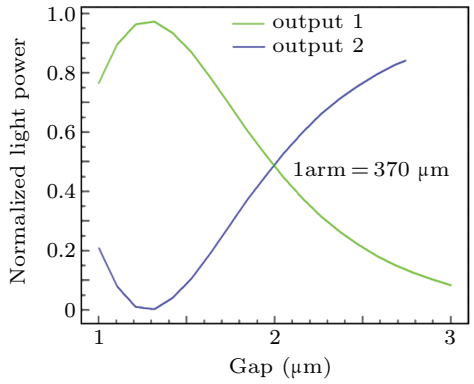


Fig. 4. Simulation of gap width to split ratio.

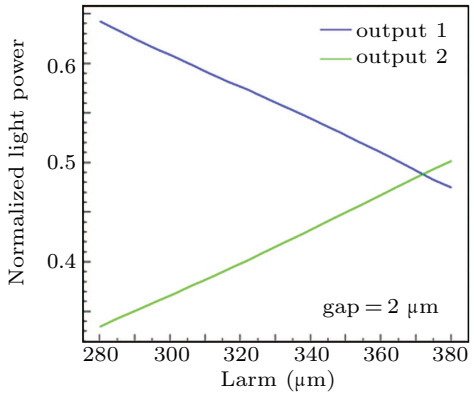


Fig. 5. Simulation of larm length to split ratio.

Using the parameters from simulation of DC, MZI can be designed. The length of modulated arm L is designed to be 2000 μm with considering the chip size. Heating electrodes made of titanium-tungsten alloy are sputtered on modulated arm which works when the light splitting is modulated.

2.2. AMZI

In the QKD decoding chip, AMZI is used to produce pulse-pairs to decode quantum messages. The structure diagram of AMZI is shown in Fig. 1, which consists of a TOPM and a DL. The TOPM is used to modulate the pulse phase based on thermo-optic effect through electrodes, and DL is used to produce pulse-pairs with 400-ps delay time. The structure diagram of DL is shown in Fig. 6, where r represents the minimum curvature radius which is set to be 2500 μm. The optical path difference between the two arms of AMZI is represented by Δl and can be determined to be 81.38 mm from the following equation:

$$\Delta l = v \cdot \Delta t = \frac{c \cdot \Delta t}{n}, \tag{1}$$

where v represents the speed of light in the core cladding layer, c is represented speed of light in vacuum which is 3×10^8 m/s, and n is the index of core cladding layer which is 1.4745.

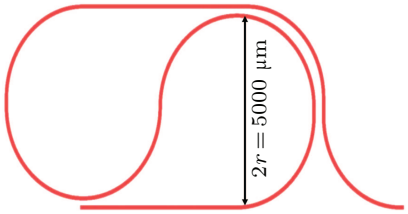


Fig. 6. Designed DL in AMZI.

2.3. VDC

Although the simulation has shown the suitable length of coupling zone, however, in practical situation it is hard to use only VOS to make all outputs balanced. Because the fabrication error will cause the drift of pulses' phase difference in two arms of DC. So in the end part of each output, a VDC is designed to compensate for the phase difference. It consists of a DC electrode and a heating electrode, which are added in the coupling zone of DC.

The structure diagram of VDC is shown in Fig. 7. In the simulation of DC, larm which represents length of coupling zone is set to be 370 μm, as long as the heating electrode, and gap which is the distance between the coupling waveguides is set to be 2 μm. The VDCs can adjust the splitting ratio by thermo-optic effect, and the effectiveness of this design is verified by simulation shown in Fig. 8.

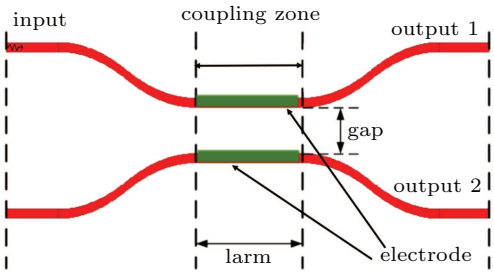


Fig. 7. Structure diagram of VDC.

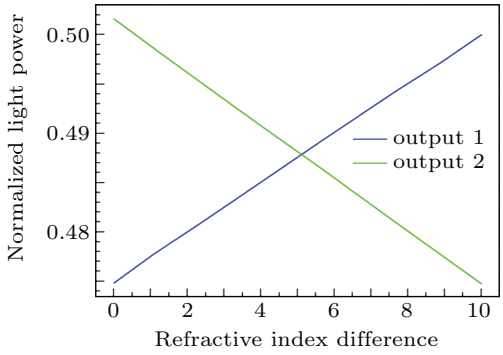


Fig. 8. Simulation of refractive index difference to split ratio.

Figure 8 shows that in the range of refractive index difference of 0.001, 3-dB insertion loss can be adjusted, which means two channels' outputs can be balanced.

3. Fabrication and package

The fabrication process of QKD decoding chip based on silica PLC technology is described below. Firstly, 6-inch (1 inch = 2.54 cm) Si wafer is washed and dried. Next, 20-μm-thick SiO_2 lower cladding layer is grown by thermal oxidation in 1050 °C. Then, 4-μm-thick GeO_2-SiO_2 core layer is deposited by plasma enhanced chemical vapor deposition (PECVD), and 1-μm-thick poly-Si hard mask layer is grown by low pressure chemical vapor deposition (LPCVD). Next, the SiO_2 waveguides are formed by photolithography and inductively coupled plasma (ICP) etching, and a 20-μm-thick boro-phospho-silicate glass (BPSG) upper cladding layer is deposited by PECVD. Then, Ti–W heating electrodes are constructed through photolithography, magnetron sputtering and lift-off, and Ti–Pt–Au leading electrodes were constructed through photolithography, evaporating and lift-off in sequence. Finally, the wafer is sliced, and the waveguide end faces of the chip are polished. The photograph of the fabricated chip is shown in Fig. 9(a), with chip size being 30 mm×12 mm.

The packaging process includes coupling, bonding, drying, and connecting. The chip is located on the optical worktable, and single mode fibers (SMF) are used to align and couple with the input waveguide and output waveguide. Then, the chip is fixed on a printed circuit board (PCB). Finally, the PCB is pasted in the packing box, and electrodes and pins are connected by gold threads. The photograph of the packaged chip is shown in Fig. 9(b).

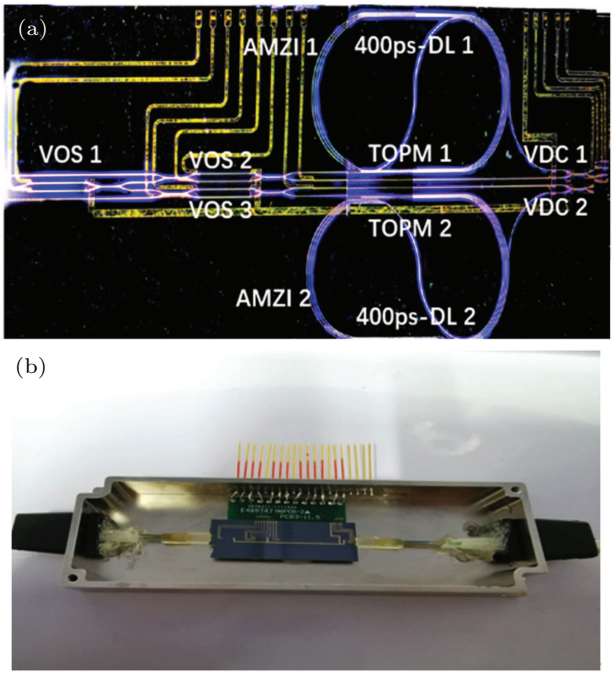


Fig. 9. (a) Illustration of fabricated chip circuit and (b) photograph of packaged chip.

4. Measurement and discussion

4.1. Classical light test

The schematic diagram of classical optics transmission measurement system is shown in Fig. 10. Excess loss of the chip lowers to 3.5 dB, which shows the characteristics of low loss in silica-material-made decoder. The pulsed laser can produce 1550-nm-wavelength pulsed light, with the pulse width being 50 ps, pulse peak 25 mW, and frequency 50 MHz. The DC voltage source can offer different voltages to VOS and VDC, to adjust pulse-pairs. The high-speed oscilloscope is connected to the outputs of the chip to display the waveforms.

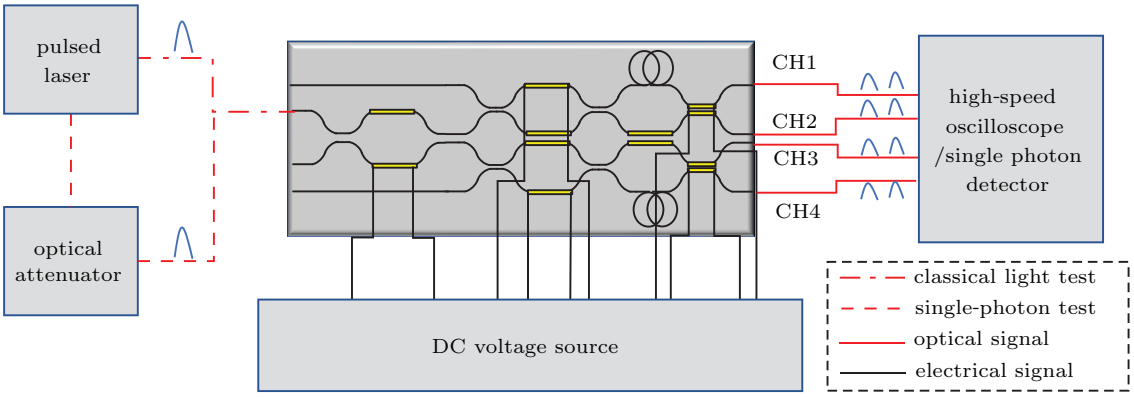


Fig. 10. Schematic diagram of the measurement system.

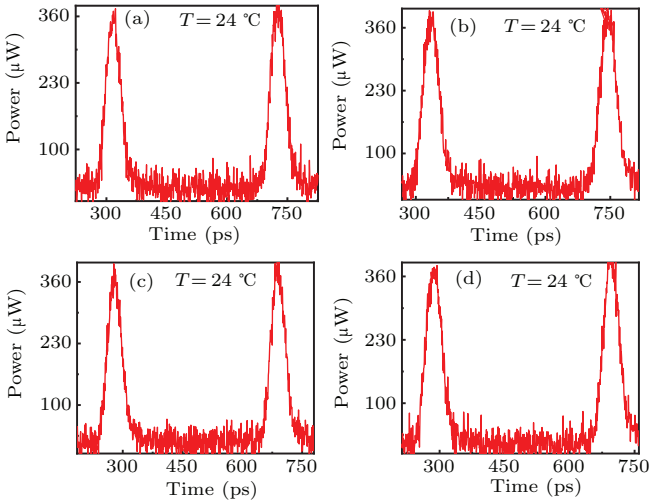


Fig. 11. Four outputs of chip in classical light test for (a) CH1, (b) CH2, (c) CH3, (d) CH4.

The oscilloscope outputs of the chip in the classical optics transmission measurement at room temperature are shown in Fig. 11.

When the voltages on the VOS1, VOS2, VOS3, VDC1 and VDC2 set to be 1 V, 5.70 V, 5.85 V, 1.52 V, and 1 V respectively, the balanced pulse-pairs of quadruple channels with the measured delay times of 405 ps and 402 ps respectively are obtained, which are nearly the same as the designed delay times. The little differences are caused by fabrication error.

4.2. Single-photon test

The schematic diagram of single photon transmission measurement system is shown in Fig. 10. The pulsed laser can produce 1550-nm-wavelength pulsed light, whose pulse width is 50 ps, pulse peak is 25 mW, and frequency is 50 MHz. The optical attenuator can make the pulsed light attenuated by 75 dB. The DC voltage source can offer different voltages on VOS and VDC, to adjust the pulse pairs. Two single photon detectors are connected to the outputs of the chip to count photons.

Firstly, the function of VDC is tested. When VDC1 and VDC2 are added to by 0-V voltage, as shown by the black line in Fig. 12, pulse peaks in CH1 and CH4 have the lowest counts of photon, while in CH2 and CH3 have the highest counts. By the time when the added voltage is 2.5 V, the results turn out to be the opposite, pulse peaks in CH1 and CH4 have become the highest, while in CH2 and CH3 decrease to the lowest values.

In order to further study the splitratio adjustment function of VDC, voltage step is set to be 0.1 V. Scanning the voltage on VDC from 0 V to 2.5 V, photon counts of pulses are changed as shown in Fig. 13.

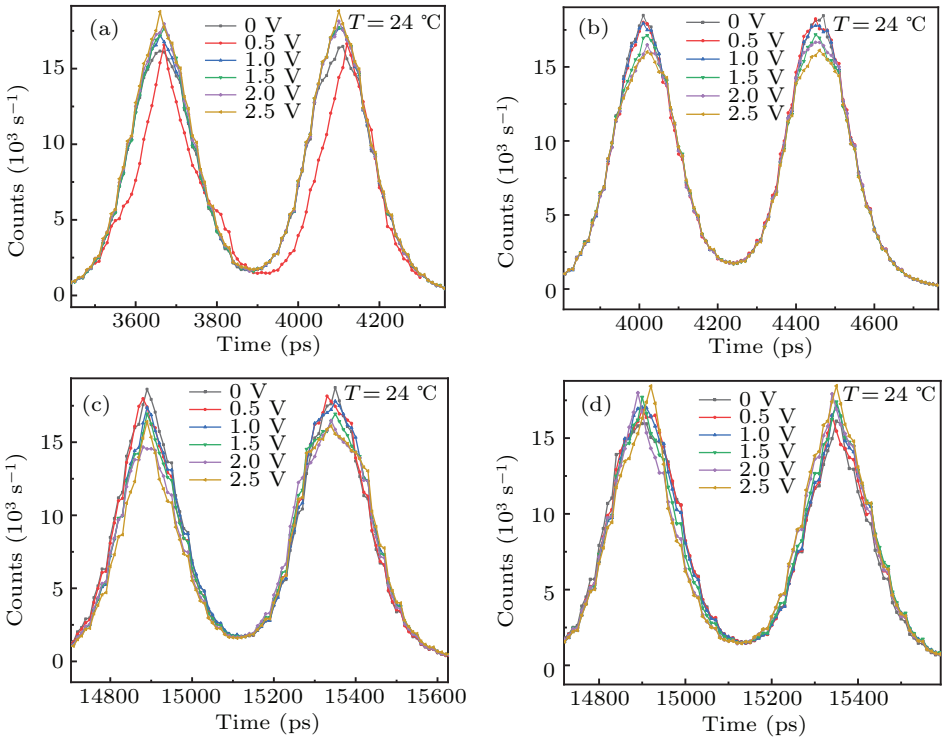


Fig. 12. Photon counts varying with time at different DC voltages in (a) CH1, (b) CH2, (c) CH3, and (d) CH4.

The propagation formula of DC can be described in Eq. (2), where P_{o1} and P_{o2} represent light powers of two outputs in VDC, and P_i denotes the input light power of VDC, k the mode coupling coefficient, and z the propagation distance, in this chip, it is set to be the same as the length of coupling zone.

$$P_{o1}(z) = P_i \cos^2(kz), \tag{2}$$

$$P_{o2}(z) = P_i \sin^2(kz). \tag{3}$$

Sine-squared function and least-squares method are used to fit the data as solid line shown in Fig. 13. The experimental results and theoretical analysis have high-quality fit. This indicates that the VDC has a function to compensate for the phase difference caused by fabrication error. From the results, 1.0 V for VDC1 and 1.1 V for VDC2 can be found in the next test.

The outputs of the chip in the single photon transmission measurement at room temperature is shown in Fig. 14. When the voltages on VOS1, VOS2, VOS3, VDC1, and VDC2 are set to be 1 V, 5.7 V, 5.85 V, 1 V, and 1.1 V, four channels of the chip can achieve the same photon count level simultaneously, which is about 17000. The little difference is caused by environmental interference. Meanwhile, the measured delay times of balanced pulse-pairs of double channels are 405 ps and 402 ps, respectively, which are the same as the classical results.

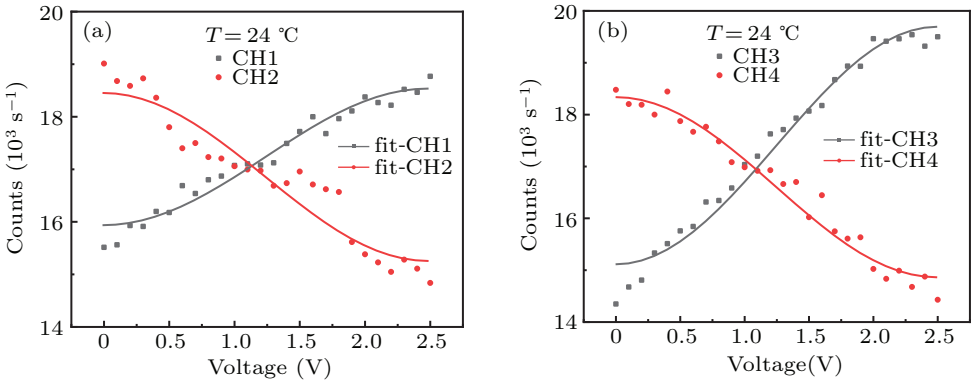


Fig. 13. Peak pulse photon counts varying with voltage in (a) CH1 and CH2, (b) CH3 and CH4.

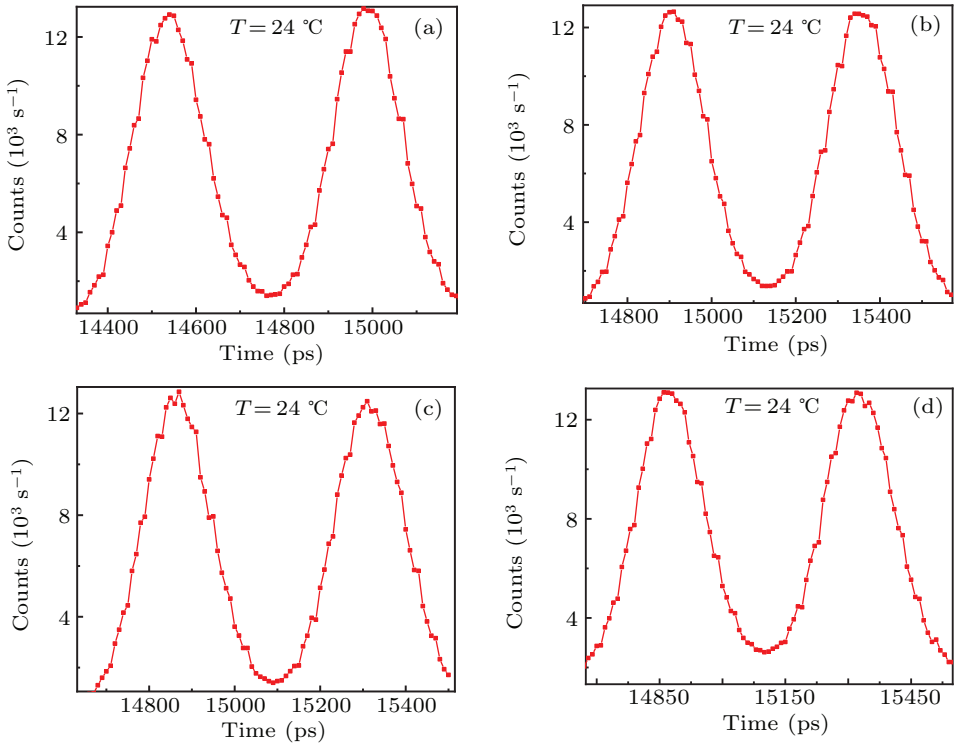


Fig. 14. Four balanced outputs of chip of single photon test in (a) CH1, (b) CH2, (c) CH3, and (d) CH4.

5. Conclusions

In this paper, we design and fabricate a new type of multi-protocol quantum decoding integrated chip based on a silica PLC platform which is compatible with BB84 phase, BB84 timebin, DPS, and COW protocols. It consists of VOS, VDC and 400ps-AMZI. When the appropriate voltage is added to the VOS1, different protocols can be selected. The VOS2 and VOS3 can compensate for the different losses caused by the different light distances between AMZI1 and AMZI2. In a single photon test, voltages on the VOS1, VOS2, VOS3, VDC1, and VDC2 are set to be 1 V, 5.70 V, 5.85 V, 1 V and 1.1 V to make the four channels' peak pulse photon counts identical simultaneously. On the basis of this, the balanced pulse-pairs with measured delay times of 402 ps and 405 ps are generated by AMZI1 and AMZI2 respectively. The chip has advantageous in achieving high interference visibilities and low

quantum bits error rate.

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