

Trigger mechanism of PDSOI NMOS devices for ESD protection operating under elevated temperatures

Jia-Xin Wang(王加鑫), Xiao-Jing Li(李晓静), Fa-Zhan Zhao(赵发展), Chuan-Bin Zeng(曾传滨), Duo-Li Li(李多力), Lin-Chun Gao(高林春), Jiang-Jiang Li(李江江), Bo Li(李博), Zheng-Sheng Han(韩郑生), and Jia-Jun Luo(罗家俊)
Citation: Chin. Phys. B, 2021, 30 (**7**): 078501. DOI: 10.1088/1674-1056/abe2fe
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Design and investigation of novel ultra-high-voltage junction field-effect transistor embedded with NPN

Xi-Kun Feng(冯希昆), Xiao-Feng Gu(顾晓峰), Qin-Ling Ma(马琴玲), Yan-Ni Yang(杨燕妮), and Hai-Lian Liang(梁海莲)
Chin. Phys. B, 2021, 30 (**7**): 078502. DOI: 10.1088/1674-1056/abe2fb

Trigger mechanism of PDSOI NMOS devices for ESD protection operating under elevated temperatures

Jia-Xin Wang(王加鑫), Xiao-Jing Li(李晓静), Fa-Zhan Zhao(赵发展), Chuan-Bin Zeng(曾传滨), Duo-Li Li(李多力), Lin-Chun Gao(高林春), Jiang-Jiang Li(李江江), Bo Li(李博), Zheng-Sheng Han(韩郑生), and Jia-Jun Luo(罗家俊)
Chin. Phys. B, 2021, 30 (**7**): 078501. DOI: 10.1088/1674-1056/abe2fe

New DDSCR structure with high holding voltage for robust ESD applications

Zi-Jie Zhou(周子杰), Xiang-Liang Jin(金湘亮), Yang Wang(汪洋), and Peng Dong(董鹏)
Chin. Phys. B, 2021, 30 (**3**): 038501. DOI: 10.1088/1674-1056/abd38f

Enhanced gated-diode-triggered silicon-controlled rectifier for robust electrostatic discharge (ESD) protection applications

Wenqiang Song(宋文强), Fei Hou(侯飞), Feibo Du(杜飞波), Zhiwei Liu(刘志伟), Juin J. Liou(刘俊杰)
Chin. Phys. B, 2020, 29 (**9**): 098502. DOI: 10.1088/1674-1056/ab9de6

Design of a novel high holding voltage LVTSCR with embedded clamping diode

Ling Zhu(朱玲), Hai-Lian Liang(梁海莲), Xiao-Feng Gu(顾晓峰), Jie Xu(许杰)
Chin. Phys. B, 2020, 29 (**6**): 068503. DOI: 10.1088/1674-1056/ab836e

---

Trigger mechanism of PDSOI NMOS devices for ESD protection operating under elevated temperatures*

Jia-Xin Wang(王加鑫)[1,2,3], Xiao-Jing Li(李晓静)[1,2,†], Fa-Zhan Zhao(赵发展)[1,2,‡], Chuan-Bin Zeng(曾传滨)[1,2], Duo-Li Li(李多力)[1,2], Lin-Chun Gao(高林春)[1,2], Jiang-Jiang Li(李江江)[1,2], Bo Li(李博)[1,2], Zheng-Sheng Han(韩郑生)[1,2,3], and Jia-Jun Luo(罗家俊)[1,2]

[1] *Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*
[2] *Key Laboratory of Science and Technology on Silicon Devices, Chinese Academy of Sciences, Beijing* 100029, *China*
[3] *University of Chinese Academy of Sciences, Beijing* 100029, *China*

(Received 9 November 2020; revised manuscript received 4 January 2021; accepted manuscript online 4 February 2021)

Trigger characteristics of electrostatic discharge (ESD) protecting devices operating under various ambient temperatures ranging from 30 °C to 195 °C are investigated. The studied ESD protecting devices are the H-gate NMOS transistors fabricated with a 0.18-μm partially depleted silicon-on-insulator (PDSOI) technology. The measurements are conducted by using a transmission line pulse (TLP) test system. The different temperature-dependent trigger characteristics of grounded-gate (GGNMOS) mode and the gate-triggered (GTNMOS) mode are analyzed in detail. The underlying physical mechanisms related to the effect of temperature on the first breakdown voltage V_{T1} are investigated through the assist of technology computer-aided design (TCAD) simulation.

Keywords: ESD, trigger voltage, temperature, GGNMOS, GTNMOS, TCAD

PACS: 85.30.De, 41.20.Cv, 85.30.Mn **DOI:** 10.1088/1674-1056/abe2fe

1. Introduction

Electrostatic discharge (ESD) has been a threat to reliability in the semiconductor industry for decades. Novel ESD protecting devices are frequently designed to mitigate such concerns.[1–4] Meanwhile, high temperature is a typical environment for integrated circuits.[5,6] The assembly and operation of integrated circuits in some cases take place at elevated temperatures. Hence, The ESD protecting designs become more complicated due to the thermally-induced variations of ESD parameters, and it is necessary to systematically and comprehensively analyze the characteristics of ESD protecting devices to ensure that they are suitable for operating under elevated temperatures. Koo *et al.*[7] reported the features of the high holding voltage of the new silicon controlled rectifier (SCR) ESD protecting device at different temperatures and improved the stability in a temperature range of 25 °C–225 °C and made a detailed analysis. Meneghesso *et al.*[8] introduced a new type of SCR, the low-voltage-trigger SCR ESD protecting structure, and obtained a high holding voltage, and performed two-dimensional (2D) device simulation (DESSIS Synopsys) to obtain the temperature dependence of the holding voltage at 25 °C–125 °C. Liang *et al.*[9] introduced the temperature dependence of the critical parameters of a variety of typical SCR and diode structures at a temperature of 225 °C. Li *et al.*[10] introduced the temperature dependence of diode and GGNMOS (grounded-gate NMOS) in a temperature range from −40 °C to 110 °C. Jang and Lin[11] and Jang *et al.*[12] analyzed the temperature-dependent steady and dynamic state characteristics of SCR-based ESD protecting circuits, focusing on the triggering and holding behavior of ESD protecting devices. Hou *et al.*[13] improved a thermal-stable diode-triggered silicon-controlled rectifier (TSDTSCR) device to obtain almost constant high-temperature ESD protecting capabilities. Do *et al.*[14] developed the floating technology to reduce the trigger voltage of 4H–SiC GGNMOS to cater to the design window and carried out high-temperature evaluation. Arbess and Bafleur[15] looked into a new type of MOS insulated gate bipolar transistor (MOS-IGBT) power clamping device for high-temperature operation. It had a lower temperature sensitivity at 200 °C. However, in most of those studies considered are only the changes in the characteristics of the traditional or novel ESD protecting devices with temperature to verify their reliability within their operating temperature range, but the relation of temperature to triggering, or holding, or failure characteristics are not analyzed by the underlying physical mechanism and simulation.

In this paper, the temperature-dependent triggering characteristics of partially depleted silicon-on-insulator (PDSOI) NMOS devices for ESD protection are analyzed. The transmission line pulsing (TLP) *I*–*V* curves are measured, and the

*Project supported by the National Natural Science Foundation of China (Grant No. 61804168).
†Corresponding author. E-mail: lixiaojing1@ime.ac.cn
‡Corresponding author. E-mail: zhaofazhan@ime.ac.cn
© 2021 Chinese Physical Society and IOP Publishing Ltd

first breakdown voltage (V_{T1}) is studied and discussed. The technology computer aided design (TCAD) simulation is carried out to obtain a physical insight into the mechanism of the temperature dependence of the triggering behavior.

2. Experiment

The device under test (DUT) was an H-gate NMOS device and fabricated with a 0.18-μm PDSOI technology. More parameters are summarized in Table 1. The measurements were targeted to the human body model (HBM) and conducted using the TLP/VFTLP (transmission line pulse/very fast transmission line pulse) test system HOXI-I with a pulse width of 100 ns and a rise time of 5 ns, which is made in the Institute of Microelectronics of the Chinese Academy of Sciences. The heating module provided a testing temperature range from 30 °C to 200 °C. We characterized the TLP *I*–*V* curves of the two operating modes, the grounded-gate NMOS (GGNMOS) mode and the gate-triggered NMOS (GTNMOS) mode, under varying temperatures. The GGNMOS mode describes an NMOS-based ESD protecting device whose gate, source, body, and substrate electrode were connected to the ground (0 V), and the drain electrode was subjected to the ESD stress. The GTNMOS differs from GGNMOS in an extra DC gate voltage supply. In our experiment, a 1.5-V DC voltage was applied to the gate electrode during the TLP testing in GTNMOS mode.

Table 1. Some parameters of the device under test.

Parameters	Volume
L (μm)	0.8
T_{OX} (nm)	12.5
T_{BOX} (nm)	400
T_{Si} (nm)	300
L_{Spacer} (μm)	0.1
C_{N+} (cm^{-3})	1×10^{20}
C_{PWELL} (cm^{-3})	1×10^{17}

Figure 1(a) shows the measured TLP *I*–*V* curves near the first breakdown point of the GGNMOS. The measured TLP *I*–*V* curves near the first breakdown point of the GTNMOS are presented in Fig. 1(b) as discussed in our previous work.[16] Each figure includes five curves related to the five different temperatures. The measured TLP *I*–*V* curves are normalized to the current per unit gate width, *i.e.*, each ESD current value is divided by the total width of the PDSOI NMOS device. The measurement results suggest that the values of V_{T1} of GTNMOS are all lower than those of GGNMOS. The value of V_{T1} in GGNMOS mode increases from 8.8 V to 9.7 V with temperature increasing from 30 °C to 195 °C. The total rise is about 0.9 V, accounting for 10.2 percent of room-temperature V_{T1}. In the GTNMOS mode, a 1.5-V voltage is applied to the gate electrode. The value of V_{T1} in GTNMOS mode decreases from 6.84 V to 6.11 V in a temperature range from 30 °C to 195 °C. The total decline is nearly 0.73 V, which is about 10.7 percent of V_{T1} at room temperature, The above results indicate that the V_{T1} varies in an opposite trend with the increasing of temperature in the two modes. The mechanisms will be analyzed by TCAD simulation below.

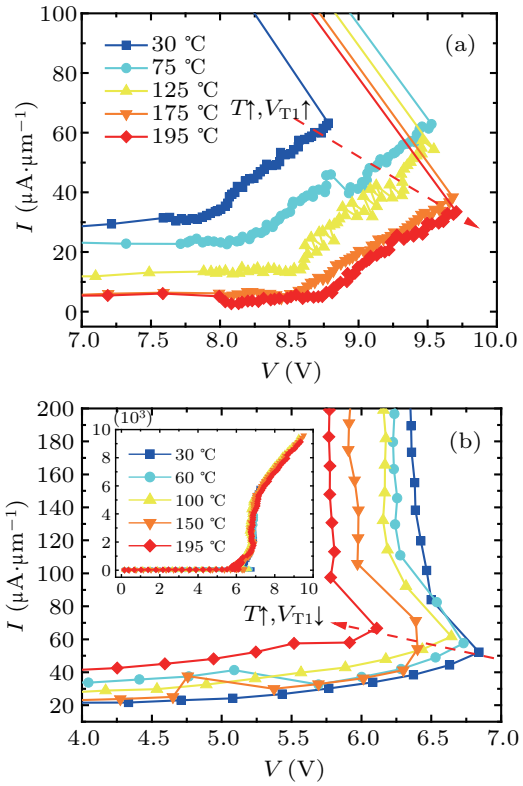


Fig. 1. TLP *I*–*V* curves of DUT in temperature range of 30 °C to 195 °C (near the first breakdown point) for (a) GGNMOS and (b) GTNMOS.

3. Simulation results

To support and analyze the experimental conclusion, TCAD simulation is carried out. The two-dimensional (2D) model for simulation is shown in Fig. 2, in which the body contact is set to be on the right of the source contact. Just because the body contact configuration of the 2D model is different from that in the real H-gate PDSOI NMOS device, the absolute value of V_{T1} in the simulation curve differs from that of the measured TLP *I*–*V* curve. Nevertheless, the same trend of V_{T1} versus temperature is obtained in the TCAD simulation, which is essential to analyze the trigger mechanism at high temperatures.

The simulation method is named the multi-current pulse simulation method. In the method, a customized piecewise linear function (PWL) is used to generate the TLP current pulse which is applied to the drain electrode. As shown in Fig. 2, the DC voltages of 0 V and 1.2 V are applied to the gate electrode

in GGNMOS and GTNMOS modes, respectively. Other electrodes including the source, body, and substrate electrode are connected to the ground (0 V).

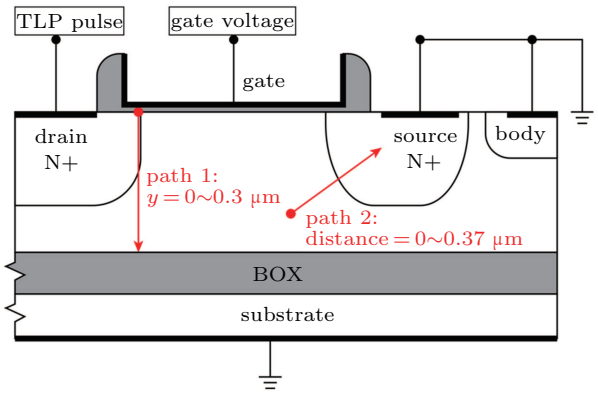


Fig. 2. Schematic diagram of the 2D model.

Figures 3 and 4 show the simulated transient *I*–*V* curves of DUT operating in GGNMOS mode and GTNMOS mode, respectively. The variation of V_{T1} *versus* temperature of TLP testing and TCAD simulation are shown in Fig. 5. The simulation results suggest that V_{T1} increases with temperature increasing in GGNMOS mode and decreases in GTNMOS mode, which is consistent well with the measured TLP *I*–*V* characteristics given in Figs. 1(a) and 1(b).

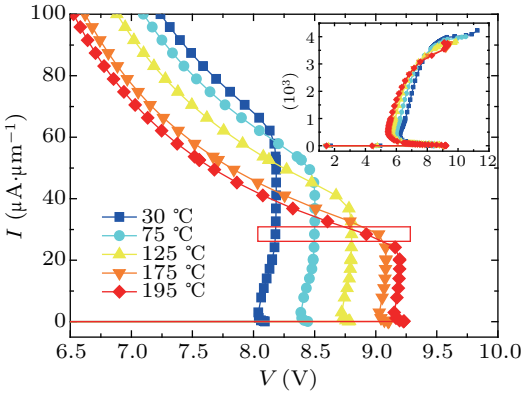


Fig. 3. TCAD simulation *I*–*V* curves of GGNMOS at temperatures ranging from 30 °C to 195 °C near the first breakdown point, with inset showing overall simulation *I*–*V* curves of GGNMOS under five different temperatures.

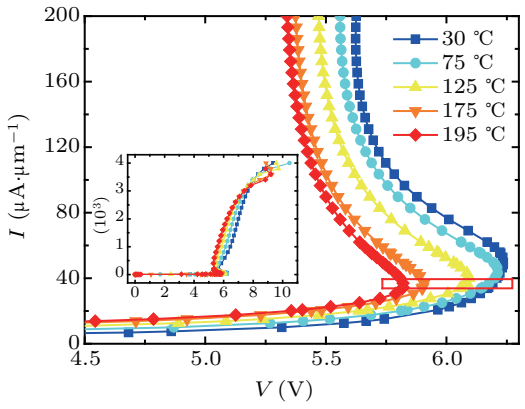


Fig. 4. TCAD simulation *I*–*V* curves of GTNMOS at temperatures ranging from 30 °C to 195 °C near the first breakdown point, with inset exhibiting overall simulation *I*–*V* curves of GTNMOS under five different temperatures.

To analyze the underlying physical mechanism of the temperature dependence of V_{T1} in GGNMOS mode and in GTNMOS mode comparatively, we choose 5 points in each mode to analyze the response process under five operating temperatures as marked in Figs. 3 and 4. At each point, a certain moment in a range of 70%–90% of the TLP pulse period is selected to analyze the distribution of some essential parameters in the following.

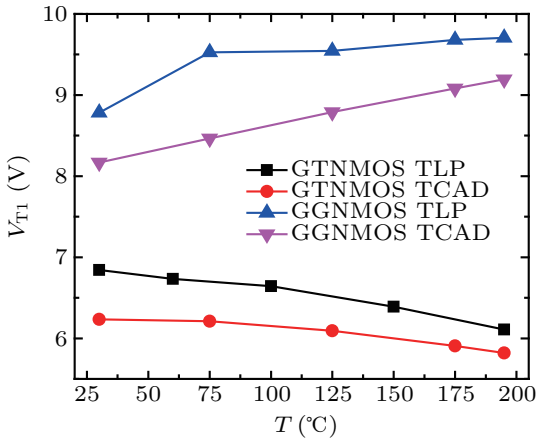


Fig. 5. Variations of V_{T1} with temperature of TLP testing and TCAD simulation.

3.1. Discussion of GGNMOS

3.1.1. Electric field

Before the first breakdown point, the ESD current maintains a very low level and flows through the drain contact, reversed drain–body junction, body region, and the body contact. Because of the high resistance of the reversed drain–body junction, a relatively high ESD voltage is mostly clamped at the junction, thus forming an extremely high electric field. Therefore, the electric field distribution at the first breakdown point is an indication of V_{T1}. The electric field distribution along path 1 (marked in Fig. 2) is shown in Fig. 6. It can be seen that the electric field increases with temperature in GGNMOS mode and decreases in GTNMOS mode. The peak electric field of GGNMOS is about 1.5 times higher than that of GTNMOS. The relationship between the critical electric field, E_c, and the avalanche threshold voltage, V_{ava}, is given by[17]

$$V_{ava} = \left(\frac{32\varepsilon_0\varepsilon_r E_c^3}{9\alpha_j q}\right)^{0.5}, \tag{1}$$

where ε_0 and ε_r are the permittivity of vacuum and the relative dielectric constant, respectively, α_j represents the ionization rate of collision, and q denotes the elementary charge. Equation (1) describes the avalanche mechanism in the linear graded PN junction. As temperature increases, the mean free path of the carriers in the space charge region decreases, a higher E_c is needed for the carriers to obtain enough kinetic

energy to trigger the avalanche breakdown. Thus, the thermal coefficient of the avalanche mechanism is proportional to temperature.[9,10]

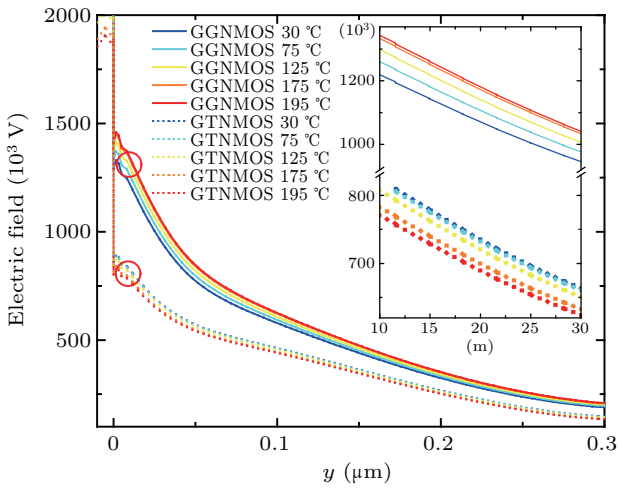


Fig. 6. Electric field distributions in GGNMOS mode and GTNMOS mode along path 1 under various ambient temperatures.

In the GGNMOS mode, the triggering of the DUT relies on the avalanche breakdown of the drain–body junction. The avalanche multiplication generates a large number of electron-hole pairs and the holes drift towards the body contact, which generates a voltage drop across the body resistance R_{Body} and raises the local body potential V_{Body}. The source–body junction is turned on by enough V_{Body}, leading the parasitic BJT to trigger on. Thus, the V_{T1} of GGNMOS is governed by the avalanche critical electric field and the avalanche threshold voltage in the drain–body junction, resulting in the V_{T1} of GGNMOS increasing with temperature rising.

Oppositely, the decreasing of V_{T1} of GTNMOS suggests that there exist other prior triggering mechanisms besides the avalanche in GTNMOS mode.

3.1.2. Impact ionization

Impact ionization occurs when the high reverse bias voltage of the drain–body junction creates a strong internal electric field, which accelerates the carriers through the silicon crystal lattice and produces secondary electron–hole pairs. The impact ionization can be used to characterize the efficiency of avalanche multiplication for GGNMOS.

Figure 7 shows the impact ionization distributions at the drain–body junction under various ambient temperatures in GGNMOS mode and the GTNMOS mode, respectively. It can be seen in Fig. 7 that the total impact ionization decreases with temperature increasing in both GGNMOS mode and GTNMOS mode.

The impact ionization is mainly governed by the electric field and the mean-free path of the carriers. As mentioned before, the critical triggering electric field increases with temperature increasing. Hence, the electric field with a positive temperature coefficient proves to influence the impact ionization little in the GGNMOS mode. The mean free path of the carriers is dominated by the scattering of phonons, generated by the vibration of the atomic lattice, which is positively correlated with temperature. The mean-free path is visualized by the mobility distribution, which decreases with temperature increasing as shown in Fig. 8.

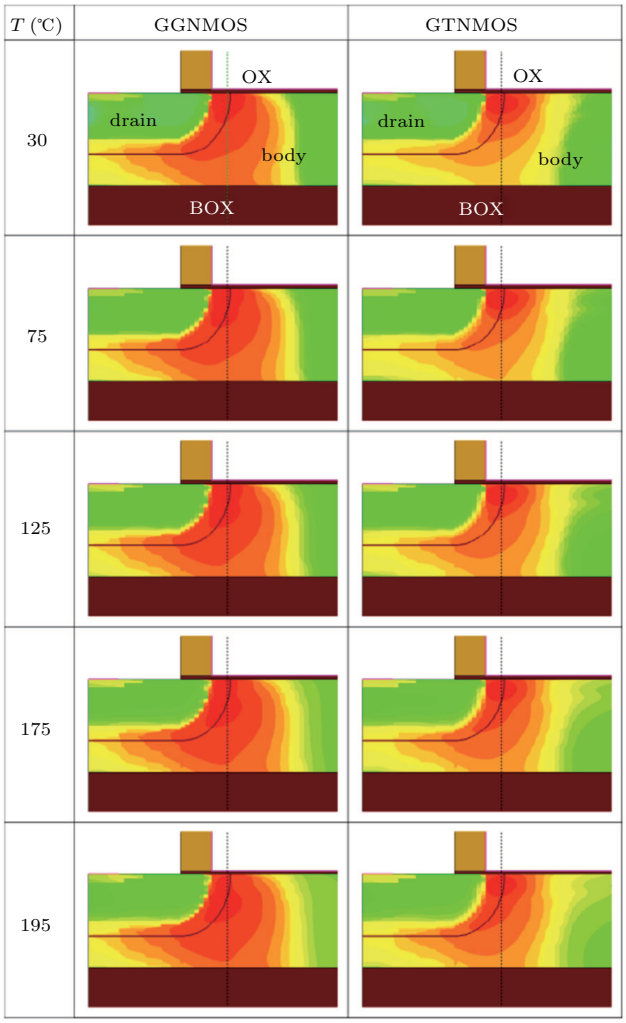


Fig. 7. Impact ionization distributions in GGNMOS mode and GTNMOS mode at drain–body junction under various ambient temperatures.

To sum up, the avalanche threshold voltage of the drain–body junction in DUT increases with temperature increasing because the impact ionization is inversely proportional to temperature. And it is the reason why the V_{T1} in GGNMOS mode rises when the temperature goes up.

From Figs. 3 and 4 it follows that comparing with the GGNMOS mode, V_{T1} of GTNMOS decreases with temperature increasing, which means that the first breakdown in the GTNMOS mode occurs at a lower electric field and lower impact ionization than in GGNMOS. Thus, the temperature dependence of triggering in GTNMOS mode is not governed by avalanche breakdown but the channel current and the triggering-on of the parasitic BJT. We will analyze the V_{T1} of GTNMOS as followed.

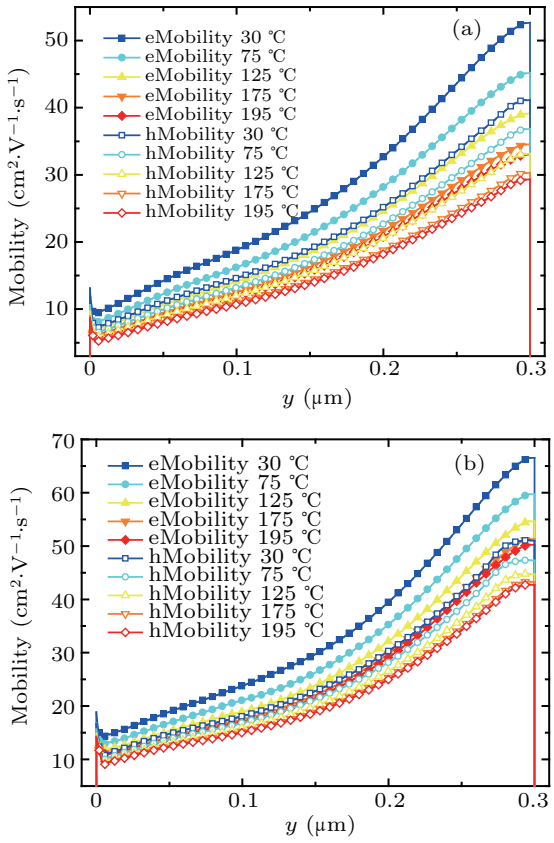


Fig. 8. Mobility distributions in (a) GGNMOS mode and (b) GTNMOS mode along path 1 under various ambient temperatures.

3.2. Discussion of GTNMOS

3.2.1. Channel current

Unlike GGNMOS, the V_{T1} of GTNMOS decreases because there exists channel current, I_{DS}, in the period of ESD pulse. The I_{DS} plays a crucial part in reducing the V_{T1} of GTNMOS mode because the I_{DS} is the main contributor to the increase of the incident current I_p for the avalanche multiplication at the drain–body junction. The avalanche generation current I_{gen} is related to I_p and the avalanche multiplication factor M by[18]

$$I_{gen} = (M-1)I_p. \tag{2}$$

Before the turning on of BJT, body current $I_{Body} = I_{gen}$. The I_p is strengthened by I_{DS}, and a lower M can sustain the same I_{Body}. The I_{DS} makes V_{T1} of GTNMOS decrease with respect to that of GGNMOS. Thus, the temperature dependence of V_{T1} is not simply affected by the avalanche breakdown. As shown in Figs. 1(b) and 4, before the first breakdown points, the I_{DS} of the GTNMOS transistor increases with temperature increasing. According to Eq. (2), I_{DS} strengthens I_p and lowers M, which ultimately makes V_{T1} of GTNMOS decrease.

3.2.2. Electrostatic potential

The forward bias of the source–body junction is one of the most essential conditions to trigger the parasitic BJT. The threshold voltage of the source–body junction can be characterized by the electrostatic potential barrier.

Figure 9 shows the distribution of electrostatic potential along path 2 (marked in Fig. 2) before the ESD stress is applied to the drain electrode of DUT. It suggests that the electrostatic potential barrier at the source–body junction decreases when the temperature goes up. The source–body junction can be forward-biased more easily at higher temperatures, which contributes to the turning on of the parasitic BJT at a lower V_{T1}. Thus, the electrostatic potential barrier of the source–body junction decreasing with temperature increasing is one of the factors leading the V_{T1} to decline in the GTNMOS mode. But it is not the major cause in GGNMOS mode compared with the avalanche breakdown behavior.

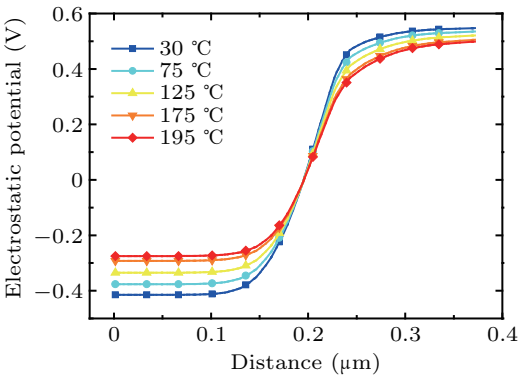


Fig. 9. Electrostatic potential distributions in GTNMOS mode along path 2 under various ambient temperatures.

3.2.3. Body resistance

The body resistance, R_{Body}, is defined as the body resistance from the source–body junction to the body electrode. The R_{Body} influences the body potential near the source–body junction when the body current, I_{Body}, flows through the body region. Previous research has shown that the resistivity of the p-silicon increases with temperature rising in a temperature range from 30 °C to 195 °C.[19]

The current density distribution in the silicon film can be used to characterize R_{Body} indirectly. The total ESD current flows into the DUT through the drain electrode and flows out through the body electrode and the source electrode. Figure 10 shows the total current density distributions of GGNMOS and GTNMOS at five different temperatures. From Fig. 10(b) it can follow that at the same ESD current before GTNMOS is triggered on, the ratio of the body current decreases with temperature increasing. It suggests that the resistance on the path from drain–body junction to body electrode is proportional to temperature. The higher body resistance contributes to higher body potential at the source–body junction, which provides the forward-biasing of the source–body junction and the turning on of the parasitic BJT.

It can be seen in Figs. 10(a) and 10(b) that the I_{Body} of GGNMOS is larger than that of GTNMOS at each temperature when the parasitic BJT is triggered. The I_{Body} from the

avalanche current in GGNMOS mode is large enough to provide the forward-biasing of the source–body junction, so the major cause to dominate the V_{T1} in GGNMOS mode is the avalanche breakdown threshold but not the positive temperature coefficient of R_{Body}.

To sum up, the temperature dependence of RBody is another factor to explain the negative temperature coefficient of V_{T1} in the GTNMOS mode. The body resistance also increases with temperature increasing in the GGNMOS mode as shown in Fig. 10(a). Still, it is not the dominant factor when referring to the temperature dependence of V_{T1}.

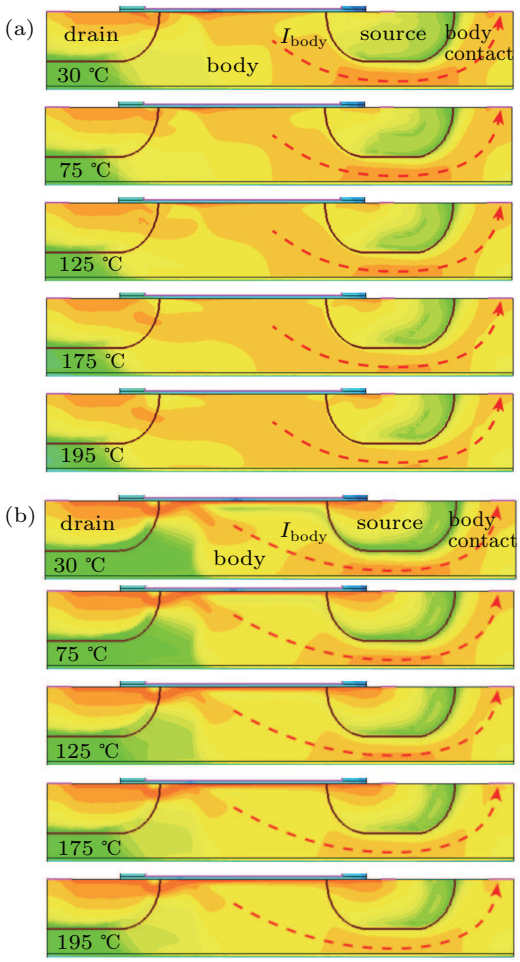


Fig. 10. Current density distributions in (a) GGNMOS mode and (b) GTNMOS mode in the silicon film under various ambient temperatures.

4. Conclusions

We have investigated the triggering parameters, V_{T1}, of a PDSOI NMOS device for ESD protecting device operating at elevated temperatures. We conclude the opposite effect that V_{T1} of GGNMOS increases with temperature increasing and that V_{T1} of GTNMOS shows reverse variation with temperature. Good agreement is achieved between the TLP measurements, and the TCAD simulated results obtained by the multi-current pulse simulation method. More analyses of the temperature dependence of V_{T1} in the two modes are conducted by using TCAD simulation outputs. In the GGNMOS mode, the variation of V_{T1} with temperature is governed by the avalanche breakdown of the drain–body junction while the temperature dependence of V_{T1} in the GTNMOS mode is dominated by the channel current and triggering of the parasitic BJT. This study offers a useful insight into and the information about obtaining the safe margin of the triggering parameters of PDSOI NMOS devices operating in a high-temperature ESD protection environment, and also presents the way of weakening the temperature effects in the two modes, which can help to design the temperature-insensitive ESD protecting devices.

References

[1] Amerasekera E A and Duvvury C 2002 *ESD in silicon integrated circuits*, 2nd edn. (West Sussex: John Wiley & Sons, Ltd.) p. 400
[2] Zhu L, Liang H L, Gu X F and Xu J 2020 *Chin. Phys. B* **29** 068503
[3] Hou F, Chen R B, Du F B, Liu J Z, Liu Z W and Liu J J 2019 *Chin. Phys. B* **28** 088501
[4] Song W Q, Hou F, Du F B, Liu Z W and Liu J J 2020 *Chin. Phys. B* **29** 098502
[5] Cressler J D and Mantooth H A 2017 *Extreme environment electronics* (Boca Raton: CRC Press) p. 1041
[6] Wang A Z H 2020 *On-Chip ESD Protection for Integrated Circuits–An IC Design Perspective* (Massachusetts: Springer Science & Business Media) p. 303
[7] Koo Y S, Lee H D, Won J I and Yang Y S 2010 *The* 2010 *International Power Electronics Conference - ECCE ASIA*, June 21–24, 2010, Sapporo, Japan, p. 248
[8] Meneghesso G, Tazzoli A, Marino F A, Cordoni M and Colombo P 2008 2008 *IEEE International Reliability Physics Symposium*, April 27–May 1, 2008, Phoenix, AZ, USA, p. 3
[9] Liang W, Dong A H, Li H, Miao M, Kuo C C, Klebanov M and Liou J J 2016 *Microelectron. Reliab.* **66** 46
[10] Li C, Zhang F L, Wang C K, Chen Q, Lu F, Wang H, Di M F, Cheng Y H, Zhao H J and Wang A 2018 14*th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, October 31–November 3, 2018, Qingdao, China, p. 743
[11] Jang S L and Lin J K 2000 *Solid-State Electron.* **44** 2139
[12] Jang S L, Lin L S and Li S H 2001 *Solid-State Electron.* **45** 2005
[13] Hou F, Liu J Z, Liu Z W, Huang W, Gong T X, Yu B and Liou J J 2019 *IEEE Trans. Electron Dev.* **66** 2044
[14] Do K I, Lee B S and Koo Y S 2019 *IEEE Electron Dev. Lett.* **40** 283
[15] Arbess H and Bafleur M 2011 *Microelectron. Reliab.* **51** 1980
[16] Wang J X, Li X J, Zhao F Z, Zeng C B, Li B, Han Z S and Luo J J 2020 *Semiconductor Technology* **46** 210
[17] McKay K G 1954 *Phys. Rev.* **94** 877
[18] Amerasekera A, Chang M C, Duvvury C and Ramaswamy S 1997 *IEEE* 34*th Annual International Reliability Physics Symposium*, April 30–May 2, 1996, Dallas, TX, USA, p. 318
[19] Li S S 1978 *Solid-State Electron.* **21** 1109