

Degradation of gate-recessed MOS-HEMTs and conventional HEMTs under DC electrical stress

Yi-Dong Yuan(原义栋), Dong-Yan Zhao(赵东艳), Yan-Rong Cao(曹艳荣), Yu-Bo Wang(王于波), Jin Shao(邵瑾), Yan-Ning Chen(陈燕宁), Wen-Long He(何文龙), Jian Du(杜剑), Min Wang(王敏), Ye-Ling Peng(彭业凌), Hong-Tao Zhang(张宏涛), Zhen Fu(付振), Chen Ren(任晨), Fang Liu(刘芳), Long-Tao Zhang(张龙涛), Yang Zhao(赵扬), Ling Lv(吕玲), Yi-Qiang Zhao(赵毅强), Xue-Feng Zheng(郑雪峰), Zhi-Mei Zhou(周芝梅), Yong Wan(万勇), and Xiao-Hua Ma(马晓华)

Citation: Chin. Phys. B, 2021, 30 (**7**): 077305. DOI: 10.1088/1674-1056/abe117
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Electrochemical liftoff of freestanding GaN by a thick highly conductive sacrificial layer grown by HVPE

Xiao Wang(王骁), Yu-Min Zhang(张育民), Yu Xu(徐俞), Zhi-Wei Si(司志伟), Ke Xu(徐科), Jian-Feng Wang(王建峰), and Bing Cao(曹冰)

Chin. Phys. B, 2021, 30 (**6**): 067306. DOI: 10.1088/1674-1056/abd6fa

Design and simulation of AlN-based vertical Schottky barrier diodes

Chun-Xu Su(苏春旭), Wei Wen(温暐), Wu-Xiong Fei(费武雄), Wei Mao(毛维), Jia-Jie Chen(陈佳杰), Wei-Hang Zhang(张苇杭), Sheng-Lei Zhao(赵胜雷), Jin-Cheng Zhang(张进成), and Yue Hao(郝跃)

Chin. Phys. B, 2021, 30 (**6**): 067305. DOI: 10.1088/1674-1056/abe0c7

Ferroelectric effect and equivalent polarization charge model of $PbZr_{0.2}Ti_{0.8}O_3$ on AlGaN/GaN MIS-HEMT

Yao-Peng Zhao(赵垚澎), Chong Wang(王冲), Xue-Feng Zheng(郑雪峰), Xiao-Hua Ma(马晓华), Ang Li(李昂), Kai Liu(刘凯), Yun-Long He(何云龙), Xiao-Li Lu(陆小力) and Yue Hao(郝跃)

Chin. Phys. B, 2021, 30 (**5**): 057302. DOI: 10.1088/1674-1056/abd469

Analysis of the decrease of two-dimensional electron gas concentration in GaN-based HEMT caused by proton irradiation

Jin-Jin Tang(汤金金), Gui-Peng Liu(刘贵鹏), Jia-Yu Song(宋家毓), Gui-Juan Zhao(赵桂娟), and Jian-Hong Yang(杨建红)

Chin. Phys. B, 2021, 30 (**2**): 027303. DOI: 10.1088/1674-1056/abbbf7

Trap analysis of composite 2D-3D channel in AlGaN/GaN/graded-AlGaN: Si/GaN: C multi-heterostructure at different temperatures

Sheng Hu(胡晟), Ling Yang(杨凌), Min-Han Mi(宓珉瀚), Bin Hou(侯斌), Sheng Liu(刘晟), Meng Zhang(张濛), Mei Wu(武玫), Qing Zhu(朱青), Sheng Wu(武盛), Yang Lu(卢阳), Jie-Jie Zhu(祝杰杰), Xiao-Wei Zhou(周小伟), Ling Lv(吕玲), Xiao-Hua Ma(马晓华), Yue Hao(郝跃)

Chin. Phys. B, 2020, 29 (**8**): 087305. DOI: 10.1088/1674-1056/ab96a4

Degradation of gate-recessed MOS-HEMTs and conventional HEMTs under DC electrical stress*

Yi-Dong Yuan(原义栋)[1,2], Dong-Yan Zhao(赵东艳)[2], Yan-Rong Cao(曹艳荣)[3,4,†], Yu-Bo Wang(王于波)[2], Jin Shao(邵瑾)[1], Yan-Ning Chen(陈燕宁)[2], Wen-Long He(何文龙)[3,4,†], Jian Du(杜剑)[2], Min Wang(王敏)[2,3], Ye-Ling Peng(彭业凌)[2], Hong-Tao Zhang(张宏涛)[3,4], Zhen Fu(付振)[2], Chen Ren(任晨)[2,3], Fang Liu(刘芳)[2], Long-Tao Zhang(张龙涛)[2,3], Yang Zhao(赵扬)[2], Ling Lv(吕玲)[4], Yi-Qiang Zhao(赵毅强)[1], Xue-Feng Zheng(郑雪峰)[4], Zhi-Mei Zhou(周芝梅)[5], Yong Wan(万勇)[5], and Xiao-Hua Ma(马晓华)[4]

[1] *School of Microelectronics, Tianjin University, Tianjin* 300072, *China*
[2] *Beijing Engineering Research Center of High-reliability IC with Power Industrial Grade, Beijing Smart-Chip Microelectronics Technology Co., Ltd, Beijing* 100192, *China*
[3] *School of Electro-Mechanical Engineering, Xidian University, Xi'an* 710071, *China*
[4] *Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xidian University, Xi'an* 710071, *China*
[5] *Smart Shine Microelectronics Technology Co., Ltd, Qingdao* 100081, *China*

(Received 13 November 2020; revised manuscript received 25 December 2020; accepted manuscript online 29 January 2021)

The performance degradation of gate-recessed metal–oxide–semiconductor high electron mobility transistor (MOS-HEMT) is compared with that of conventional high electron mobility transistor (HEMT) under direct current (DC) stress, and the degradation mechanism is studied. Under the channel hot electron injection stress, the degradation of gate-recessed MOS-HEMT is more serious than that of conventional HEMT devices due to the combined effect of traps in the barrier layer, and that under the gate dielectric of the device. The threshold voltage of conventional HEMT shows a reduction under the gate electron injection stress, which is caused by the barrier layer traps trapping the injected electrons and releasing them into the channel. However, because of defects under gate dielectrics which can trap the electrons injected from gate and deplete part of the channel, the threshold voltage of gate-recessed MOS-HEMT first increases and then decreases as the conventional HEMT. The saturation phenomenon of threshold voltage degradation under high field stress verifies the existence of threshold voltage reduction effect caused by gate electron injection.

Keywords: gate-recessed MOS-HEMTs, channel electron injection, gate electron injection, barrier layer traps

PACS: 73.61.Ey, 73.20.–r, 73.40.Kp, 73.40.Qv **DOI:** 10.1088/1674-1056/abe117

1. Introduction

AlGaN/GaN high electron mobility transistor (HEMT) is a kind of semiconductor device with wide band gap, high electron mobility and high breakdown electric field. Owing to its superior electrical, optical and thermal properties, it has become a research hotspot of the third-generation semiconductor materials and devices.[1–5] The gate-recessed metal–oxide–semiconductor high electron mobility transistor (MOS-HEMT) device can reduce the gate tunneling current and improve the gate control ability of the conventional HEMT device, so it has been widely concerned.[6–10] GaN-based HEMT has great application prospects in high temperature, high frequency, and high power electronics. Although it has been put into the market to a certain extent, there are still many reliability problems that seriously restrict the development of GaN HEMT.[11–14] GaN-based HEMTs are usually used in microwave high-power fields. The devices often work under high drain-bias (V_{DS}). Therefore, the degradation of GaN-based HEMTs in high field has aroused extensive research. Under high field stress, the channel hot electron effect can cause the device characteristics and output current to degrade.[15,16] Trew *et al.*[17] put forward that there exists a strong electric-field peak near the gate between gate and drain, and gate electrons can get to the barrier layer's surface under the influence of electric-field peak, which results in leakage current between the gate and drain. Gate electrons can also fill the surface traps, and thus forming a virtual gate, which will cause some degradation phenomena such as the increase of threshold voltage (V_{TH}) and the reduction of drain current. The research of Wenping Gu *et al.*[18] shows that the effect of hot electron and the virtual gate lead the device to degrade.

At present, there are many studies on AlGaN/GaN conventional HEMTs' degradation under electrical stress, show-

*Project supported by the Laboratory Open Fund of Beijing Smart-chip Microelectronics Technology Co., Ltd and the National Natural Science Foundation of China (Grant No. 11690042), the Science Challenge Project, China (Grant Nos. TZ2018004 and 12035019), and the National Major Scientific Research Instrument Projects, China (Grant No. 61727804).

†Corresponding author. E-mail: yrcao@mail.xidian.edu.cn
‡Corresponding author. E-mail: he.wenlong1991@163.com

© 2021 Chinese Physical Society and IOP Publishing Ltd

ing that the channel hot electron injection and gate electron injection can lead the threshold voltage to vary. However, there are few studies of the gate-recessed MOS-HEMT device. In order to analyze the difference and similarity in reliability between gate-recessed MOS-HEMT device and conventional HEMT device, in this paper the comparison between the characteristic changes of gate-recessed Al_2O_3/AlGaN/GaN HEMT and conventional HEMT devices are conducted under electrical stress. And the influence of the two degradation modes, channel hot electron injection, and gate electron injection, on the characteristic parameters and reliability of the device are studied.

2. Devices and stress experiments

The tested GaN-based gate-recessed MOS-HEMTs were fabricated by low pressure metal-organic chemical vapor deposition (LP-MOCVD) equipment to grow AlGaN/GaN heterostructure on sapphire substrate. In the GaN-based gate-recessed MOS-HEMTs, the materials from bottom to top were sapphire substrate, 40-nm-thick AlN nucleating layer, 1-μm-thick undoped GaN epitaxial layer, and 25-nm-thick AlGaN barrier layer with a doping concentration of 2×10^8 cm^{-3}. In addition, Al component of AlGaN barrier layer was about 30%. Chlorine-based reactive ion etching (RIE) was used to etch the recessed-gate, and atomic layer deposition (ALD) was used to deposit 5-nm-thick Al_2O_3 gate dielectric layer. Electron beam evaporation was used to grow a Ti/Al/Ni/Au (respectively with 22 nm/140 nm/55 nm/45 nm in thickness) multilayer metal to realize the ohmic contacts and also used to form a Ni/Au/Ni (respectively with 45 nm/200 nm/20 nm in thickness) gate electrode multilayer metal. The gate length and width for each of the gate-recessed MOS-HEMTs were respectively 0.8 μm and 50 μm, and the thickness of the dielectric layer was 5 nm. The gate electrode lay in the midpoint between source and drain while Si_3N_4 layer acted as a passivation layer. Compared with the gate-recessed MOS-HEMT device proposed in this work, conventional HEMT device had no groove or deposition oxide layer step, and the rest of the structure were the same. The schematic diagrams of the two kinds of HEMTs are shown in Fig. 1.

With the Hall effect measurement tests at room temperature, we obtained the mobility and density of two-dimensional electron gas (2DEG), which are 1150 cm^2/V·s and 1.2×10^{13} cm^{-2}, respectively in the AlGaN/GaN heterostructure. The Keithley4200, a semiconductor parameter analyzer was used to test the direct current (DC) characteristics and electrical-stress characteristics of HEMTs. There are three main electrical-stress test parts in this paper: (i) channel electron injection stress (gate floating, $V_S = 0$ V, and $V_D = 15$ V); (ii) gate electron injection stress (source floating, $V_G = -20$ V, and $V_D = 0$ V); (iii) another high field electrical stress (coupling between channel electron injection and gate electron injection) ($V_G = V_S = 0$ V and $V_D = 15$ V). The stress times of tests were all 1000 s.

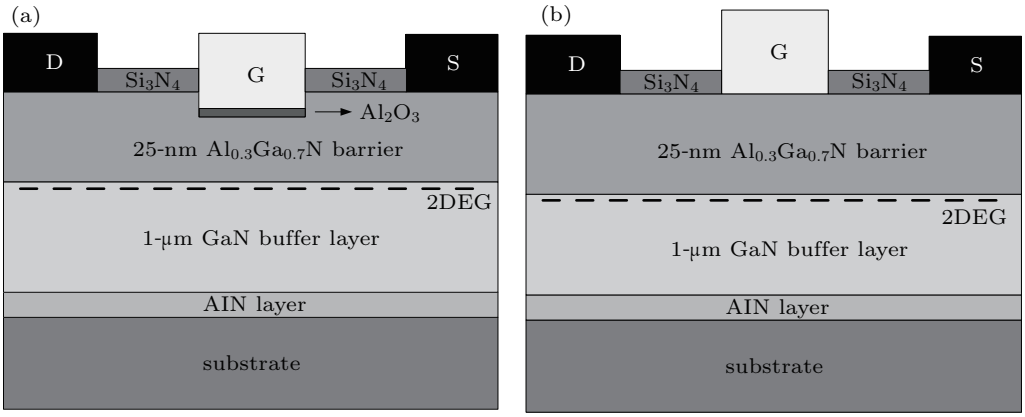


Fig. 1. Schematic diagram of (a) gate-recessed MOS-HEMT and (b) conventional HEMT.

3. Experimental results and analysis

3.1. Experimental results

After 1000 s of channel electron injection stress (gate floating, $V_S = 0$ V, and $V_D = 15$ V) and gate electron injection stress (source floating, $V_G = -20$ V, and $V_D = 0$ V), the threshold voltage variations of conventional HEMTs and gate-recessed MOS-HEMTs with stress time are obtained as shown in Figs. 2 and 3. In Fig. 2, under the stress of channel electron injection, the characteristics of the two kinds of devices are degraded, and the threshold voltages are both increased.

Figure 3 shows the degradations of conventional HEMT and gate-recessed MOS-HEMT under gate electron injection stress. The threshold voltage of conventional HEMT decreases (negative shift) in the first 100 s, while the threshold voltage of gate-recessed MOS-HEMT increases (positive shift) significantly during the first 100-s stress. And then in the 100 s–1000 s process of the gate electron injection stress, the threshold voltage of conventional HEMT and the threshold voltage of gate-recessed MOS-HEMT are both reduced.

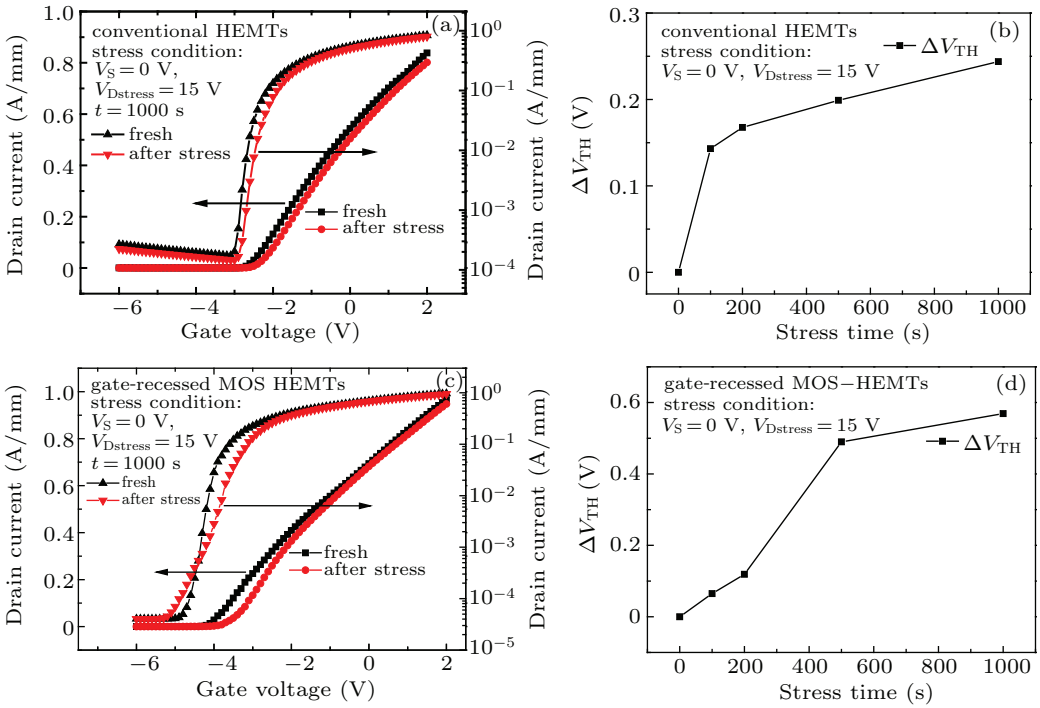


Fig. 2. Under channel electron injection stress: (a) drain current *versus* gate voltage, (b) threshold voltage *versus* stress time of conventional HEMT, (c) drain current *versus* gate voltage, and (d) threshold voltage *versus* stress time of gate-recessed MOS-HEMT.

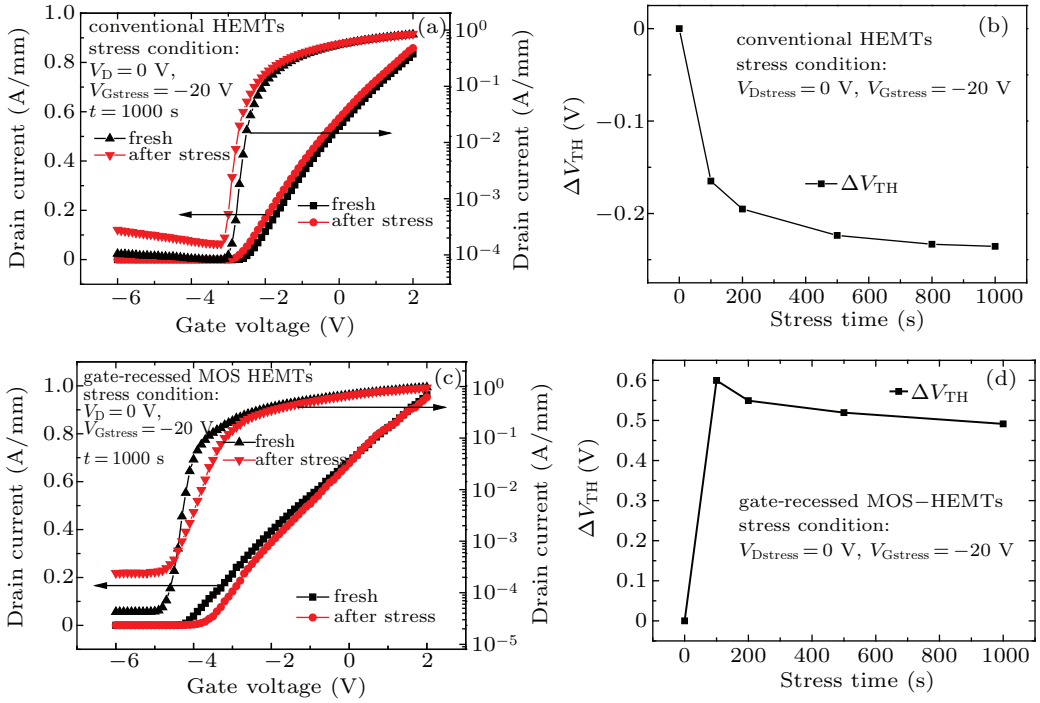


Fig. 3. Under gate electron injection stress: (a) drain current *versus* gate voltage, (b) threshold voltage *versus* stress time of conventional HEMT, (c) drain current *versus* gate voltage, (d) threshold voltage *versus* stress time of gate-recessed MOS-HEMT.

The threshold voltage and drain current degradations of the two devices under the two kinds of electron injection stresses are obtained and shown in Table 1. For the same device, the degradation under channel electron injection condition is more serious, and the electrons trapped by the barrier layer are an important factor leading the parameters to degrade, indicating that the hot electrons generated by the channel impact ionization captured by the barrier layer traps are more important in the case of high-field electrical stress.

Table 1. Parameters' degradation of two kinds of devices under two electron injection stresses.

	Conventional HEMTs		Gate-recessed MOS-HEMTs	
Parameters	I_D	V_{TH}	I_D	V_{TH}
Channel electron injection	4.43%	9.51%	2.87%	13.57%
Gate electron injection	2.82%	9.28%	1.05%	11.75%

In addition, from Figs. 2 and 3, we can obtain that the

leakage currents degrade much more seriously under gate electron injection stress than under channel electron injection stress. And the subthreshold swing (SS) of gate-recessed MOS-HEMT change much larger than that of conventional HEMT.

3.2. Mechanism analysis

Under the channel hot electron injection condition, electrons in the device channel are accelerated by the strong electric field and become hot electrons with high energy. The hot electrons can overflow from the channel, and may be trapped by defects in the AlGaN barrier layer, causing the current to decrease and the threshold voltage to increase in the device. High-energy hot electrons may collide with the lattices to produce new defects,[19,20] resulting in further degradation. At the same time, the gate etching of the gate-recessed MOS-HEMT brings about more defects under the gate dielectric of the device[21] which can cause the SS to degrade after being stressed. With the injection of channel hot electrons, the traps under the gate dielectric can capture electrons and form an additional negative charge layer under the MOS structure. This charge layer will shield part of the electric field from the gate to the channel, thereby resulting an additional threshold voltage degradation, and the schematic diagram is shown in Fig. 4(a). Therefore, for the gate-recessed MOS-HEMT device, when channel hot electrons are injected, the degradation of the device is the result of the combined effect of traps in the barrier layer and those under the gate dielectric of the device.

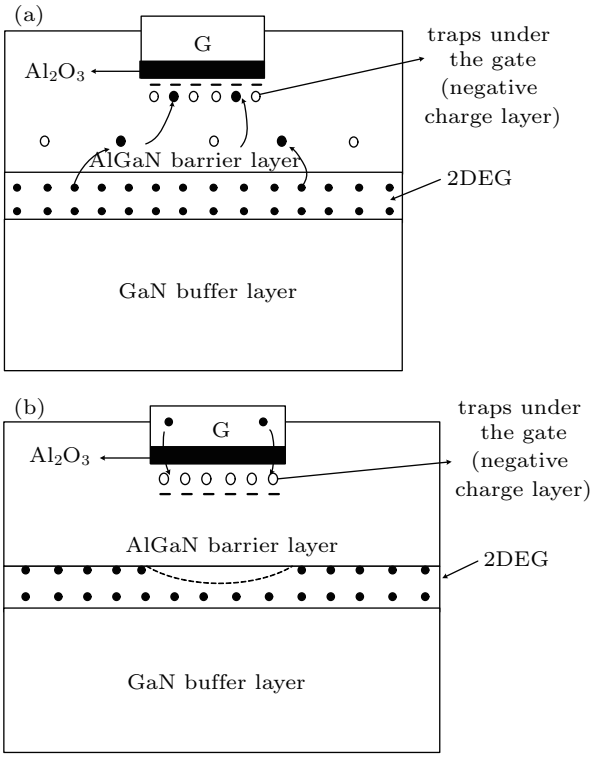


Fig. 4. Effects of under-gate traps on gate-recessed MOS-HEMT under stresses of (a) channel hot electrons injection and (b) gate electrons injection.

In some researches it is believed that in the process of gate electron injection, gate electrons can be injected into the barrier layer's surface to fill in the surface state, thus forming a virtual gate between the gate and the drain,[22] which plays a role in depleting the channel, thus increasing the threshold voltage and reducing the current. However, Table 1 shows that the threshold voltage of conventional HEMT device under gate electron injection stress does not increase but decreases. The conventional HEMT has no gate dielectric, and the gate electrons are easier to inject into the barrier layer under the strong negative gate voltage stress. When the electrons are injected into the barrier layer, on the one hand, the surface states will be filled to form a virtual gate; on the other hand, the electrons injected into the barrier layer can be trapped and those above Fermi level in AlGaN barrier layer will be released into GaN layer under the effect of negative gate voltage stress, which increases the 2DEG concentration as shown in Fig. 5.[23] The effect of increasing 2DEG concentration is greater than that of the virtual gate, therefore, the threshold voltage of conventional HEMT decreases. However, under the gate electron injection stress, the threshold voltage of gate-recessed MOS-HEMT first increases and then decreases. This is because in addition to the depletion of the channel by the virtual gate, the traps under the gate can capture the electrons from the gate injection, thus forming a negative charge layer, which can also deplete part of the channel, as shown schematically in Fig. 4(b). Therefore, for the gate-recessed MOS-HEMT, the threshold voltage increases significantly in the first 100 s. However, with the extension of the stress time, the number of electrons tunneling through the gate dielectric into the barrier layer and then releasing into the channel increases, resulting in the reduced threshold voltage as shown in Fig. 3(d) after 100 s. In addition, with the effect of gate electrons, the traps under gate result in much larger *SS* and leakage current of gate-recessed MOS-HEMT.

In order to further analyze the changes of the traps inside the device under the gate electron injection stress, the interface traps are characterized by the conductivity method,[24,25] as their time constant τ is relatively small and can trap and release the electrons easily. The detailed principle for this technique can be found in Ref. [26]. The experimental data of parallel conductance G_P/ω as a function of radial frequency ω of the gate-recessed MOS-HEMT before and after the electrical stress are shown in Fig. 6. And the relationship between G_P/ω and ω can be expressed as[26]

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1+(\omega\tau_{it})^2], \tag{1}$$

where D_{it} and τ_{it} are the interface trap density and time constant, respectively.

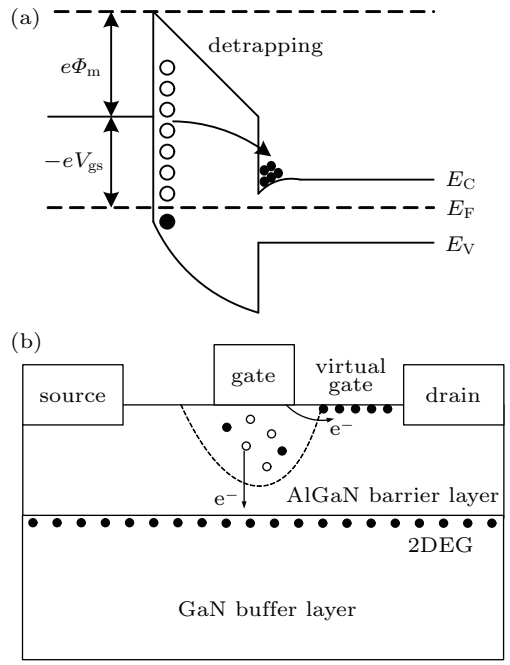


Fig. 5. Under gate electron injection stress: (a) energy band diagram and (b) structure diagram of electrons entering into channel through barrier layer trap.

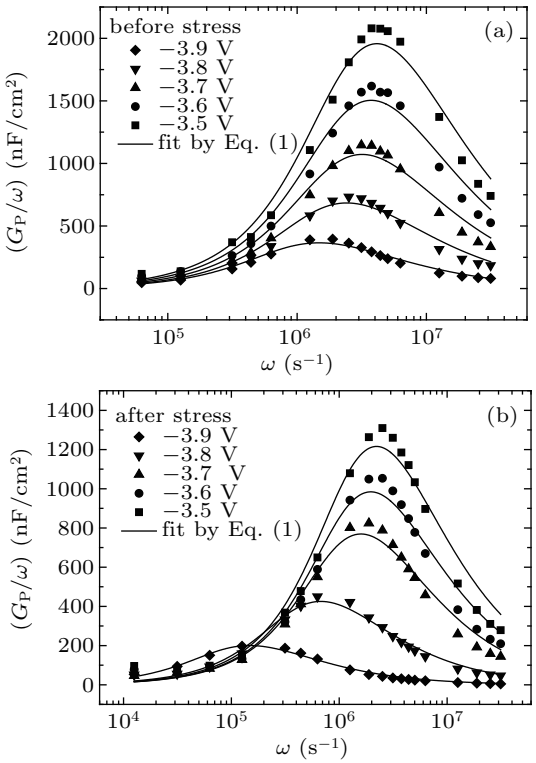


Fig. 6. (G_P/ω)–ω curves (a) before stress and (b) after stress for gate-recessed MOS-HEMT device.

According to the curves fitted by Eq. (1) in Fig. 6, we can obtain the interface trap density D_{it} and time constant τ_{it}. The range of D_{it} and τ_{it} before being stressed are 0.57×10^{13} eV^{-1}·cm^{-2}–3.04×10^{13} eV^{-1}·cm^{-2} and 0.5 μs–1.3 μs respectively. After being stressed for 1000 s, D_{it} and τ_{it} become 0.31×10^{13} eV^{-1}·cm^{-2}–1.89×10^{13} eV^{-1}·cm^{-2} and 0.9 μs–13.7 μs. The increase of the time constant τ_{it} in Fig. 7(a) shows that some interface traps have become deeper level traps after being stressed. The interface trap energy E_T can be estimated from the following equation:[27]

$$\tau_{it} = (\sigma_T N_C \nu_t)^{-1} \exp\left(\frac{E_T}{kT}\right), \tag{2}$$

where the capture cross section σ_T, the density of states in the conduction band N_C, and the average thermal velocity of the carriers ν_t are all constants, and have been reported in other paper.[28] The relationship between E_T and D_{it} is illustrated in Fig. 7(b). The trap energy level E_T is higher, and the trap densities D_{it} are lower after being stressed than before being stressed. The results are consistent with those of Fig. 7(a). Therefore, the shallow level traps that can capture the gate injected electrons and release them into the channel become less, and thus the threshold voltage drops slowly. It is further proved that the threshold voltage is affected by the electron capture and release effect of barrier layer traps under the gate electron injection stress.

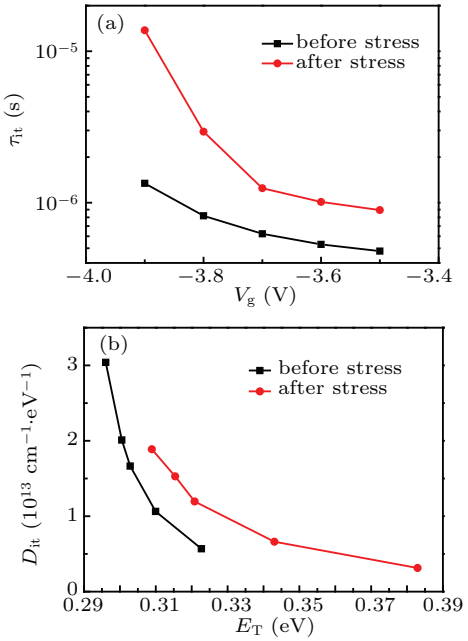


Fig. 7. (a) Relationship between time constant and gate voltage and (b) relationship between trap energy level E_T and trap density D_{it} before and after being stressed, for gate-recessed MOS-HEMT device.

Figure 8 shows the threshold voltage changes of conventional HEMT and gate-recessed MOS-HEMT under another high field stress condition (coupling between channel electron injection and gate electron injection) ($V_G = V_S = 0$ V, $V_D = 15$ V). In the first 100 s, the threshold voltages of both HEMTs increase obviously, and then increase slowly in the period of 100 s–1000 s, which is different from the degradation of device under the stress of channel hot electron injection. Under this high field stress, in addition to the effect of channel electron injection, the gate electrons will be injected into the barrier layer by the voltage between the gate and drain, $V_{GD} = -15$ V. According to the previous analysis, the gate electron injection can cause the threshold voltage to

decrease. Under the effect of coupling between channel electron and gate electron injection, the threshold voltage of the device increases slowly in the period from 100 s to 1000 s. The overall increase of the threshold voltage under this high field stress indicates that the main effect in the process comes from the influence of channel electron injection.

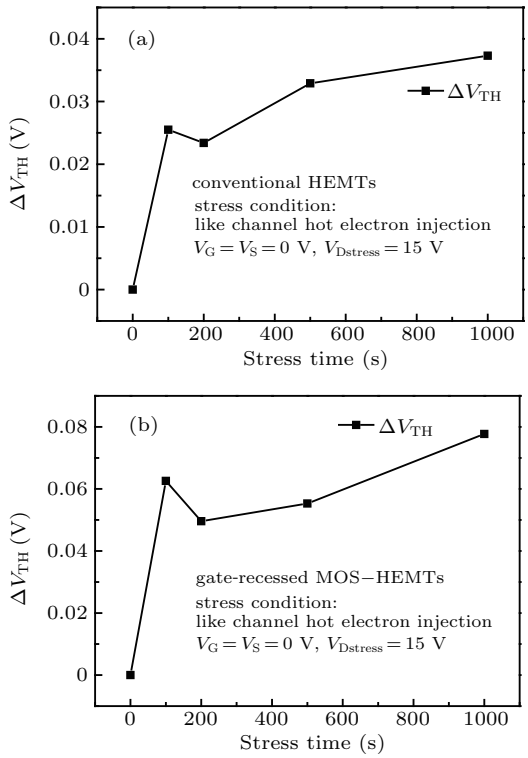


Fig. 8. Threshold voltage changes of (a) conventional HEMTs and (b) gate-recessed MOS-HEMTs under high field stress (coupling between channel electron injection and gate electron injection).

4. Conclusions

Owing to the introduction of etching and gate dielectrics into gate-recessed MOS-HEMTs, when studying the degradation of gate-recessed MOS-HEMTs and conventional HEMTs under different electron injection modes, it is necessary to take the influence of the under-gate traps into consideration. Under the channel hot electron injection stress, besides the effect of barrier layer traps, the traps introduced by groove etching can trap electrons and deplete part of the channel. Therefore, the degradation of gate-recessed MOS-HEMT is more serious. The gate electrons injected into the barrier layer will be released into the channel, which makes the threshold voltage degradation different from the previous studies, that is, the threshold voltage decreases. Meanwhile, because of defects under gate dielectrics which can trap electrons from gate and deplete part of the channel, the threshold voltage of gate-recessed MOS-HEMT first increases and then decreases as that of the conventional HEMT does. In addition, the increase of threshold voltage is slow under the condition of high field electrical stress (coupling between the channel electron injection and gate electron injection). It is further proved that the gate electron injection can reduce the threshold voltage. At the same time, the overall increase of threshold voltage indicates that the electron captured by barrier trap comes mainly from channel hot electrons injection.

References

[1] Raja P V, Bouslama M, Sarkar S, Pandurang K R, Nallatamby J C, Das-Gupta N and Das Gupta A 2020 *IEEE Trans. Electron Dev.* **67** 2304

[2] Radhakrishna U, Choi P and Antoniadis D A 2010 *IEEE Trans. Electron Dev.* **66** 95

[3] Huang S, Liu X, Wang X, Kang X, Zhang J, Fan J, Shi J, Wei K, Zheng Y, Gao H, Sun Q, Wang M, Shen B and Chen K J 2018 *IEEE Trans. Electron Dev.* **65** 207

[4] Zhang S, Wei K, Xiao Y, Ma X H, Zhang Y C, Liu G G, Lei T M, Zheng Y K, Huang S, Wang N, Asif M and Liu X Y 2018 *Chin. Phys. B* **27** 097309

[5] Wu Y F, Kapolnek D, Ibbetson J P, Parikh P, Keller B P and Mishra U K 2001 *IEEE Trans. Electron Dev.* **48** 586

[6] Hao Y, Yang L, Ma X H, Ma J G, Cao M Y, Pan C Y, Wang C and Zhang J C 2011 *IEEE Electron Dev. Lett.* **32** 626

[7] Acurio E, Crupi F, Magnone P, Trojman L and Lucolano F 2017 *Microelectron. Eng.* **178** 42

[8] Lee C T and Wang C C 2018 *AIP Adv.* **8** 045014

[9] Kim H S, Jang W H, Eom S K, Han S W, Kim H, Seo K S, Cho C H and Cha H Y 2018 *J. Semicond. Technol. Sci.* **18** 187

[10] Zhu J J, Jing S Q, Ma X H, Liu S Y, Wang P F, Zhang Y C, Zhu Q, Mi M H, Hou B, Yang L, Kuball M and Hao Y 2020 *IEEE Trans. Electron Dev.* **67** 3541

[11] Jiang H X, Zhu R Q, Lyu Q and Lau K M 2019 *IEEE Electron Dev. Lett.* **40** 530

[12] Li S C, Hu Q L, Wang X, Li T Y, Li X F and Wu Y Q 2019 *IEEE Electron Dev. Lett.* **40** 295

[13] Efthymiou L, Murukesan K, Longobardi G, Udrea F Shibib A and Terrill K 2019 *IEEE Electron Dev. Lett.* **40** 1253

[14] Mao W, Fan J S, Du M, Zhang J F, Zheng X F, Wang C, Ma X H, Zhang J C and Hao Y 2016 *Chin. Phys. B* **25** 127305

[15] Meneghesso G, Mion A, Neviani A, Matloubian M, Brown J, Hafizi M, Liu T, Canali C, Pavesi M, Manfredi M and Zanoni E 1996 *IEEE Electron Devices Meeting*, San Francisco, CA, USA p. 43

[16] Dammann M, Pletschen W, Waltereit P, Bronner W, Quay R, Muller S, Mikulla M, Ambacher O, van der Wel P J, Murad S, Rödle T, Behtash R, Bourgeois F, Riepe K, Fagerlind M and Sveinbjornsson E O 2009 *Microelectron. Reliab.* **49** 474

[17] Trew R J, Liu Y, Kuang W W and Bilbro G L 2006 *IEEE Compound Semiconductor Integrated Circuit Symposium*, San Antonio, TX, USA p. 103

[18] Gu W P, Hao Y, Zhang J C, Wang C, Feng Q and Ma X H 2009 *Chin. J. Phys.* **58** 511

[19] Koley G, Kim H, Eastman L F and Spencer M G 2003 *Electron. Lett.* **39** 1217

[20] Nicollian E H and Goetzberger A 1967 *Bell System Technical Journal* **46** 1055

[21] Sicre S B F and De Souza M M 2010 *IEEE Trans. Electron Dev.* **57** 1642

[22] Ghosh S, Das S, Dinara S M, Bag A, Chakraborty A, Mukhopadhyay P, Jana S K, and Biswas D 2018 *IEEE Trans. Electron Dev.* **65** 1333

[23] Kim H, Thompson R M, Tilak V, Prunty T R, Shealy J R and Eastman L F 2003 *IEEE Electron Dev. Lett.* **24** 421

[24] Coffie R, Chen Y C, Smorchkova I, Wojtowicz M, Chou Y C, Heying B and Oki A 2006 *IEEE International Reliability Physics Symposium Proceedings*, San Jose, CA, USA p. 99

[25] Fu L H, Lu H, Chen D J, Zhang R, Zheng Y K, Wei K and Liu X Y 2012 *Chin. Phys. B* **21** 108503

[26] Schroder D K 2006 *Semiconductor Material and Device Characterization* (New York: Wiley) p. 784

[27] Shih H A, Kudo M and Suzuki T K 2012 *Appl. Phys. Lett.* **101** 043501

[28] Gregušová D, Stoklas R, Mizue C H, Hori Y, Novák J, Hashizume T and Kordoš P 2010 *J. Appl. Phys.* **107** 106104