

SBT-memristor-based crossbar memory circuit

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SBT-memristor-based crossbar memory circuit*

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Implementing memory using nonvolatile, low power, and nano-structure memristors has elicited widespread interest. In this paper, the SPICE model of $Sr_{0.95}Ba_{0.05}TiO_3$ (SBT)-memristor was established and the corresponding characteristic was analyzed. Based on an SBT-memristor, the process of writing, reading, and rewriting of the binary and multi-value memory circuit was analyzed. Moreover, we verified the SBT-memristor-based 4×4 crossbar binary and multi-value memory circuits through comprehensive simulations, and analyzed the sneak-path current and memory density. Finally, we apply the 8×8 crossbar multi-value memory circuits to the images memory.

Keywords: memristor, memory, SPICE, crossbar

PACS: 84.32.−y, 85.25.Hv **DOI:** 10.1088/1674-1056/abd7dc

1. Introduction

The amount of data that needs to be stored is increasing, and the requirement of memory equipment is getting higher. However, it has become more difficult to shrink transistor dimensions to manufacture larger capacity memory devices due to the limits of semiconductor material and current manufacturing technology.[1,2] The emergence of memristors provides an excellent solution to this problem. Its existence was predicted by professor Chua in 1971,[3] but was not physically realized due to the limitations of the processing technology. In 2008, a research group from HP Labs, led by Dr. Williams, developed the first memristor, which consists of a double-layered TiO_2 film.[4] Now memristors have been made of various materials, such as Y_2O_3, NbO_2, MoS_2, TaO_x, SiO_2.[5–10] Memristors have been used in chaotic systems, neuromorphic systems, and logic circuits.[11–16]

The resistance of the memristor will be changed with the quantity of charge flowing and its *u*–*i* characteristic curve is a pinched hysteresis loop under a periodic excitation.[17,18] When power is disconnected from the memristor, its state will be maintained until the power is supplied again. This means that the memristor device can be used as a non-volatile memory component.[19–22] Memristive memory technologies such as the resistive random access memory (RRAM) have several desirable attributes.[23–30] They are classified as non-volatile with near-zero standby power consumption and they have ultra-high density.[31–35] Most memristor crossbar memory are implemented based on the HP memristor model.[36–38] In Ref. [36], a 2T2M memristor-based memory cell was proposed, which can realize binary memory. In Ref. [37], a 2T1M memristor-based memory cell was proposed and binary memory was realized, in the process of reading data, the two transistors in the memory cell must work alternately.

A $Sr_{0.95}Ba_{0.05}TiO_3$ (SBT)-memristor SPICE model was established in this paper, it is based on a previously published SBT-memristor model.[39] According to the characteristics of SBT-memristor, the binary and multi-value memory process of writing, reading, and rewriting based on an SBT-memristor was analyzed. Furthermore, a novel crossbar memory circuit composed of 1 transistor and 1 SBT-memristor memory cell was proposed, which has higher stability and memory density.

2. The SBT-memristor and its SPICE model

Appropriate models of memristors is essential for memristor-based circuit and system design. Different kinds of memristors possess distinct models depending on the material, size, manufacturing process, *etc.* In our previous work, an SBT nanometer film was prepared.[40] The SBT-memristor flux-controlled mathematical model with deterministic parameters was obtained as follows:

$$\begin{aligned} i &= (A + B|\varphi(t)|)u(t), \\ \frac{\mathrm{d}\varphi(t)}{\mathrm{d}t} &= u(t), \end{aligned} \tag{1}$$

where $A = 0.0676$, and $B = 0.3682$.[39]

Next, we established the corresponding SPICE model of the SBT-memristor to facilitate circuit analysis. Table 1 describes the SPICE sub-circuit.

Table 1. Sub-circuit description of the SBT-memristor model.

*SBT-memristor model
.SUBCKT memristor 1 2 PARAMS:
.param $a = 0.0676$ $b = 0.3682$
Cx x 0 1 IC = 0.0315
Raux x 0 1T
Gx 0 x value = {V(1,2)}
Gw 1 2 value = $\{(a + b*(\mathrm{abs}(V(x))))*V(1,2)\}$
.ENDS memristor

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Applying AC power to the memristor, the typical characteristic curve can be obtained in Fig. 1. Subject to bigger positive (or negative) voltage pulses, the memductance increases (or decreases) obviously; while subject to smaller (or zero) voltage pulses, the memductance would slowly increase (or unchanged).

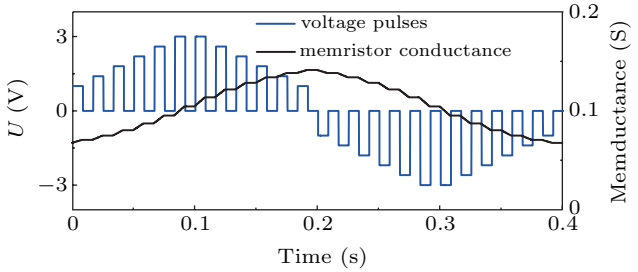


Fig. 1. The changes of memductance with different voltage pulses.

3. The binary memory circuit based on an SBT-memristor

3.1. The SBT-memristor-based memory circuit

In Fig. 2, a memory circuit based on the SBT-memristor was designed. Floating, writing (rewriting), and reading were realized by switching on "1", "2", and "3", respectively.

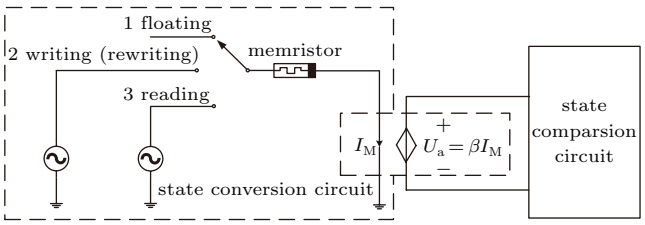


Fig. 2. An SBT-memristor-based memory circuit.

When the switch was set to "3", three steps were required to achieve the reading. Firstly, the memory state of the memristor was converted into the current signal I_M by the state conversion circuit. Secondly, the current signal I_M was converted to voltage signal U_a by the current controlled voltage source, where $U_a = \beta I_M$. Finally, the voltage signal U_a was converted to digital output by the state comparison circuit.

3.2. The design of binary memory circuit based on an SBT-memristor

In Fig. 3, the binary memory circuit based on an SBT-memristor was designed. When the voltage of comparator port 1 was greater than the voltage of port 2, the output voltage was 5 V, the logic value was set as "1", or else the output voltage was 0 V, the logic value was set as "0". The circuit parameters were set as follows: $R_1 = R_2 = R_3 = 1$ kΩ, β = 1 Ω, $U_{ref1} = 5$ V, and $U_{ref2} = 0.61$ V.

The relationship between the memristor current value and the memory data were exhibited in Table 2. The current I_S was set as 0.61 A. If the current of the memristor was $I_M < I_S$, which was defined as logic "0". If the current of memristor was $I_S \leq I_M$, which was defined as logic "1".

Table 2. The binary memory state of SBT-memristor.

Logic value	Current of memristor	Number of pulses
0	$I_M < 0.61$ A	2
1	0.61 A $\leq I_M$	4

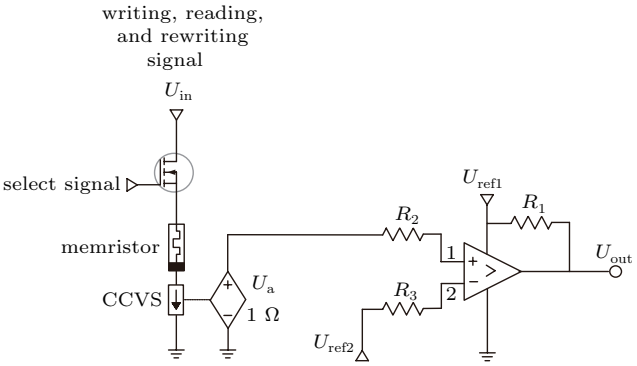


Fig. 3. The binary memory circuit based on an SBT-memristor.

3.3. Writing process of binary memory circuit based on an SBT-memristor

The change of memristor current during the writing process was shown in Fig. 4. In Fig. 4(a), writing signal was designed by the two pulses of 10 V amplitude and 60 Hz frequency. The current of memristor gradually increased and finally stabilized at about 0.57 A, which was the logic "0" state. In Fig. 4(b), writing signal was designed by the four pulses of 10-V amplitude and 60-Hz frequency. The current of memristor gradually increased and finally stabilized at about 0.73 A, which was the logic "1" state.

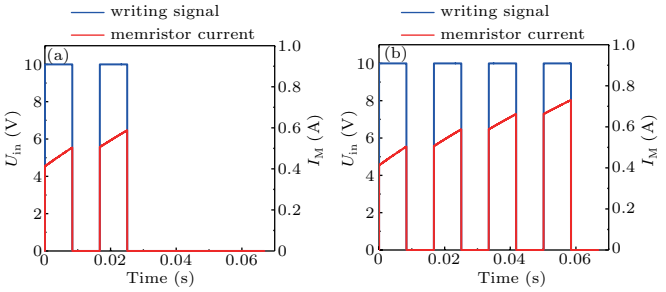


Fig. 4. The change of current value of memristor during different writing processes: (a) "0" signal; (b) "1" signal.

3.4. Reading process of binary memory circuit based on an SBT-memristor

Two pulses with opposite amplitudes and the same period were applied to the SBT-memristor, in other words, the total magnetic flux was 0, which did not change the state of the SBT-memristor. In Fig. 5, reading signal was designed by the two pulses with ±10-V amplitudes and 60-Hz frequency. In Fig. 5(a), the current of memristor gradually increased and finally stabilized at about 0.57 A, which was lower than I_S. As a result, reading process for logic "0" was realized. In Fig. 5(b), the current of memristor gradually increased and finally stabilized at about 0.73 A, which was higher than I_S. As a result, reading process for logic "1" was realized.

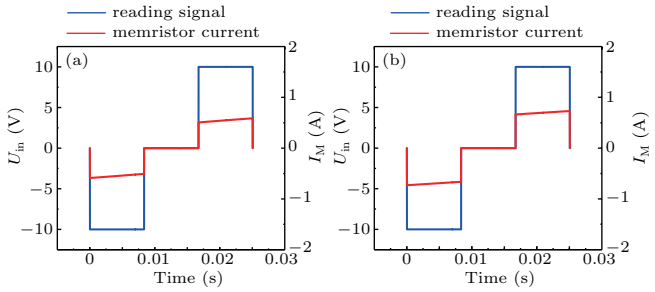


Fig. 5. The changes of memristor current when reading different logic signals: (a) "0" signal; (b) "1" signal.

3.5. Rewriting process of binary memory circuit based on an SBT-memristor

The rewriting process of the binary memory was shown in Fig. 6. If the memristor is in the "0" state, it can change into the "1" state by applying two pulses of 10-V amplitude and 60-Hz frequency, as shown in Fig. 6(a). If the memristor is in the "1" state, it can change into the "0" state by applying two pulses of −10-V amplitude and 60-Hz frequency, as shown in Fig. 6(b).

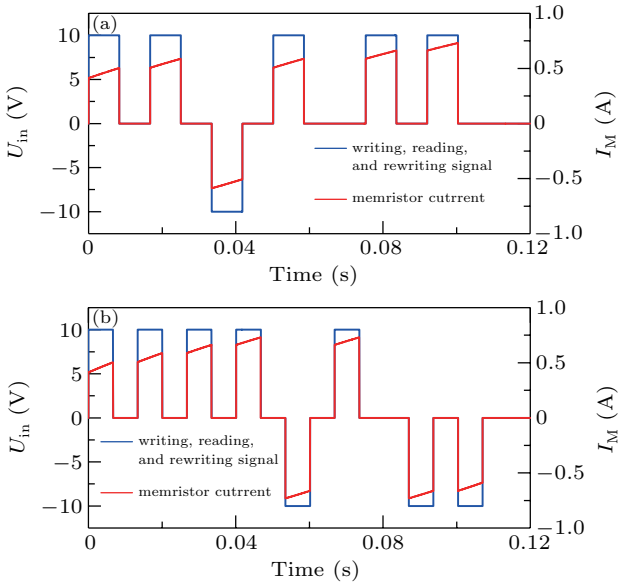


Fig. 6. (a) The process of rewriting "0" state to "1" state; (b) the process of rewriting "1" state to "0" state.

4. The multi-value memory circuit based on an SBT-memristor

4.1. The design of the SBT-memristor-based multi-value memory circuit

In Fig. 7, the multi-value memory circuit based on an SBT-memristor was designed. The circuit parameters were set as follows: $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R_9 = R_{10} = R_{11} = R_{12} = 1$ kΩ, $\beta = 1$ Ω, $U_{ref1} = 5$ V, $U_{ref2} = 0.45$ V, $U_{ref3} = 0.53$ V, $U_{ref4} = 0.61$ V, and $U_{ref5} = 0.69$ V.

We set the currents I_1, I_2, I_3, I_4 as $I_1 = 0.45$ A, $I_2 = 0.53$ A, $I_3 = 0.61$ A, and $I_4 = 0.69$ A. The memory state of SBT-memristor was defined in Table 3. If the current of memristor was $I_1 \leq I_M < I_2$, the memristor was in "00" state. If the current of memristor was $I_2 \leq I_M < I_3$, the memristor was in "01" state. If the current of memristor was $I_3 \leq I_M < I_4$, the memristor was in "10" state. If the current of memristor was $I_4 \leq I_M$, the memristor was in "11" state.

Table 3. The multi-value memory state of SBT-memristor.

ASCII	Current of memristor	Number of pulses
00	$0.45\ \text{A} \leq I_M < 0.53\ \text{A}$	1
01	$0.53\ \text{A} \leq I_M < 0.61\ \text{A}$	2
10	$0.61\ \text{A} \leq I_M < 0.69\ \text{A}$	3
11	$0.69\ \text{A} \leq I_M$	4

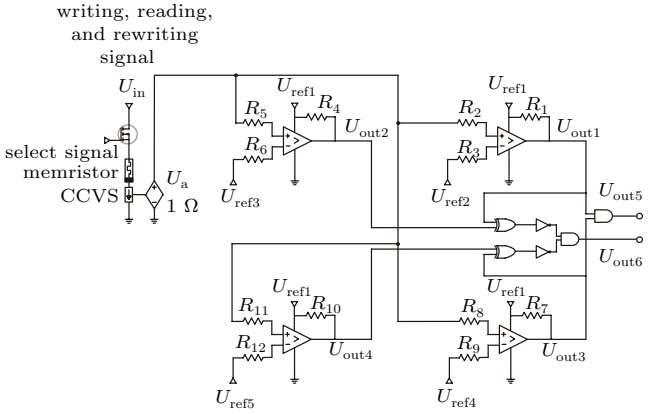


Fig. 7. The multi-value memory circuit based on an SBT-memristor.

4.2. Writing and reading process of multi-value memory circuit based on an SBT-memristor

The change of memristor current during the multi-value writing process was shown in Fig. 8. In Fig. 8(a), writing signal was designed by the one pulse of 10-V amplitude and 60-Hz frequency. The current of memristor gradually increased and finally stabilized at about 0.48 A, which was the logic "00" state. In Figs. 8(b)–8(d), writing signal was designed by the 2, 3, and 4 pulses of 10-V amplitude and 60-Hz frequency, respectively. The current of memristor gradually increased and finally stabilized at about 0.57 A, 0.64 A, and 0.73 A, which were the logic "01", "10", and "11" states, respectively.

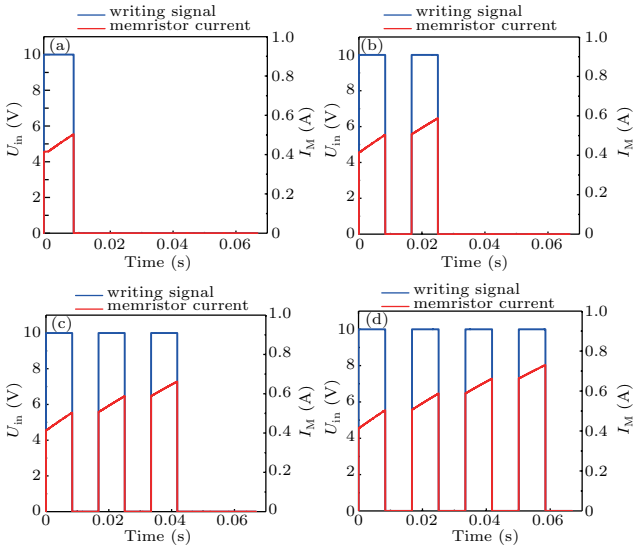


Fig. 8. The changes of current value of memristor when writing different logic signals: (a) "00" signal, (b) "01" signal, (c) "10" signal, and (d) "11" signal.

The reading process of multi-value memory circuit was similar as that of binary memory circuit, as shown in Fig. 9.

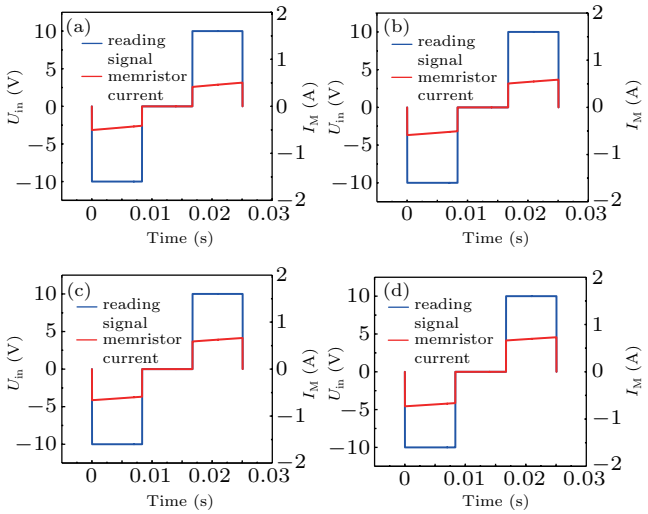


Fig. 9. The changes of memristor current when reading different logic signals: (a) "00" signal, (b) "01" signal, (c) "10" signal, and (d) "11" signal.

4.3. Rewriting process of multi-value memory circuit based on an SBT-memristor

In the multi-value memory circuit based on an SBT-memristor, the SBT-memristor can be changed from the existing memory state to another memory state by applying the corresponding positive or negative pulses. The processes of rewriting "00" state to other states, "01" state to other states, "10" state to other states, and "11" state to other states were shown in Figs. 10–13, respectively.

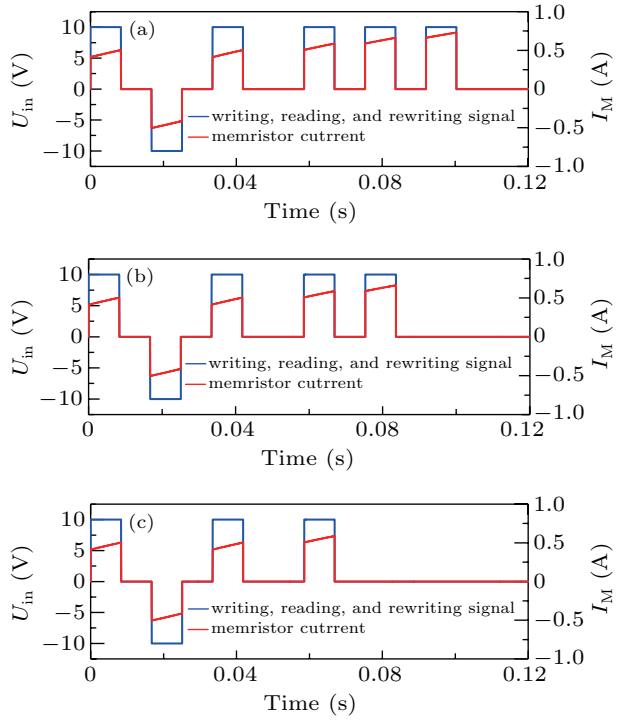


Fig. 10. (a) The process of rewriting "00" state to "11" state, (b) the process of rewriting "00" state to "10" state, and (c) the process of rewriting "00" state to "01" state.

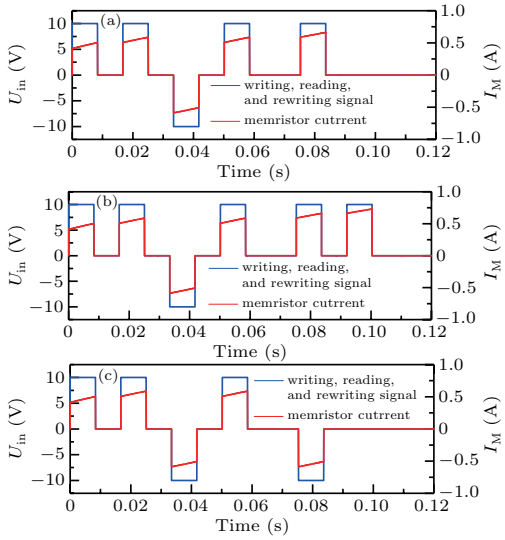


Fig. 11. (a) The process of rewriting "01" state to "10" state; (b) the process of rewriting "01" state to "11" state; (c) the process of rewriting "01" state to "00" state.

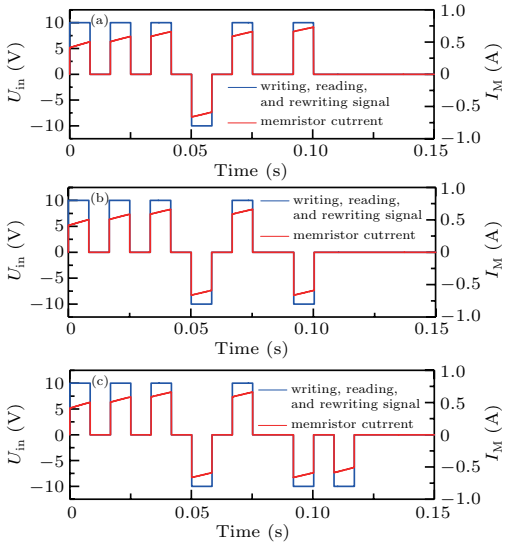


Fig. 12. (a) The process of rewriting "10" state to "11" state; (b) the process of rewriting "10" state to "01" state; (c) the process of rewriting "10" state to "00" state.

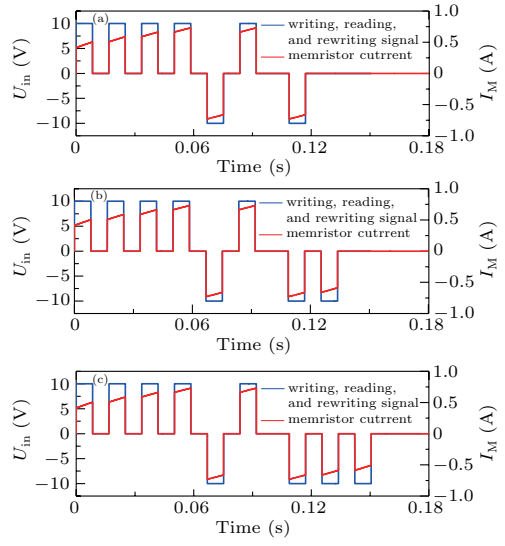


Fig. 13. (a) The process of rewriting "11" state to "10" state, (b) the process of rewriting "11" state to "01" state, and (c) the process of rewriting "11" state to "00" state.

5. The SBT-memristor-based crossbar memory circuit design

5.1. Design of the SBT-memristor-based crossbar binary memory circuit

The schematic diagram for the SBT-memristor-based 4×4 crossbar binary memory circuit was shown in Fig. 14. Each memristor in the array was controlled by writing, reading, rewriting, and column select signal. The writing and reading signals adopt the setting values in Figs. 4 and 5, and the relationship between the memristor current value and the memory state was shown in Table 2.

The results of SBT-memristor-based 4×4 crossbar binary memory circuit after writing and reading were shown in Fig. 15. This verified that the above-mentioned circuit can realize binary memory.

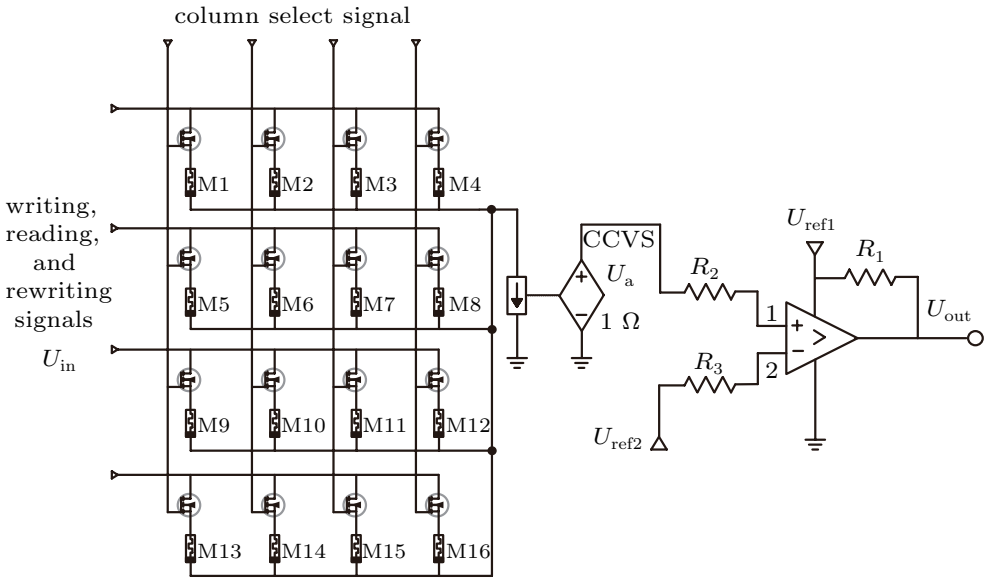


Fig. 14. The SBT-memristor-based 4 × 4 crossbar binary memory circuit.

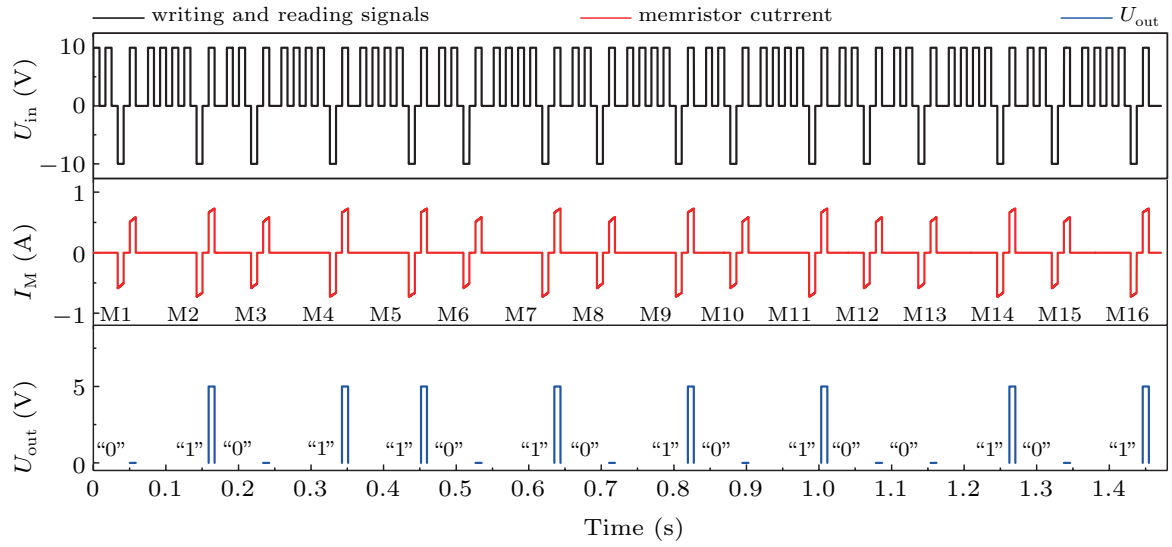


Fig. 15. The results of SBT-memristor-based 4 × 4 crossbar binary memory circuit.

5.2. Design of the SBT-memristor-based crossbar multi-value memory circuit

In Fig. 16, an SBT-memristor-based 4×4 crossbar multi-value memory circuit was designed. The writing and reading signals adopt the setting values in Figs. 8 and 9, and the relationship between the memristor current value and the memory state was shown in Table 3.

The results of SBT-memristor-based 4×4 crossbar multi-value memory circuit after reading/writing were shown in Fig. 17. U_{out5} and U_{out6} are the output voltages of logic value. The output voltages was 0 V or 5 V when the positive current of the memristor was in the setting range in Table 3. All the results verified that the above-mentioned circuit can realize multi-value memory.

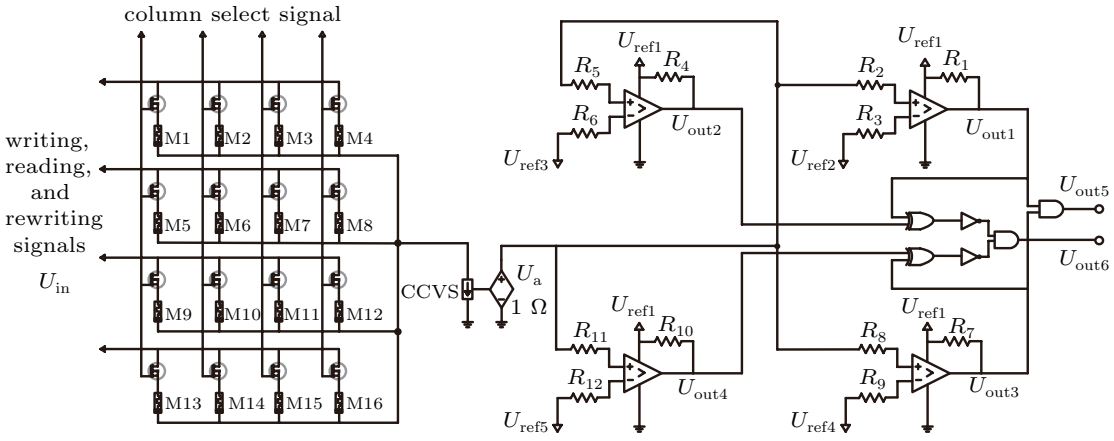


Fig. 16. The SBT-memristor-based 4 × 4 crossbar multi-value memory circuit.

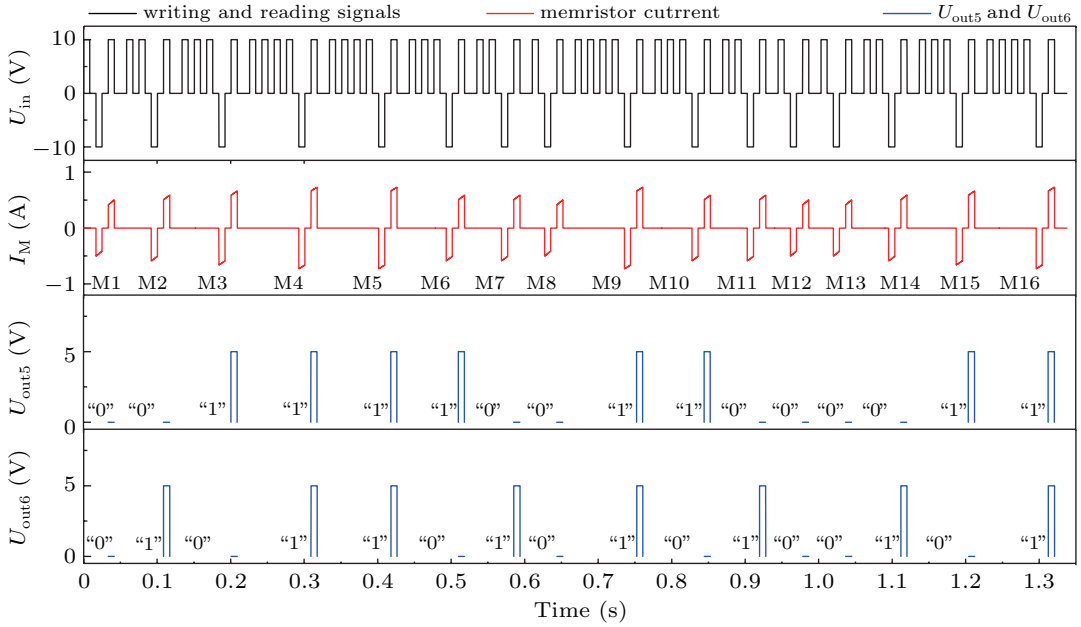


Fig. 17. The results of SBT-memristor-based 4 × 4 crossbar multi-value memory circuit.

5.3. Sneak-path current

In the SBT-memristor-based 4×4 crossbar multi-value memory circuit, when M1 and M5 were accessed and written into the "11" state, M2 and M6 were not accessed. The current change of M1, M2, M5, and M6 was shown in Fig. 18. We can get that even in the worst case the sneak current is 1.652 μA, which hardly affects the state of the memristor.

5.4. Comparison

Most memristive memory schemes have implemented binary memory.[36,37,41] Compared to multi-value memory, the binary memory does not have the advantages in memory density. In Ref. [38], an 8T1M memristor-based memory cell was presented to increase the density of memory. However, this memory cell required 9 elements to memory 3-levels, which losts its ascendency in integration density. The specific comparison is presented in Table 4.

Table 4. Comparison of different schemes.

	Number of transistors in each memory cell	Number of memristors in each memory cell	Memory bits in each memory cell	Memory density (related with the number of devices used and memory bits in each memory cell)
Ref. [36]	2	2	2	average
Ref. [37]	2	1	2	average
Ref. [38]	8	1	3	low
Ref. [41]	4	2	2	low
Here	1	1	4	high

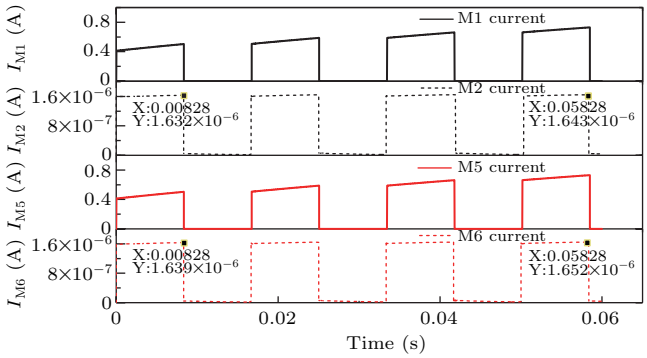


Fig. 18. The changes of M1, M2, M5, and M6 currents when M1 and M5 are accessed and written into the "11" state, M2 and M6 are not accessed.

5.5. Images memory using the SBT-memristor-based crossbar multi-value memory circuit

We divide the gray scale into four levels (gray scale 1, gray scale 2, gray scale 3, and gray scale 4) corresponding to the four states ("00" state, "01" state, "10" state, and "11" state) of the SBT-memristor-based multi-value memory, respectively, as shown in Fig. 19.

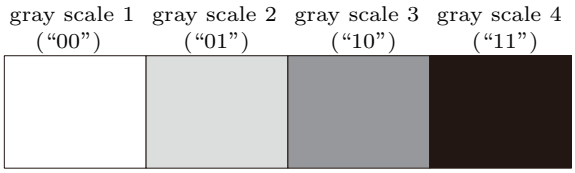


Fig. 19. The four levels of gray scale and its corresponding four states.

The schematic diagram of images memory using the SBT-memristor-based 8×8 crossbar multi-value memory circuit was shown in Fig. 20. In the image memory for the first time, we process the picture data into the writing signal, and change the memory state of the SBT-memristor through the writing signal.

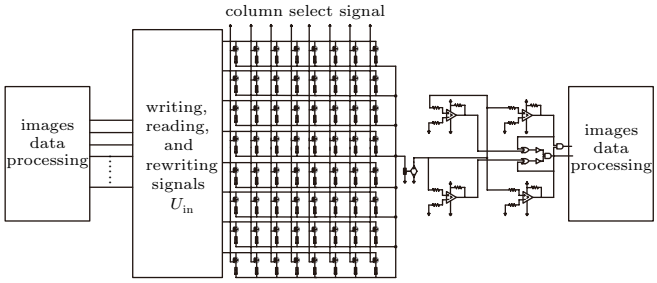


Fig. 20. The schematic diagram of images memory using the SBT-memristor-based 8×8 crossbar multi-value memory circuit.

We can obtain the memory data through the reading signal after accomplishing the writing process. In the image memory for the first time, the writing signal was shown in Figs. 21(a) and 21(b), the reading signal and the current change of the 8×8 SBT-memristor were shown in Figs. 21(c) and 21(d).

Next, we convert the data into image according to the order of writing and reading, as shown in Fig. 22.

Based on the state after the image memory for the first time, we rewrite the SBT-memristor-based 8×8 crossbar multi-value memory circuit. The rewriting signal was shown in Figs. 23(a) and 23(b), the reading signal and the current change of the 8×8 SBT-memristor were shown in Figs. 23(c) and 23(d).

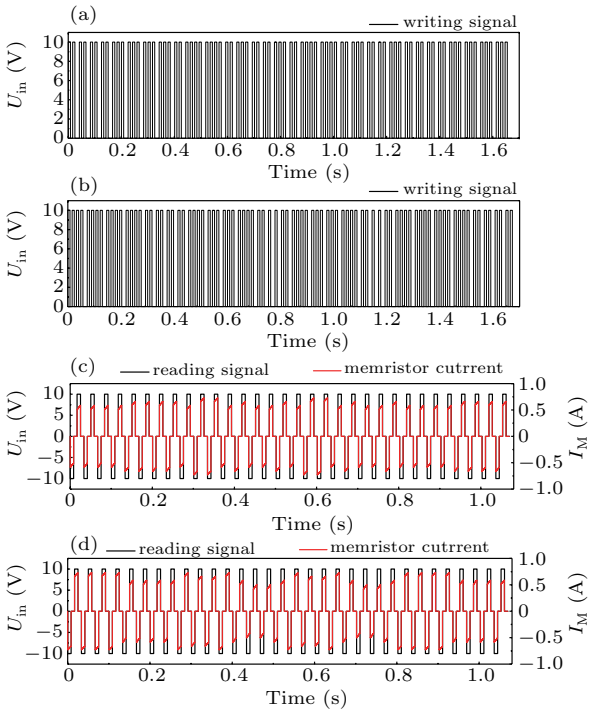


Fig. 21. (a) The writing signal of M1–M32, (b) the writing signal of M33–M64, (c) the reading signal and the current change of M1–M32, and (d) the reading signal and the current change of M33–M64.

(a)

(writing/ reading)1	(writing/ reading)2	(writing/ reading)3	(writing/ reading)4	.....	(writing/ reading)8
(writing/ reading)9	(writing/ reading)10	(writing/ reading)11	(writing/ reading)12	.....	(writing/ reading)16
(writing/ reading)17	(writing/ reading)18	(writing/ reading)19	(writing/ reading)20	.....	(writing/ reading)24
(writing/ reading)25	(writing/ reading)26	(writing/ reading)27	(writing/ reading)28	.....	(writing/ reading)32
⋮	⋮	⋮	⋮	⋮	⋮
(writing/ reading)57	(writing/ reading)58	(writing/ reading)59	(writing/ reading)60	.....	(writing/ reading)64

(b)

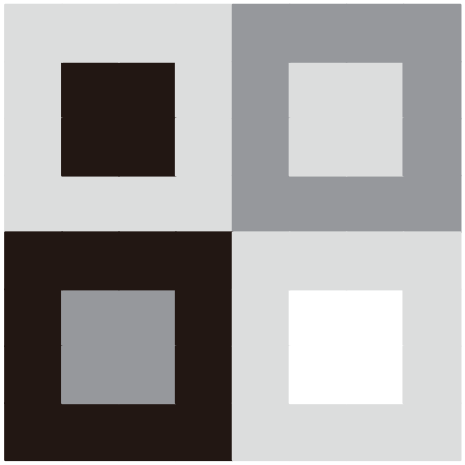


Fig. 22. (a) The order of writing and reading; (b) the image in the writing and reading for the first time.

We convert the data into image according to the order of rewriting and reading, as shown in Fig. 24.

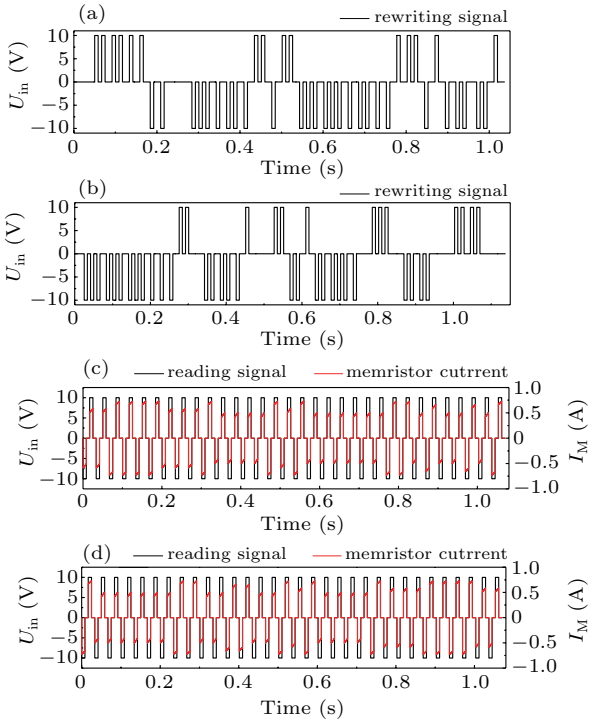


Fig. 23. (a) The rewriting signal of M1–M32, (b) the rewriting signal of M33–M64, (c) the reading signal and current change of M1–M32, and (d) the reading signal and current change of M33–M64.

(a)

(rewriting/ reading)1	(rewriting/ reading)2	(rewriting/ reading)3	(rewriting/ reading)4	.....	(rewriting/ reading)8
(rewriting/ reading)9	(rewriting/ reading)10	(rewriting/ reading)11	(rewriting/ reading)12	.....	(rewriting/ reading)16
(rewriting/ reading)17	(rewriting/ reading)18	(rewriting/ reading)19	(rewriting/ reading)20	.....	(rewriting/ reading)24
(rewriting/ reading)25	(rewriting/ reading)26	(rewriting/ reading)27	(rewriting/ reading)28	.....	(rewriting/ reading)32
⋮	⋮	⋮	⋮	⋮	⋮
(rewriting/ reading)57	(rewriting/ reading)58	(rewriting/ reading)59	(rewriting/ reading)60	.....	(rewriting/ reading)64

(b)

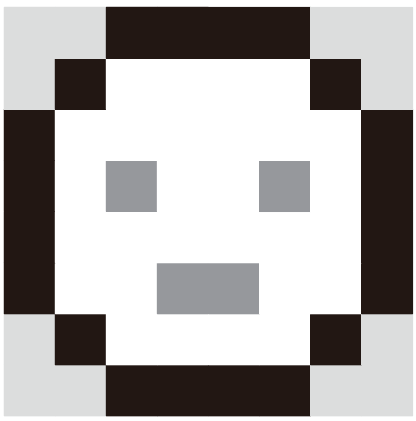


Fig. 24. (a) The order of rewriting and reading; (b) the image after rewriting and reading.

6. Conclusion

In this paper, an SBT-memristor-based SPICE model was established. The writing, reading, and rewriting processes of the binary and multi-value memory circuit were analyzed. Next, a novel SBT-memristor-based crossbar binary memory circuit was designed, accomplishing the binary memory. The crossbar multi-value memory circuit was proposed, which increased the memory density of SBT-memristor. Moreover, we verified the 4×4 crossbar binary and multi-value memory circuits through comprehensive simulations, and analyzed the sneak-path current and memory density. Finally, we use the SBT-memristor-based 8×8 crossbar multi-value memory circuits to complete the images memory.

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