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Effect of electrical contact on performance of WSe_2 field effect transistors*

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Two-dimensional (2D) transition metal dichalcogenides (TMDCs) such as tungsten diselenide (WSe_2) have spead many interesting physical properties, which may become ideal candidates to develop new generation electronic and opto-electronic devices. In order to reveal essential features of 2D TMDCs, it is necessary to fabricate high-quality devices with reliable electrical contact. We systematically analyze the effect of graphene and metal contacts on performance of multi-layered WSe_2 field effect transistors (FETs). The temperature-dependent transport characteristics of both devices are tested. Only graphene-contacted WSe_2 FETs are observed with the metal-insulator transition phenomenon which mainly attributes to the ultra-clean contact interface and lowered contact barrier. Further characterization on contact barrier demonstrates that graphene contact enables lower contact barrier with WSe_2 than metal contact, since the Fermi level of graphene can be modulated by the gate bias to match the Fermi level of the channel material. We also analyze the carrier mobility of both devices under different temperatures, revealing that graphene contact can reduce the charge scattering of the device caused by ionized impurities and phonon vibrations in low and room temperature regions, respectively. This work is expected to provide reference for fabricating 2D material devices with decent performances.

Keywords: two-dimensional materials, tungsten diselenide, metal-insulator transition, Schottky barrier, contact

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1. Introduction

Since the discovery of graphene in 2004, two-dimensional (2D) layered materials have been widely studied to develop next-generation electronics and optoelectornics, due to their premium electrical and optoelectrical properties.[1–4] However, as compared to traditional bulk semiconductors, performance of 2D material based devices is more easily affected by fabrication processes/techniques, because of their large surface-to-volume ratio and atomically thin thickness.[5,6] One of the key factors to ensure decent performance of 2D material devices is maintaining good electrical contact between the channel material and electrodes. Currently, 2D material based devices mainly use metal as the contact electrode, which usually involves e-beam lithography (EBL) and metal deposition processes. These fabrication processes inevitably introduce residues and/or defects to the crystal, leading to interface charge trapping and even Fermi level pinning effect.[7,8] Furthermore, Schottky barrier is highly likely to be formed due to the mismatch between the work function of metal electrode and the Fermi level of the channel material. Various methods have been proposed to optimize the contact between metal and the channel materials, such as choosing metals with appropriate work functions,[6,9] phase engineering,[10] using metal-insulator-semiconductor (MIS) structure,[11,12] and high temperature annealing.[13]

Besides metal contact, 2D graphene has also been used as contact electrodes for 2D material devices by stacking it on the channel material.[14,15] As a semi-metal, graphene possesses good conductivity and high carrier mobility to be a promising candidate for contact.[16] Meanwhile, the process of fabricating graphene contact is free of residues and defects, minimizing charge trapping and/or Fermi pinning effect. Consequently, 2D material based devices using graphene as contact may preferably present the intrinsic properties of channel materials. This is especially important to study the properties of TMDCs, which exhibit various excellent and interesting physical features.

One of the interesting characteristics observed in several TMDCs is the metal-insulator-transition (MIT) phenomenon,[7,8] which is still under active research to reveal its mechanism. Although it has many potential applications including resistive switching, ultrafast photocurrent switching and neuromorphic computation,[17,18] the MIT phenomenon can only be observed under certain strictly regulated conditions, and good electrical contact may be one of such conditions.

In this work, we fabricated the multi-layered WSe_2 FETs with graphene and Cr/Au as contacts, respectively, and systematically compared their performances. Both devices show ambipolar characteristics with the current on/off ratio greater

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than 10^6 at room temperature. However, only graphene-contacted device was observed with the MIT phenomenon. Furthermore, we analyze the transport characteristics of both devices under various temperatures to calculate the Schottky barrier height for the two types of contacts. As compared to metal-contacted devices, the graphene-contacted device has a much lower barrier height under appropriate gate voltage and higher field effect mobility. We finally investigate the effect of carrier scattering on the carrier field-effect mobility of both devices through temperature-dependent experiment. Our work may provide a fundamental insight into the effect of electrode contact on the performance of TMDCs based devices.

2. Experiments

2.1. Device fabrication

Multi-layered WSe_2 and graphene flakes were mechanically exfoliated by a piece of tape from their bulk crystals and then transferred onto a p-doped Si substrate covered with 285 nm thermally grown SiO_2.[19] The WSe_2 flakes were used as the channel material with thickness of around 9.2 nm. Graphene flakes and metal were used as electrodes to fabricate graphene-contacted and metal-contacted WSe_2 devices, respectively. Graphene contacts were made by stacking two graphene flakes on two opposite sides of a WSe_2 flake, which was then deposited with metal electrodes. The metal electrodes were defined by EBL, followed by depositing 10 nm Cr and 30 nm Au films sequentially on the WSe_2 flake using e-beam evaporation. Standard lift-off process was then performed to complete the metal electrode fabrication.

2.2. Sample characterization

The Raman spectra were obtained by a Renishaw InVia Raman microscope with incident laser intensity of ~1.38 mW at 532 nm. The thickness of these materials was characterized by an atomic force microscope (AFM) (Dimension Icon, Bruker, Germany) in tapping mode. The electrical characteristics of the WSe_2 devices were inspected by a semiconductor parameter analyzer B1500 (Agilent, USA). The low temperature electrical test environment was realized using the low temperature probe station of CRX-6.5K (Lake Shore, USA).

3. Results and discussion

Figures 1(a) and (b) show the schematic and optical image of the graphene-contacted WSe_2 device, respectively. All the WSe_2 flakes used in this work were mechanically exfoliated from the same bulk crystal, which were then transferred on SiO_2/Si substrates with a 285-nm-thick SiO_2 dielectric layer.

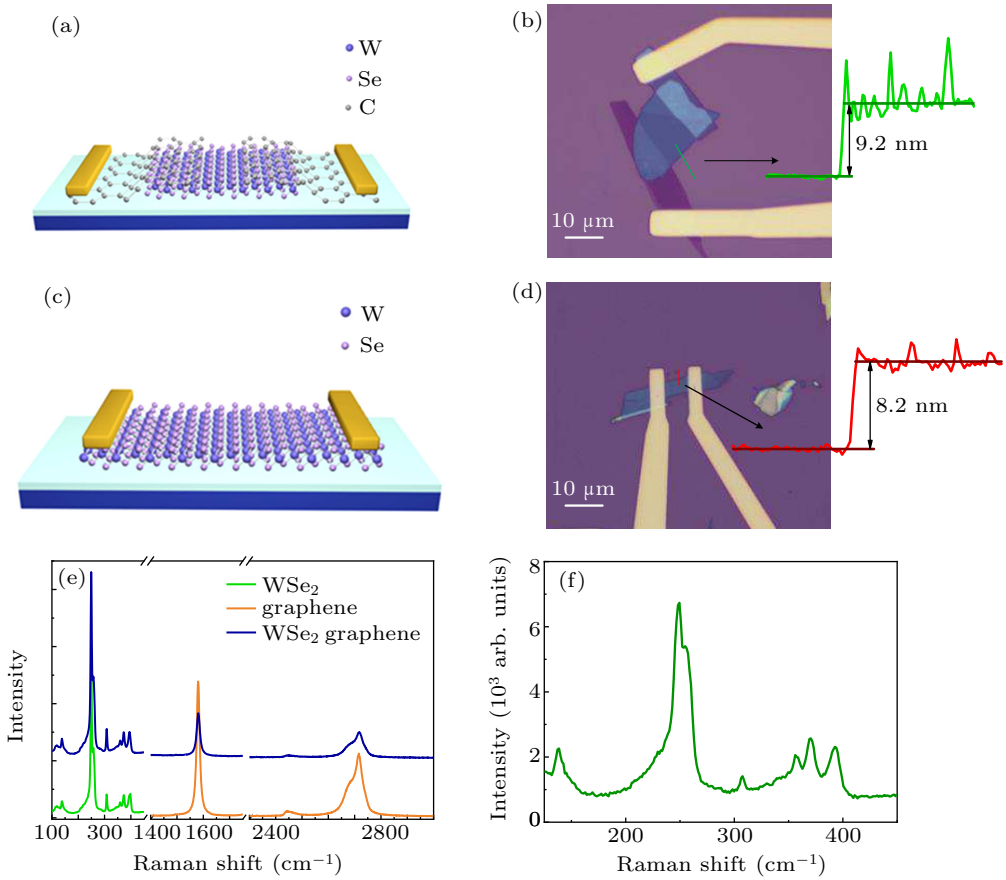


Fig. 1. Characterization of two devices with different contacts. (a) Schematic of the graphene-contacted WSe_2 device. (b) Optical image of the graphene-contacted WSe_2 device. Inset: the height profile of the WSe_2 measured along green line. (c) Schematic diagram of the Cr/Au-contacted WSe_2 device. (d) Optical image of the Cr/Au-WSe_2 FET. Inset: the height profile the WSe_2 measured along red line. (e) Raman spectra of WSe_2 (green line), graphene (orange line) and the overlapped region (blue line) for the graphene-contacted WSe_2 device. (f) Raman spectra of the WSe_2 for Cr/Au-WSe_2 FET.

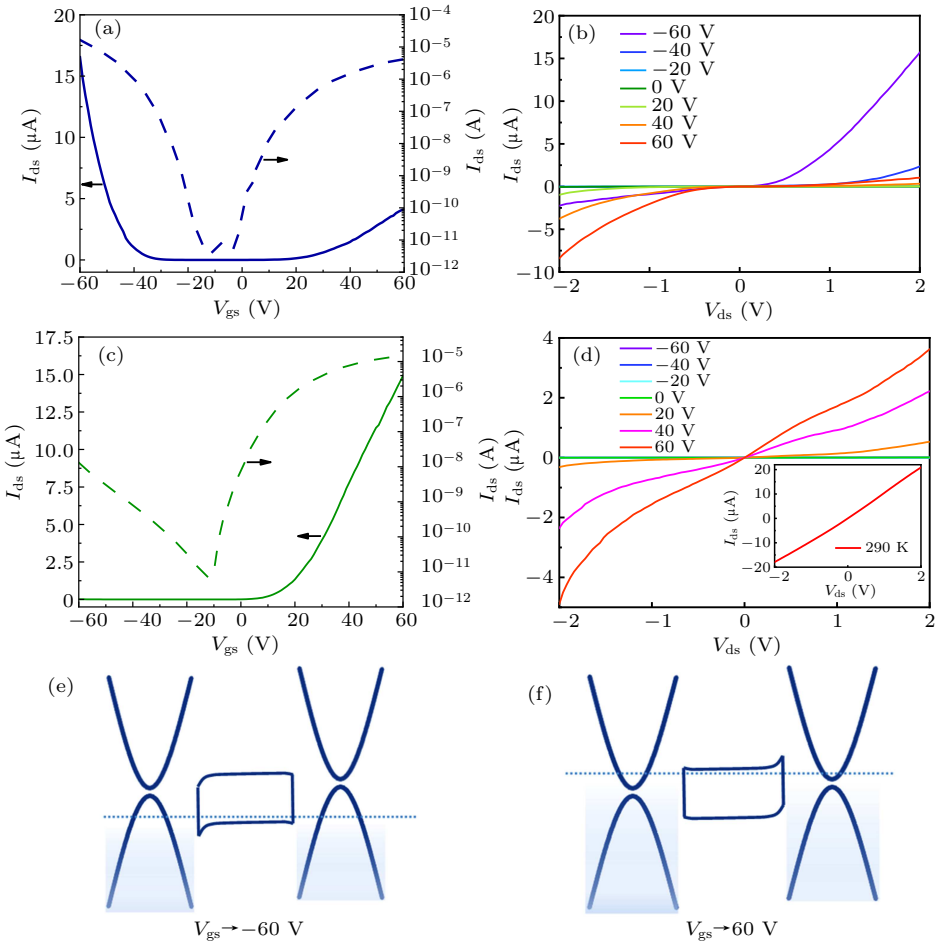


Fig. 2. Electrical characterization of graphene- and metal-contacted WSe_2 devices. Transfer curves of (a) graphene-contacted and (c) Cr/Au-contacted WSe_2 FETs in linear (solid line) and logarithm (dashed line) scales. Output curves of (b) graphene-contacted and (d) Cr/Au-contacted WSe_2 FETs under different V_{gs} as V_{ds} sweeps from −2 V to 2 V. Inset: the output curve of the Cr/Au-contacted WSe_2 FET in vacuum at room temperature. [(e), (f)] Band alignment of the graphene-contacted WSe_2 device at different gate potentials.

To fabricate graphene-contacted WSe_2 FET, two graphene flakes were transferred onto two sides of the WSe_2 flake to form van der Waals contacts, which served as the source and drain electrodes. Cr/Au was then deposited on the graphene flakes to connect to the test terminals. The gate voltage was applied through heavily doped Si substrate as back-gate electrode. The thickness of the WSe_2 flake and two graphene flakes were measured to be 9.2 nm, 11.6 nm and 5.4 nm, respectively, by AFM. Figure 1(e) shows the Raman spectra of WSe_2 (green line), graphene (orange line) and WSe_2/graphene overlapped region (blue line), in which characteristic Raman peaks of WSe_2 and graphene were observed and consistent with previously reported results.[20,21] Figures 1(c) and 1(d) are the schematic and optical image of Cr/Au-contacted WSe_2 FET, respectively. The fabrication of Cr/Au-contacted WSe_2 FET was the same as the process of making graphene-contacted WSe_2 FET, except that no graphene flakes were stacked on WSe_2. The AFM height profile identified the thickness of the WSe_2 flake to be 8.2 nm. Figure 1(f) presents the Raman spectrum of the WSe_2 used in the Cr/Au-contacted device, in which the characteristic peak positions were perfectly consistent with the previous reports.[21]

Figures 2(a)–2(d) present the transfer and output characteristics of graphene- and Cr/Au-contacted WSe_2 devices, respectively. The transfer curve of the graphene-contacted device under V_{ds} bias of 2 V is shown in both linear (solid line) and logarithm (dashed line) scales in Fig. 2(a). As gate voltage swept from −60 V to 60 V, the device exhibits ambipolar behavior, with I_{on} around 16.5 μA at −60 V and I_{on}/I_{off} ratio more than 10^6. Figure 2(b) shows the output curve of the same device in Fig. 2(a) under different V_{gs} as V_{ds} sweeps from −2 V to 2 V. The output curves are highly asymmetric, which attributes to the asymmetric heterojunction formed at the interface of graphene and WSe_2. Since van der Waals contacts can minimize interface defects and charge traps, the current value in output curve matches the current value in the transfer curve under the same biases V_{gs} and V_{ds}. Figures 2(e) and 2(f) illustrate the band alignment of the graphene-contacted WSe_2 device under gate bias of −60 V and +60 V. Specifically, when a high negative gate potential is applied, the work function of graphene and the Fermi level of WSe_2 shift to the valence band, which induces the band bending making the relative Schottky barrier height lower. As a result, holes can be

injected into the valence band more easily. Conversely, the graphene work function and the Fermi level of WSe_2 are modulated in opposite directions under high positive gate voltage. Under this condition, the Fermi level of WSe_2 is close to the conduction band, and the small barrier height helps electron injection. On the other hand, the transfer curve of the metal-contacted WSe_2 FET is shown in Fig. 2(c), which was obtained under the same ambient conditions. As compared to the graphene-contacted device, this device also shows ambipolar behavior and on-off ratio greater than 10^6 with I_{on} around 14.9 μA at 60 V gate bias. The output curve of this FET is shown in Fig. 2(d), which becomes more symmetric than the curves obtained from graphene-contacted FET. Nevertheless, discrepancy in I_{ds} is observed under the same V_{gs} and V_{ds} biases between the output and the transfer curves. This is ascribed to the hysteresis characteristics of the device caused by charge trap and release at the interface between metal and channel material, which can be suppressed in a vacuum. The inset in Fig. 2(d) shows the output characteristics measured under 60 V gate bias in vacuum at room temperature, which can well match the current in transfer characteristics as gate voltage sweeps to 60 V. The dimension-dependent electrical performance of the WSe_2 device should also be considered. Regarding to the thickness, single-layer and multi-layer WSe_2 have direct and indirect band gap, respectively, which have differences in electron-hole recombination and luminous efficiency. Moreover, as compared to the devices made of single-layer WSe_2, devices made of multi-layer WSe_2 show statistically higher mobility.[22] In this article, all the WSe_2 flakes are multi-layer with similar thicknesses of several nanometers to minimize the impact of thickness on the electrical performance. Meanwhile, the shape and size of the WSe_2 devices between electrodes are square ranging from tens of square microns to hundreds of square microns. In the following experiment, we use the carrier mobility as a key parameter to characterize the device electrical performance, which normalizes the influence of the channel size.

To investigate the contact mechanism, the temperature-dependent transfer curves of the graphene-contacted WSe_2 device in both linear (solid line) and logarithm (dashed line) scales are presented in Fig. 3(a). Generally, the device has higher I_{ds} value and on/off ratio compared to the result in Fig. 2(a). Since the temperature-dependent tests were carried out in a vacuum chamber, the adsorption of charge accepters such as water vapor and oxygen was inhibited. In addition, the channel current of the device changed differently with temperature, when the gate was negatively and positively biased. Specifically, the I_{ds} decreased with increasing temperature when the gate voltage was negative, indicating a typical metallic state. In contrast, when the gate voltage was positive, the I_{ds} increased with increasing temperature, corresponding to an insulating state. This phenomenon indicates the presence of MIT in this device. Figure 3(b) presents the conductance G of the device as a function of temperature under different gate biases extracted from Fig. 3(a). We can clearly observe that in the metal phase region, the conductance decreases as the temperature increases, while in the insulating phase the conductance increases with temperature increases. The inset of Fig. 3(b) shows the locally enlarged view of conductance under different positive gate voltages.

On the contrary, the MIT phenomenon was not observed in metal-contacted WSe_2 devices. Figure 3(c) shows the temperature-dependent transfer characteristics of the Cr/Au-contacted WSe_2 FET. When the gate voltage sweeps from −60 V to 60 V, the I_{ds} increases as the temperature increases, showing the traditional semiconducting behavior. From Fig. 3(c), the conductance of the device as a function of temperature under different gate voltages is extracted and plotted in Fig. 3(d). As compared with Fig. 3(b) (graphene-contacted WSe_2 FET), the conductance of the metal-contacted WSe_2 FET increases with the temperature, regardless of the variation of gate bias. This may be due to the fact that the MIT phenomenon can be easily screened by the influence of the Schottky barrier at the contact interface between metal and channel material.

In order to verify this point of view, we calculate the Schottky barriers of these two structures under different gate biases. When 2D thermionic emission dominates the transport behavior of 2D devices, the following equation can be used to describe the process:

$$I_{ds} = A^*_{2D} T^{3/2} \cdot \exp\left(\frac{q\Phi_B}{k_B T}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{k_B T}\right)\right], \quad (1)$$

where $A^*_{2D} = 4\pi q m^* k_B^2 h^{-3}$ is the 2D equivalent Richardson constant, m^* is the effective mass, h is Planck's constant, T is the absolute temperature, q is the elementary charge, Φ_B is the Schottky barrier height, and k_B is the Boltzmann constant, V_{ds} is 2 V. We then draw the Arrhenius plot and linearly fit it to derive the Schottky barrier height according the equation. Figures 4(a) and 4(b) plot the linear fit of $\ln(I_{ds}/T^{3/2})$ versus $1000/T$ at negative back-gate voltage and positive back-gate voltage for the graphene-contacted device, respectively. The good agreement of the experimental data with the fitting curve means that the carrier transport follows the thermally activated model. Moreover, the slope of the fitting curves in the Arrhenius plot indicates the phase of the device: positive slope indicates metallic phase, while negative slope corresponds to insulating phase. In addition, as the gate voltage sweeps from −60 V to 60 V, the absolute value of the slope of the fitting curve first increases and then decreases. Based on the same electron thermionic emission model, Figs. 4(c) and 4(d) show the Arrhenius plot and linear fitting results of the

Cr/Au-contacted WSe_2 FET under different gate biases. Different from the graphene-contacted device, the slopes of the fitting curves for the Cr/Au-contacted WSe_2 FET are all positive under both negative and positive gate biases, indicating insulating property. However, it is similar to the graphene-contacted device that the slope of the fitting curves reaches the maximum value within V_{gs} sweeping from −60 V to 60 V. According to the slope of each fitting line, we extract the effective Schottky barrier heights of the graphene-contacted and Cr/Au-contacted WSe_2 FETs as a function of gate bias, which are presented in Figs. 4(e) and 4(f), respectively. Obviously, the effective Schottky barrier heights of both the devices are tunable by the gate voltage, which decrease as the amplitude of the gate voltage increases. The barrier-gate voltage curves for both graphene-contacted and Cr/Au-contacted devices can be divided into two branches. In the left branch of the curves (under negative gate bias), the majority carriers are holes, while in the right branch of the curves the majority carriers are electrons. Furthermore, the electrical transport in the linear part of each branch is dominated by the thermal emission. When the tunneling current is not negligible, the curve will deviate from the linear region. We fit the linear parts of the two branches of the two curves and extract the Φ_B at the demarcation point of the linear fit and nonlinear part. For the graphene-contacted device corresponding to Fig. 4(e), the barrier heights of the electron and hole are 43 meV and 65 meV, respectively. In contrast, for the metal-contacted FET in Fig. 4(f), the barrier heights are 155 meV and 162 meV for electron and hole, respectively. Therefore, contact barrier between graphene and WSe_2 is much lower than that between Cr/Au and WSe_2, resulting in the observable MIT phenomenon.

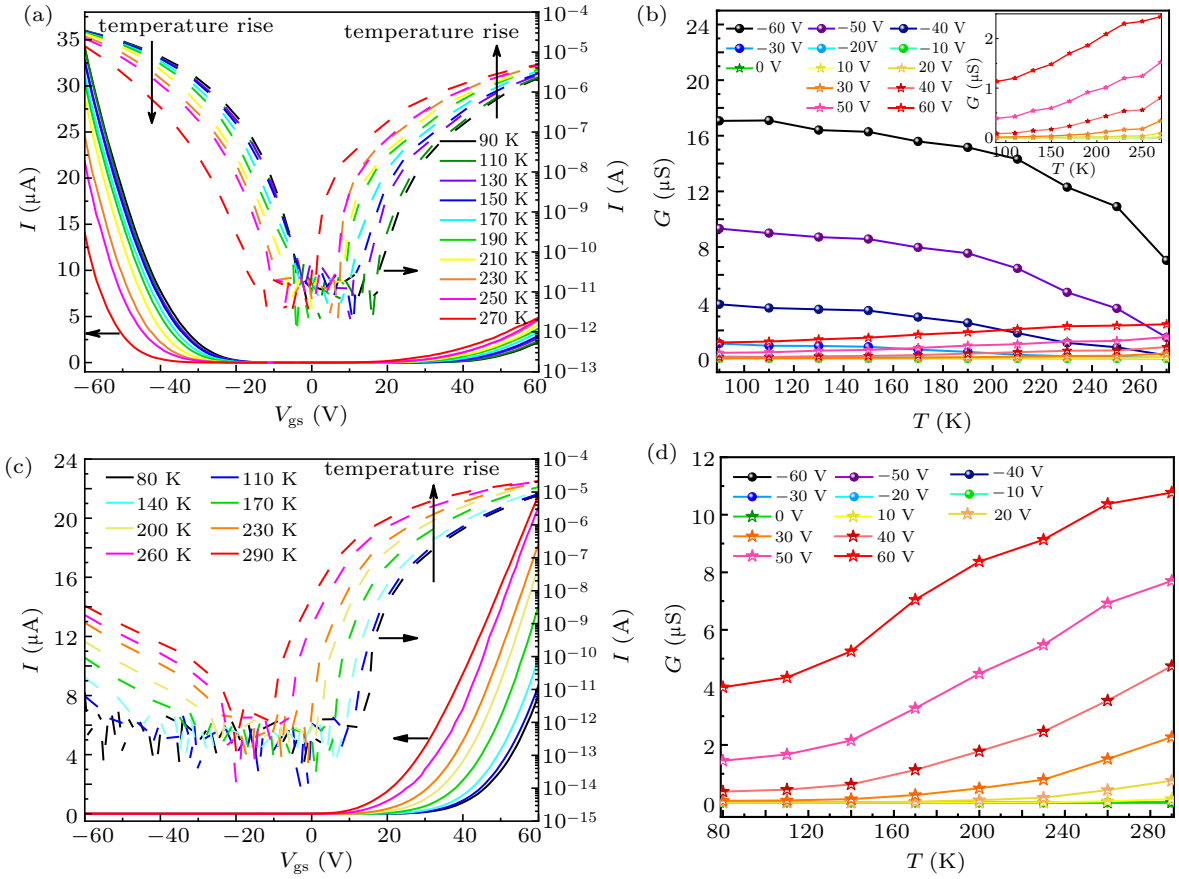


Fig. 3. Temperature-dependent electrical properties of graphene- and metal-contacted WSe_2 devices. (a) Temperature-dependent transfer curve of the graphene-contacted WSe_2 device. (b) Conductance versus temperature curve of the graphene-contacted WSe_2 device. Inset: a locally enlarged view of conductance versus temperature curve under different positive gate voltages. (c) Temperature-dependent transfer and (d) conductance curves of the Cr/Au-contacted WSe_2 FET.

Since reducing the height of the contact barrier facilitates charge transport, we further explore the influence of graphene contact on the electrical properties of the device from the perspective of carrier mobility. We calculate the field-effect mobility according to the following formula:

$$\mu = \frac{\mathrm{d}I_{ds}}{\mathrm{d}V_{gs}} \times \frac{L}{WC_iV_d}, \tag{2}$$

where μ is the field-effect mobility, L and W are the channel length and width, respectively, $C_i = \varepsilon_0\varepsilon_r/d$ is the capacitance between the channel and the back gate (ε_0 is the permittivity in vacuum, ε_r is 3.9 for SiO_2 and d is the thickness of the dielectric layer of 285 nm). We derive the carrier field-effect mobility as a function of temperature for the graphene-contacted and Cr/Au-contacted WSe_2 devices in Figs. 5(a) and 5(b),

respectively. In the entire temperature range, the graphene-contacted device has higher carrier mobility than the metal-contacted device, further indicating the optimization of electrical performance by graphene contact. Meanwhile, the difference in mobility at different temperatures give us insight into the mobility-limiting scattering mechanism. The experimental limitation of field-effect mobility is usually caused by the presence of scattering sources and disorder. In the low temperature region, the mobility is mainly affected by the contact resistance and the charge impurity scattering. For the graphene-contacted WSe_2 device, the mobility is relatively stable under 200 K, which means that no significant degradation is caused by charge scattering. However, for the Cr/Au-contacted WSe_2 device, the mobility decreases with the decreasing temperature in the low temperature range. In this situation, the scattering probability caused by ionized impurities increases with the decrease of temperature, and as a result, the carrier mobility also decreases with temperature leading to deterioration of device performance. On the other hand, in the phonon limited region, the carrier mobility decreases with increasing temperature due to the increased number of phonon modes, which fits the expression $\mu = T^{-\gamma}$. The positive power-law correlation is consistent with the performance of other materials, which demonstrates that the phonon scattering mechanism is satisfied.[7,23] The exponent γ indirectly reflects the effect of the phonon limitation, which is 2.21 and 0.93 for the graphene-contacted and Cr/Au-contacted WSe_2 devices, respectively. Although it degrades faster in the region dominated by phonon scattering, the carrier mobility of the graphene-contacted WSe_2 device maintains a value higher than that of the Cr/Au-contacted WSe_2 device.

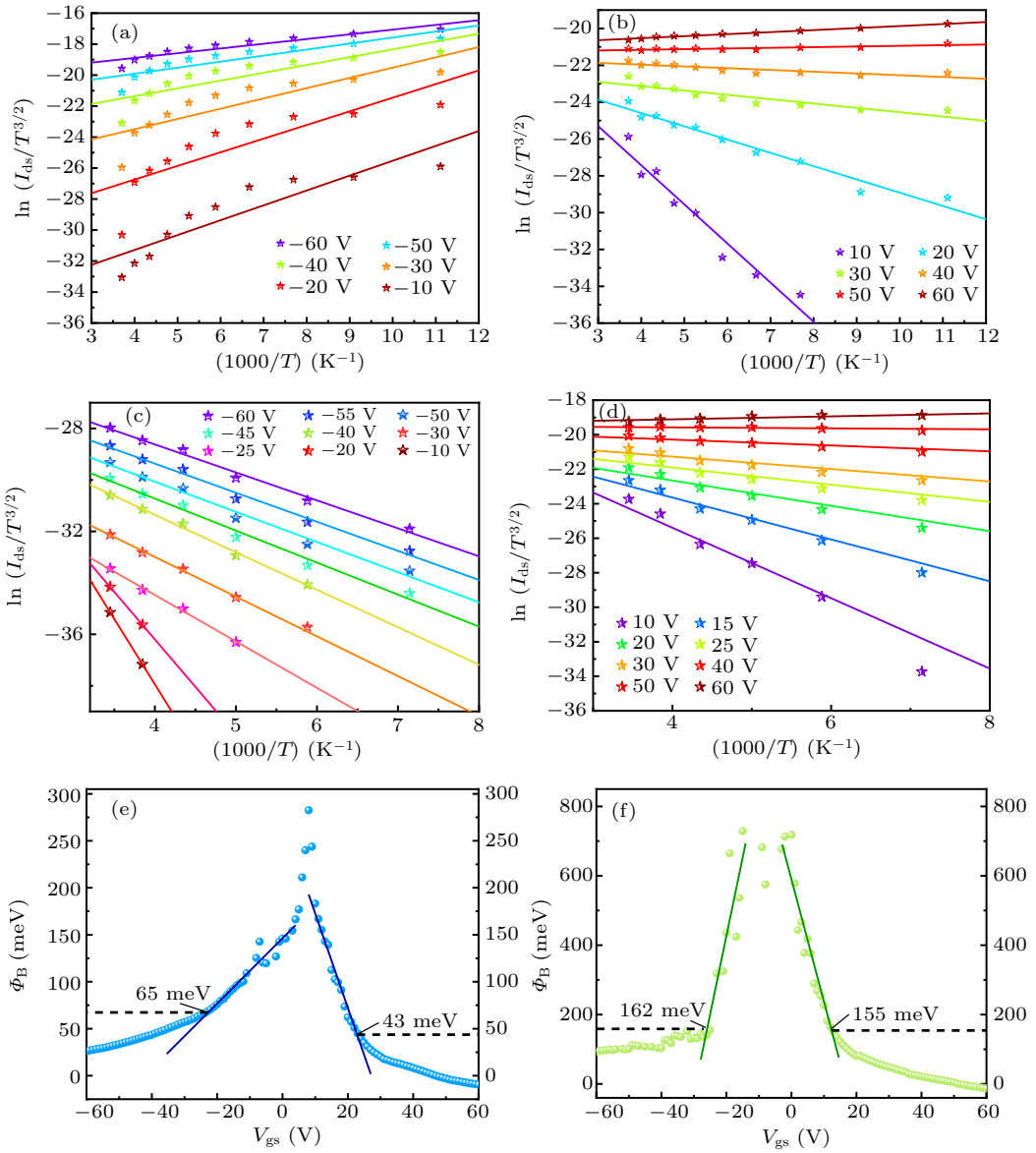


Fig. 4. Arrhenius plots and Schottky barrier of graphene- and metal-contacted WSe_2 devices. [(a), (b)] The linear fit of $\ln(I_{ds}/T^{3/2})$ versus $1000/T$ at negative (a) and positive (b) back-gate voltage for the graphene-contacted device. [(c), (d)] The linear fit of $\ln(I_{ds}/T^{3/2})$ versus $1000/T$ at negative (c) and positive (d) back-gate voltage for the Cr/Au-contacted device. [(e), (f)] Effective Schottky barrier height as a function of gate bias for the graphene-contacted (e) and Cr/Au-contacted (f) FETs.

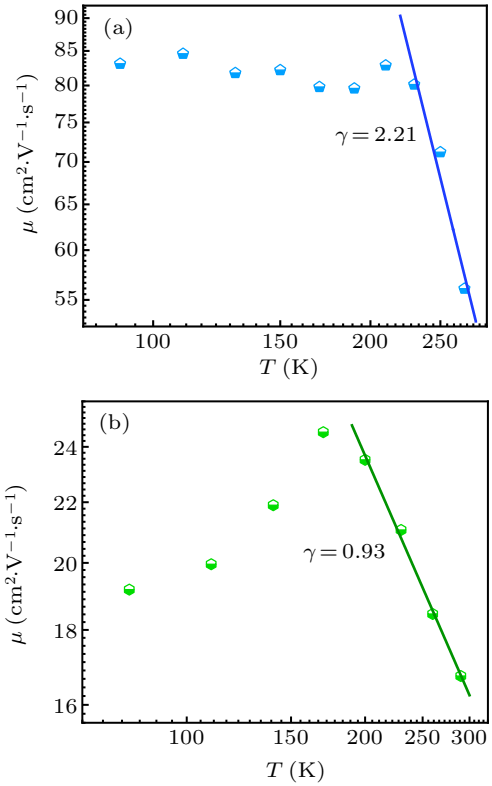


Fig. 5. Carrier mobility as a function of temperature in the logarithmic scale for (a) the graphene-contacted and (b) Cr/Au-contacted devices.

In general, the graphene-contacted WSe_2 device shows better performance than the metal-contacted device due to two reasons. From the perspective of device fabrication, there are no dangling bonds on the surface of two-dimensional materials, and the graphene and WSe_2 are combined by van der Waals force to avoid the defects and residues caused by EBL and metal deposition. The defects at the interface between WSe_2 and metal are expected to affect the Schottky barrier. Firstly, defects may prevent good physical contact, and thus, electrical contact between WSe_2 and metal. Secondly, the conventional method to form near-ohmic contact between a semiconductor and a metal is to heavily dope the semiconductor, so that electrons can easily tunnel through the contact barrier. The defects may induce defect states and affect the doping level of WSe_2. The metal deposition process inevitably induces defects on the WSe_2 surface, resulting in the change of the Schottky barrier. Therefore, graphene contact to WSe_2 can create a more controllable and cleaner interface than metal contact. In addition, the Fermi level of graphene contacts can be effectively modified by the back-gate voltage to match the Fermi level of WSe_2, so that the contact barrier between graphene and WSe_2 is significantly reduced and carrier mobility is thus increased.

4. Conclusion

In summary, we have fabricated the WSe_2 FETs with graphene and Cr/Au as contact electrodes, respectively, to analyze the effect of contact on device performance. In our experiments, only the graphene-contacted device is observed with the MIT phenomenon, which may be attributed to its ultraclean contact interface and low contact barrier. In detail, the contact barriers of the graphene-contacted device for electrons and holes are as low as 43 meV and 65 meV, respectively, which are significantly lower than the values of the metal-contacted FET (155 meV for electrons and 162 meV for holes). We also analyze the influence of carrier scattering on the device transport behavior under different temperatures, indicating that graphene contact reduces the charge scattering of the device caused by ionized impurities and phonon vibrations in low and room temperature regions, respectively. Our work may provide important reference for further development of high-performance 2D material based electronic devices.

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