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Enhanced interface properties of diamond MOSFETs with Al_2O_3 gate dielectric deposited via ALD at a high temperature*

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The interface state of hydrogen-terminated (C–H) diamond metal–oxide–semiconductor field-effect transistor (MOSFET) is critical for device performance. In this paper, we investigate the fixed charges and interface trap states in C–H diamond MOSFETs by using different gate dielectric processes. The devices use Al_2O_3 as gate dielectrics that are deposited via atomic layer deposition (ALD) at 80 °C and 300 °C, respectively, and their *C*–*V* and *I*–*V* characteristics are comparatively investigated. Mott–Schottky plots ($1/C^2$–V_G) suggest that positive and negative fixed charges with low density of about 10^{11} cm^{-2} are located in the 80-°C- and 300-°C deposition Al_2O_3 films, respectively. The analyses of direct current (DC)/pulsed *I*–*V* and frequency-dependent conductance show that the shallow interface traps (0.46 eV–0.52 eV and 0.53 eV–0.56 eV above the valence band of diamond for the 80-°C and 300-°C deposition conditions, respectively) with distinct density (7.8×10^{13} $eV^{-1}\cdot cm^{-2}$–8.5×10^{13} $eV^{-1}\cdot cm^{-2}$ and 2.2×10^{13} $eV^{-1}\cdot cm^{-2}$–5.1×10^{13} $eV^{-1}\cdot cm^{-2}$ for the 80-°C- and 300-°C-deposition conditions, respectively) are present at the Al_2O_3/C–H diamond interface. Dynamic pulsed *I*–*V* and capacitance dispersion results indicate that the ALD Al_2O_3 technique with 300-°C deposition temperature has higher stability for C–H diamond MOSFETs.

Keywords: diamond MOSFET, ALD temperature, pulsed *I*–*V*, interface trap, conductance method

PACS: 81.05.ug, 85.30.Tv, 85.30.De **DOI:** 10.1088/1674-1056/abd749

1. Introduction

The ultra-wide band gap semiconductor diamond, due to its superior material properties, is considered to be a remarkable candidate for high-power and high-frequency applications.[1–3] Hydrogen-terminated (C–H) diamond, which has a negative electron affinity, forms a two-dimensional hole gas (2DHG) surface channel regardless of how high the activation energy associated with p-type dopants is.[4] The conduction of the C–H diamond surface can be realized by exposing it to the air adsorbates or overcoating it with different oxides such as Al_2O_3 and transition metal oxides (TMO). For these oxide materials, the empty electron states below diamond's valence band maximum (VBM) capture the electrons in the diamond surface, which results in the upward band bending of VBM and the formation of the 2DHG layer.[2] Compared with high electron affinity insulators and other high-*k* oxides,[5] Al_2O_3 forming by atomic layer deposition (ALD) is considered as a promising gate insulator and passivation layer for perusing high-performance C–H diamond MOSFETs.[6–9] Even so, the stability of device operation is still a critical limitation for the Al_2O_3-based C–H diamond FETs.[10] Theoretically, there are no surface states in a complete C–H diamond surface due to non-existence of dangling bonds. For this reason, there has not been made much effort devoted to the interface trap issues in C–H diamond. As a matter of fact, the gate dielectric Al_2O_3 deposition condition can give rise to the traps at the interface. The trap-induced DC-RF dispersion in diamond microwave device can restrict the available current and output power of diamond MOSFETs.[11] Interface traps have been investigated for diamond MOSFETs with ALD Al_2O_3 deposited below 200 °C.[12] However, the understanding of the Al_2O_3/C–H interface behavior for Al_2O_3 deposited at even higher temperatures is still limited.

Since the C–H bonds and adsorbates generating holes are sensitive to factors such as environment and heat, the quality of the Al_2O_3 films deposited at different temperatures[13] and their relevant transistor behaviors have been reported.[14] In fact, the bond enthalpy of C–H is higher than those of C–C and C–O,[15] which means that the C–H bond itself is quite stable. For the surface adsorbates, Al_2O_3 deposited at 80 °C proved to be an effective solution to preserve air adsorption.[8] However, it was shown that the adsorbate desorption occurs

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even at moderate temperatures (< 200 °C).[16] Notably, it was reported that a high-temperature (450 °C) ALD process could also induce surface p-type conduction after the removal of air adsorbates, during which the surface holes were regenerated by the negative fixed charges in Al_2O_3.[7,9] But the thin 450-°C deposition Al_2O_3 film is difficult to preserve new origins of hole accumulation,[17] it may limit the further development of the corresponding diamond MOSFETs in the high-frequency application, where high aspect-ratio is required.[18] Recently, the band offset of the 300-°C Al_2O_3 depositing on C–H diamond claimed that this condition could also induce the p-type diamond conduction,[19] thus it is expected to achieve high output-current diamond devices using the thin 300-°C ALD grown Al_2O_3. Up to now, the significant interface properties of the C–H diamond MOSFETs with or without air adsorbates have not been unveiled. In this paper, we find that the fixed charges in Al_2O_3 films are much lower than the 2DHG density. Our DC/pulsed *I*–*V* and frequency-dependent conductance measurements show that the interface trap states of the C–H diamond MOSFETs can be effectively suppressed at 300 °C for ALD-Al_2O_3 deposition in comparison with those deposited at 80 °C, which indicates that the ALD deposition temperature is sufficiently high to achieve a high-quality interface for C–H diamond.

2. Device fabrication and characterization

The C–H diamond MOSFETs were fabricated on (100)-oriented type-IIa commercial diamond substrates. The substrates were prepared by using a strong acid solution (HNO_3/H_2SO_4), and the purpose of this process is to remove the nondiamond phase.[1] The surface hydrogen-termination was realized by exposing the diamond surface to hydrogen plasma at 850 °C for 20 min. Then, the samples were exposed to the air for a few hours to induce a high conductive 2DHG channel in the diamond surface. The gold (Au) metals were evaporated to protect the C–H diamond surface, afterwards, the metals covering the non-device areas were etched by using the potassium iodide (KI) solution. After exposing the diamond surface to the oxygen plasma, the device isolation was realized by replacing the C–H surface termination with the high resistive C–O surface termination. Drain and source electrode metals were formed by wet etching using KI solution. A 10-nm-thick (confirmed by the ellipsometry) Al_2O_3 layer was coated on the C–H surface through the ALD method using $Al(CH_3)_3$ and H_2O as precursors. For one sample, the ALD deposition temperature was 80 °C and for the other sample, it was 300 °C. Aluminum (Al) gate metal was formed by using the thermal evaporation and lift-off process. The schematic diagrams of the fabrication processes are shown in Fig. 1. The gate width (W_G) was 200 μm and the gate lengths (L_G) were 0.1 μm and 50 μm, respectively.

Figure 2 shows the top-view SEM pictures of the 0.1-μm-L_G diamond devices. For the 0.1-μm L_G devices, DC and pulsed *I*–*V* curves were measured by using a Keithley 4200 semiconductor parameter analyzer. For the 50-μm L_G Fat-FET devices, besides the DC I_{GS}–V_{GS} test, capacitance and conductance measurements (ranging from 1 kHz to 1 MHz) were performed by using an Agilent B1500A semiconductor device analyzer. All measurements were conducted in a dark environment at room temperature (300 K).

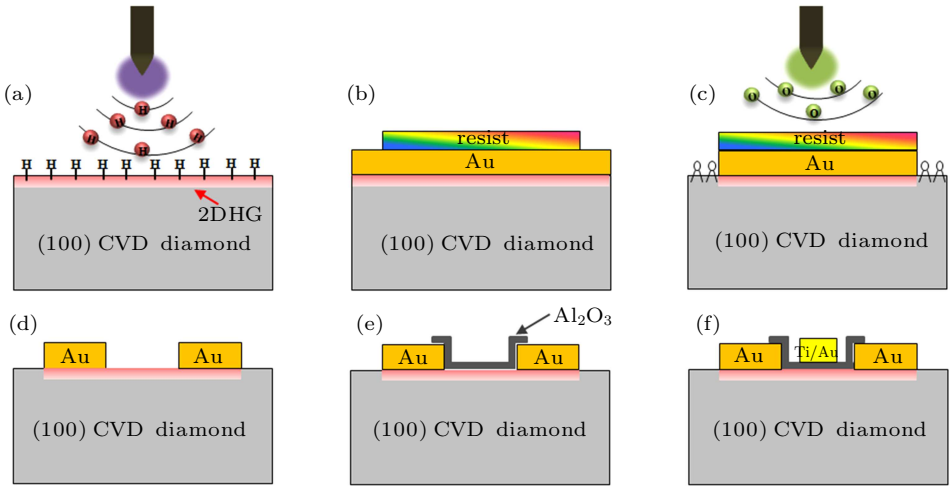


Fig. 1. C–H diamond MOSFET fabrication processes. (a) Hydrogen-termination treatment, (b) deposition of Au to protect H-terminated diamond surface, and preparation of wet etching process of non-device areas, (c) device isolation by using oxygen plasma, (d) formation of source and drain electrodes, (e) ALD deposition of Al_2O_3 as gate insulator and passivation layer, and (f) gate fabrication and lift-off.

Figure 3(a) shows the measured *C*–V_G characteristics of the gate–source capacitance of the Fat-FET devices at 1 MHz. The measured dielectric constants (ε) of Al_2O_3 under 80-°C and 300-°C depositions are 8.75 and 6.78, respectively, which are consistent with the reported values.[20,21] The inset of Fig. 3(a) shows the calculated hole sheet density (n_p) *versus* gate voltage by integrating the *C*–V_G curve. The maximum 2DHG concentrations are 8.7×10^{12} cm^{-2} (300 °C) and 1.1×10^{13} cm^{-2} (80 °C), respectively. The inset shows that less channel holes exist in the 300 °C-deposition diamond

device than in the 80-°C case, which is possibly due to the fact that the conduction-related surface adsorbates of C–H diamond decrease with ALD deposition temperature increasing, which was indicated by the reported high-resolution transmission electron microscopy (HRTEM) images.[22] Furthermore, the Mott–Schottky plot is shown in Fig. 3(b), from which the flat band voltage (V_{FB}) was determined by linear extrapolation of the $1/C^2$–V_G curves to the abscissa. The background acceptor concentration (N_A) extracted from the linear slope[23] are 1.1×10^{13} cm^{-3} and 2.2×10^{13} cm^{-3} for 80 °C and 300 °C, separately. The values suggest the high purity of the diamond samples. Taking into account the difference in work function between Al (4.3 eV) and C–H diamond (4.9 eV),[24] the theoretical flat band voltage (V_{FB0}) was calculated to be 0.6 V. As indicated in Fig. 3(b), the measured V_{FB} values for 80-°C and 300-°C depositions were 0.42 V and 0.74 V, respectively. According to $Q_{ox}=C_{ox}\times(V_{FB}-V_{FB0})/q$, the fixed charges in the oxide layer (Q_{ox}) were estimated to be 8.7×10^{11} cm^{-2} (80 °C) and -5.9×10^{11} cm^{-2} (300 °C). The negative fixed charges in the Al_2O_3 deposited at 300 °C could be due to some unoccupied levels in the bandgap of Al_2O_3 located near the valence band edge of diamond.[25] The positive fixed charges observed in the 80-°C deposition device may be attributed to the oxygen vacancies in the oxide films.[26]

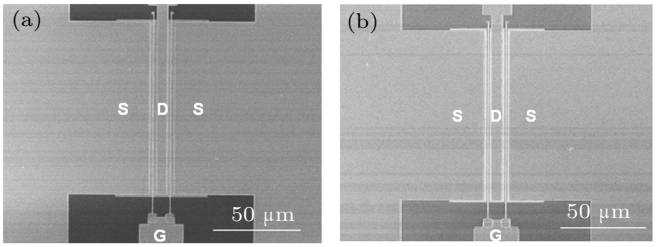


Fig. 2. Topview SEM images of 0.1-μm L_G: (a) 80-°C deposition device and (b) 300-°C deposition device.

The DC tests (I_{D-DC}) show that both diamond devices' maximum drain currents exceed −400 mA/mm (L_G = 0.1 μm), the I_{DS}–V_{GS} curve of the 80-°C and 300-°C deposition devices at $V_{DS}=-8$ V are shown in Fig. 4. Owing to the higher dielectric constant of the 80-°C deposition ALD Al_2O_3 film, the device has exhibited better subthreshold performance. Pulsed *I*–*V* test is more effective than DC *I*–*V* measurement to characterize the traps-related performances because of its discontinuous signal excitation. Comparatively speaking, there is more severe current degradation in the 80-°C deposition diamond device when it is operated in the pulse *I*–*V* mode as shown in Fig. 5. Specifically, pulsed *I*–*V* ($I_{D-pulse}$) measurements are employed to characterize the response of trap charging/discharging for the 0.1-μm-L_G diamond MOSFETs ($V_{GSQ}=5$ V, $V_{DSQ}=-8$ V). If the time constant of the charged traps is smaller than the pulse width, reduced holes and thus reduced current will be observed due to insufficient time for discharging from traps.[27] Figure 6 shows the $I_{D-pulse}/I_{D-DC}$ characteristics measured at $V_{GS}=-2$ V and $V_{DS}=-6$ V. During the measurements, the pulse period used is 1 ms and the pulse width varies from 1 μs to 100 μs. For the 80-°C deposition device, a much more serious current degradation is observed, which suggests that it has more donor-like traps with a time constant smaller than 100 μs. In addition, it is worth noting that the drain current densities of the 300-°C deposition device in this work is the highest in the reported C–H diamond MOSFETs with 300-°C deposition ALD Al_2O_3.[14,19]

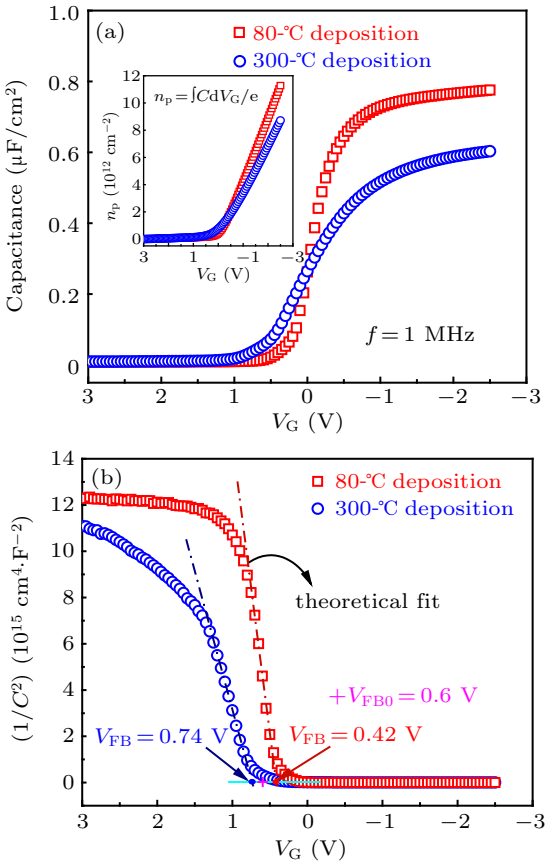


Fig. 3. (a) C–V_G and (b) $1/C^2$–V_G characteristics of the Al_2O_3/C–H diamond capacitor measured at 1 MHz and room temperature (RT). V_{FB} of 0.42 V and 0.74 V are measured at 80-°C and 300-°C depositions, respectively, and V_{FB0} of 0.6 V is the theoretical value, it is fitting with the formula $1/C^2=(-2/\varepsilon\varepsilon_0 eN_A)(V-V_{FB}+kT/e)$.

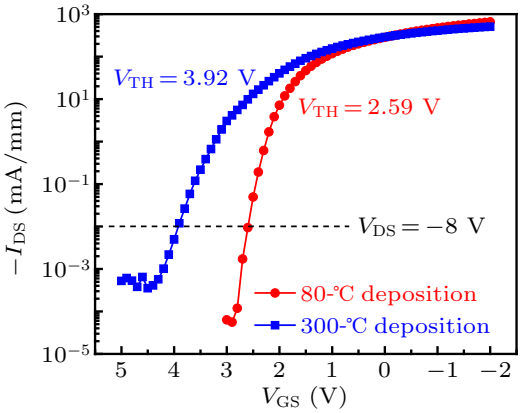


Fig. 4. DC I_{DS}–V_{GS} curve of 80-°C and 300-°C deposition 0.1-μm-L_G devices at $V_{DS}=-8$ V.

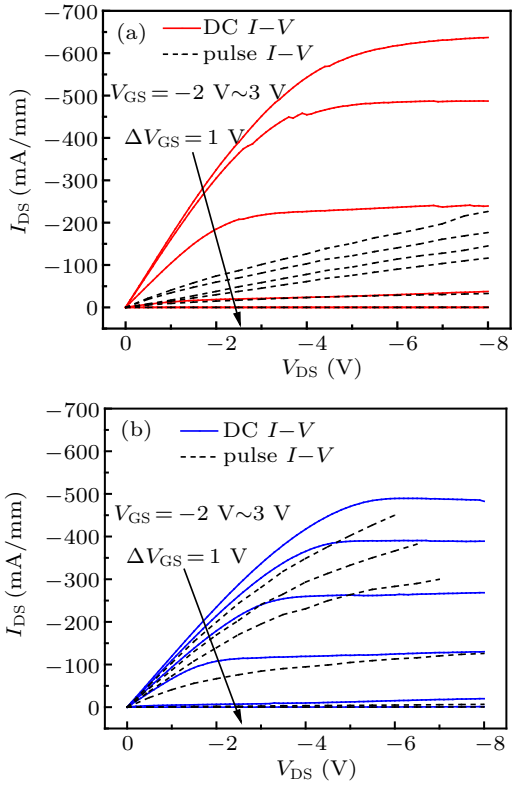


Fig. 5. DC and pulsed I–V characteristics of (a) 80-°C and (b) 300-°C deposition diamond MOSFETs. In pulsed I–V case, quiescent bias point is selected at $V_{GSQ}=5$ V, $V_{DSQ}=-8$ V, and pulsed period and width are 1 ms and 1 μs, respectively.

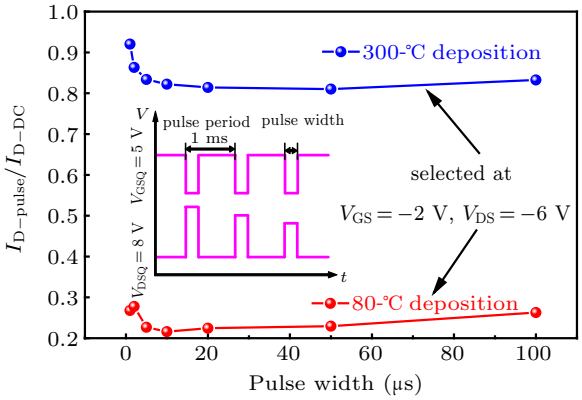


Fig. 6. Ratio of pulse current to DC current ($I_{D-pulse}/I_{D-DC}$) characteristics of 80-°C and 300-°C deposition devices at $V_{GS}=-2$ V and $V_{DS}=-6$ V, with inset showing applied waveform during pulse I–V measurement.

3. The interface trap mapping by conductance method

In general, emission, rather than capture, is the rate limiting process.[28] Thus characterization of the trap emission time constant (τ_{it}) in diamond is crucial to the understanding of the interior trap behaviors. The frequency-dependent conductance method, proposed by Nicollian and Goetzberger,[28] is used to determine the interface traps behavior. The inset of Fig. 7 shows (a) the equivalent circuit of the measured MOS structure, where C_m and G_m denote the measured capacitance and conductance, respectively; (b) the equivalent circuit of the MOS structure used for the conductance method, where $C_{it}=qD_{it}$ is the interface trap capacitance when D_{it} is given in $eV^{-1}\cdot cm^{-2}$, R_{it} represents the energy loss caused by the capture-emission of carriers by interface trap, $\tau_{it}=R_{it}C_{it}$ is the interface trap time constant; (c) the simplified circuit with equivalent parallel conductance (G_p). In particular, series resistance (R_s) is introduced into the equivalent circuit considering high contact and access resistance of C–H diamond devices.[29]

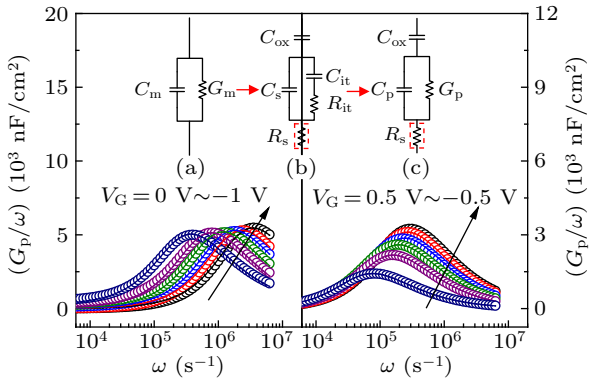


Fig. 7. Experimental data (circles) and fitting curves (lines) of $G_p/\omega\sim\omega$. Plotted $G_p/\omega\sim\omega$ results of the 80-°C (left) and 300-°C deposition (right) devices are selected in their subthreshold bias regions. Inset shows (a) measured and [(b), (c)] equivalent circuits of MOS structure, correcting for series resistance (R_s) of contact resistance and access resistance of diamond FETs.

The $G_p/\omega\sim\omega$ characteristics at the selected voltages can be determined from C_m and G_m,[28] which can be expressed as

$$\frac{G_p}{\omega}=\frac{\omega G_c C_{ox}^2}{G_c^2+\omega^2\left(C_{ox}-C_c\right)^2}, \tag{1}$$

where C_{ox} of 0.78 μF/cm^2 and 0.60 μF/cm^2 were extracted from the C–V_G characteristics of the 80-°C and 300-°C deposition devices, respectively,

$$C_c=\frac{C_m}{\left(1-R_sG_m\right)^2+\left(\omega R_sC_m\right)^2}, \tag{2}$$

$$G_c=\frac{\omega^2R_sC_mC_c-G_m}{R_sG_m-1}, \tag{3}$$

with $\omega=2\pi f$ being the radial frequency, R_s is the series resistance and determined from

$$R_s=\frac{G_{ma}}{G_{ma}^2+\omega^2C_{ma}^2}. \tag{4}$$

Here, G_{ma} and C_{ma} are the measured conductance and capacitance in the accumulation mode. By assuming continuous interface trap levels, G_p/ω can be given by

$$\frac{G_p}{\omega}=\frac{qD_{it}}{2\omega\tau_{it}}\ln\left[1+\left(\omega\tau_{it}\right)^2\right], \tag{5}$$

where q is the elemental charge, and D_{it} denotes the trap density. Mapping of D_{it} and τ_{it} can be achieved by fitting the experimental $G_p/\omega\sim\omega$ data through using Eq. (5) as shown in Fig. 7. For Eq. (5), the peak point $(G_p/\omega)_{max}$ is located at

$\omega\tau_{it} = 2$, and D_{it} correlated with $(G_p/\omega)_{max}$ equals $(2.5/q)$ $(G_p/\omega)_{max}$. It can be seen that the measured conductance peaks of the 80-°C deposition device are broader than those predicted by Eq. (1), which was also observed in the non-annealed MOSFETs.[30] From Fig. 7, it can be seen that the 300-°C ALD process on the C–H diamond surface results in the suppression of the oxide charge non-uniformities and a higher interface quality. According to the Shockley–Read–Hall (SRH) statistic model,[28] the trap energy levels above diamond valence band (E_{it}–E_V) can be deduced from the trap time constant (τ_{it}), which is written as

$$E_{it} - E_V = kT \ln\left(v_{th}\sigma_p N_V \tau_{it}\right), \tag{6}$$

where v_{th} is the thermal velocity, σ_p is the hole capture cross section, and N_V is the effective density of states in diamond valence band. By assigning $T = 300$ K, $v_{th} = 1 \times 10^7$ cm/s, $\sigma_p = 4 \times 10^{-13}$ cm^{-2}, and $N_V = 2.7 \times 10^{19}$ cm^{-3}, figure 8(a) shows the mapping results of the trap density distributions and the corresponding energy levels, indicating that shallow traps ($E_{it} - E_V \approx 0.46$ eV–0.56 eV) exist in diamond devices. Specifically, D_{it} in the 80-°C deposition device is in a range of 7.8×10^{13} eV^{-1}·cm^{-2}–8.5×10^{13} eV^{-1}·cm^{-2} for an energy level span of 0.46 eV–0.52 eV above the valence band of diamond. The higher trap density in the 80-°C deposition device is consistent with the results obtained from the above pulse I–V analysis. The devices with high interface traps may suffer the weak Fermi-level pinning (WFLP) effect, which will make the majority of charges in the MOS capacitor accommodated by interface traps, and cannot be found to operate as a classic MOS capacitor.[31] Notably, besides the depletion and accumulation performances in the C–V curves (Fig. 3(a)), the typical current–voltage on/off characteristics (Fig. 4) can be observed for both devices. That is to say, the potential influence of the WFLP effect on our devices is generally acceptable. For the 300-°C deposition device, D_{it} is in a range of 2.2×10^{13} eV^{-1}·cm^{-2}–5.1×10^{13} eV^{-1}·cm^{-2}, with the energy level span of 0.53 eV–0.56 eV above the valence band of diamond. In fact, diamond material is expected to have deep energy level interface traps with long τ_{it}.[12] According to the SRH model, relation between the detectable trap energy range in the band gap of diamond (5.5 eV) and the correlated τ_{it} is shown in Fig. 8(b). Notably, by using the conductance method at RT, only a small part of the trap states in diamond can be detected, and the calculated τ_{it} is around 1 year for the near-midgap trap states even at 300 °C (the grey line).

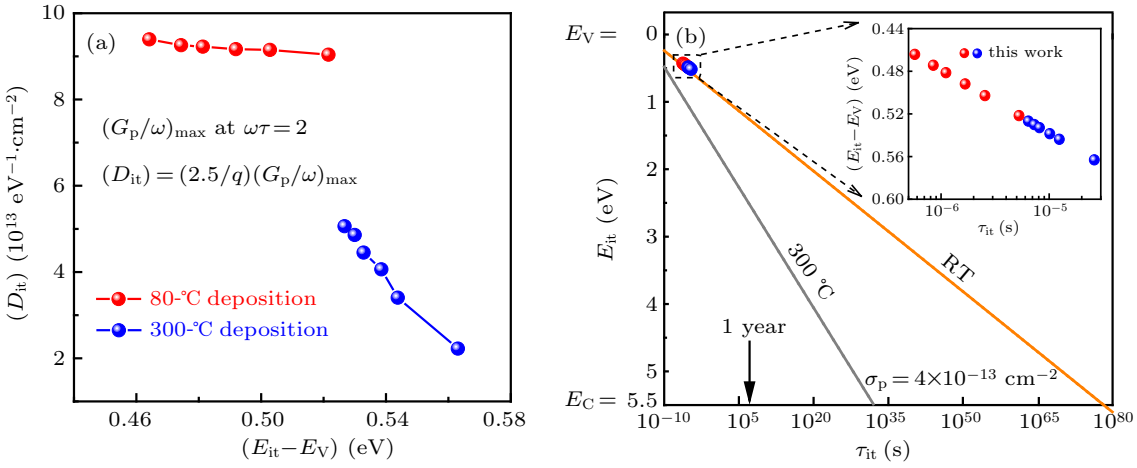


Fig. 8. (a) Energy distributions of interface state density of Al_2O_3/C–H diamond structure, and (b) energy level E_{it} *versus* trap emission time constant τ_{it} in diamond band gap at RT (orange line) and 300 °C (grey line).

Figure 9 shows the schematic of energy band of the capturing process and emission process of the interface traps with different trap energy levels above the valence band of diamond (at the same gate voltage), and the red line and blue line demonstrate the energy band of the 80-°C and 300-°C deposition devices, respectively. Higher band up-bending of the 80-°C deposition suggests higher carrier concentration in the 2DHG channel, and it contains shallower energy level interface traps (ΔE_T) while the trap density is higher. As shown in Fig. 9(a), the interface traps capture the carriers when reducing V_G. Figure 9(b) indicates that the filled interface traps with lower ΔE_T first emit the holes to the channel when increasing V_G, while those interface traps with higher ΔE_T are more difficult to emit the holes. The gate leakage current characteristics of both Fat-FETs are shown in Fig. 10, it can be noted that the I_{GS} of the 80-°C deposition device begins to increase at the forward bias, while the 300-°C deposition device maintains low I_{GS} in the total V_{GS} range. This can be attributed to the emission of the trapped holes into the gate electrode as suggested by the Frenkel–Poole (FP) emission effect,[14] since the detected interface trap of the 80-°C deposition device is higher than that of the 300-°C deposition device.

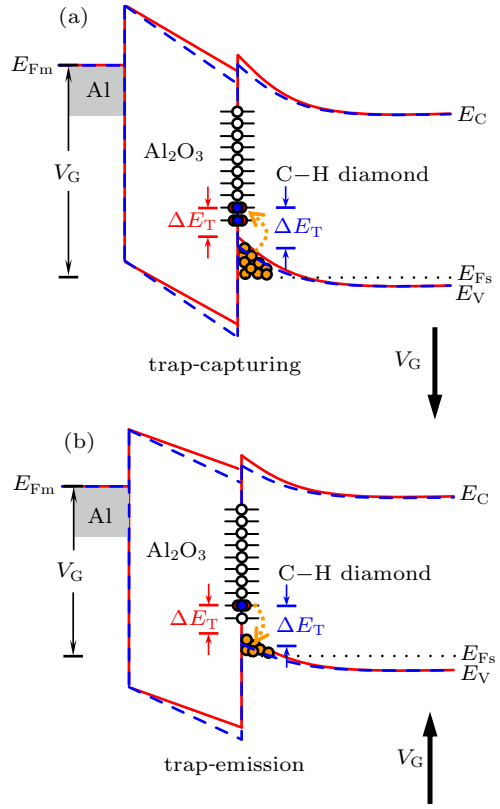


Fig. 9. Schematic diagram of band diagrams of the capturing and emission processes of Al_2O_3/C–H diamond interface traps, where red and blue lines demonstrate the energy band of the 80-°C and 300-°C deposition devices, respectively. (a) Trap capturing with V_G decreasing (hole accumulation), and (b) trap emission with V_G increasing (hole depletion).

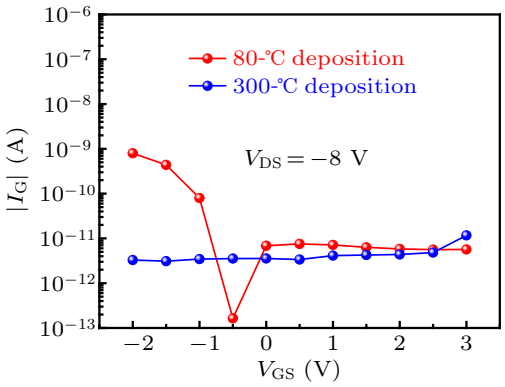


Fig. 10. Gate leakage current of 50 μm-L_G diamond MOSFETs.

4. Conclusions and perspectives

In this paper, the comparative studies by using C–V_G and pulse/DC I–V measurements are presented to characterize the traps-induced current degradation in the C–H diamond MOSFETs at different Al_2O_3 deposition temperatures. The results show that while a wide range of ALD deposition temperatures can be used to fabricate diamond FETs with low gate leakage current and high drain current density, different trapped charges can exist in the Al_2O_3 dielectric layer. Experimental results show that 300-°C ALD grown Al_2O_3 can be a suitable gate dielectric and passivation layer solution for the prospective diamond power devices.

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