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Improved 4H-SiC UMOSFET with super-junction shield region*

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This article investigates an improved 4H-SiC trench gate metal–oxide–semiconductor field-effect transistor (MOSFET) (UMOSFET) fitted with a super-junction (SJ) shielded region. The modified structure is composed of two n-type conductive pillars, three p-type conductive pillars, an oxide trench under the gate, and a light n-type current spreading layer (NCSL) under the p-body. The n-type conductive pillars and the light n-type current spreading layer provide two paths to and promote the diffusion of a transverse current in the epitaxial layer, thus improving the specific on-resistance ($R_{on,sp}$). There are three p-type pillars in the modified structure, with the p-type pillars on both sides playing the same role. The p-type conductive pillars relieve the electric field (E-field) in the corner of the trench bottom. Two-dimensional simulation (silvaco TCAD) indicates that $R_{on,sp}$ of the modified structure, and breakdown voltage (V_{BR}) are improved by 22.2% and 21.1% respectively, while the maximum figure of merit (FOM $= V_{BR}^2/R_{on,sp}$) is improved by 79.0%. Furthermore, the improved structure achieves a light smaller low gate-to-drain charge (Q_{gd}) and when compared with the conventional UMOSFET (conventional-UMOS), it displays great advantages for reducing the switching energy loss. These advantages are due to the fact that the p-type conductive pillars and n-type conductive pillars configured under the gate provide a substantial charge balance, which also enables the charge carriers to be extracted quickly. In the end, under the condition of the same total charge quantity, the simulation comparison of gate charge and OFF-state characteristics between Gauss-doped structure and uniform-doped structure shows that Gauss-doped structure increases the V_{BR} of the device without degradation of dynamic performance.

Keywords: breakdown voltage, specific on-resistance, silicon carbide, switching energy loss, super-junction (SJ), trench gate MOSFET

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1. Introduction

The advantages of silicon carbide (SiC) include a good wide bandgap performance, high electron saturation drift velocity, and high thermal conductivity.[1] The SiC is therefore very suitable for the development of the next-generation power electronic components that possess a high conversion efficiency, high voltage capability and low conduction loss. Furthermore, through simulation studies, Yu and Sheng[2] have shown the possibility that a SiC device can perform beyond its unipolar theoretical limit.

A SiC power trench gate MOSFET is a good candidate for serving as power switching in order to increase conversion efficiency. However, the UMOSFET does have a critical issue that it can generate a large E-field in the corner of the trench bottom, which affects the reliability of the device. To overcome this, some shielding methods and structures have been improved.[3–5] The most representative approach is to introduce the p+shielded region under the gate trench (conventional-UMOS).[6–9] However, the JFET region is formed between the p+shielded region and the p-base region, which increases the specific on-resistance. In order to achieve a better trade-off between specific on-resistance and avalanche voltage, a super-junction is a new structure, which improves the trade-off between specific on-resistance and avalanche voltage, and enables the low specific on-resistance in the industrial silicon power MOSFET.[10–12] Orouji *et al.*[13] studied the unique features that were exhibited by power in the 4H-SiC UMOSFET, where the n- and p-type columns in the drift region were incorporated in order to improve the breakdown voltage, on-resistance. In order to achieve lower on-resistance and better switching performance, Deng *et al.*[14] investigated a device structure that had a built-in floating component. In order to optimize the trade-off between on-resistance and short circuit ruggedness, He *et al.*[15] improved a 4H-SiC super-junction trench MOSFET by adding a grounded p+buried layer below the p-body, an oxide trench under the gate, and a p-region surrounding the oxide trench.

Moreover, the practical feasibility of fabricating super-junction structures has been discussed in some papers.[16–21] Kobayashi *et al.*[16] for example, reported that the SJ structure was formed on the drift layer by using multi-epitaxial growth seven times, gaining a thickness of 0.65 μm each, and then the

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p-column was formed by implanting aluminum into the drift-layer and multi-epitaxial layers eight times in total. Furthermore, Kosugi *et al.*[17] developed a novel trench-filling epitaxial growth method as a promising alternative and Harada *et al.*[18] presented the first demonstration of the dynamic characteristics for a SiC superjunction MOSFET that was realized by the multi-epitaxial growth method.

This article investigates an improved 4H-SiC UMOSFET that has alternate p-type and n-type conductive pillars under the gate. The simulations indicate that the modified structure exhibits a good dynamic performance and improves the V_{BR} and $R_{on,sp}$. The figure of merit of the conventional-UMOS is 563 MW/cm^2, while the FOM of the modified-UMOS is 1008 MW/cm^2. The V_{BR} of the Gauss-doped structure is improved to 10.4% compared with that of the uniform-doped structure. The Gauss-doped and uniform-doped superjunction shield region gate–drain charges are the same.

2. Description of device structure and fabrication procedure

Figures 1(a) and 1(b) show the schematic cross section of a conventional-UMOS and a modified-UMOS, which are both used for reference. The detailed simulation parameters of the structure are listed in Table 1.

Figure 2 shows a feasible method of fabricating the modified-UMOS. An n-type epitaxial layer was grown on an n+substrate. The whole drift layer was about 10-μm thick with a doping concentration of 7.0×10^{15} cm^{-3}. The trench was formed by inductive coupled plasma reactive-ion etching (ICP-RIE) with SF_6, O_2, and HBr, using a Ni/Al_2O_3 bi-layer mask.[22,23] The n-pillars were formed by deposition[14] as shown in Fig. 2(a). The p-pillars, with a depth of 6 μm, were formed by a multi-epitaxial growth method[18] as shown in Fig. 2(c). Finally, the p-body region, the light n-type current spreading layer, the n+source region, the p+source region, and the gate structure were implemented in a similar way to that adopted in the conventional-UMOS.

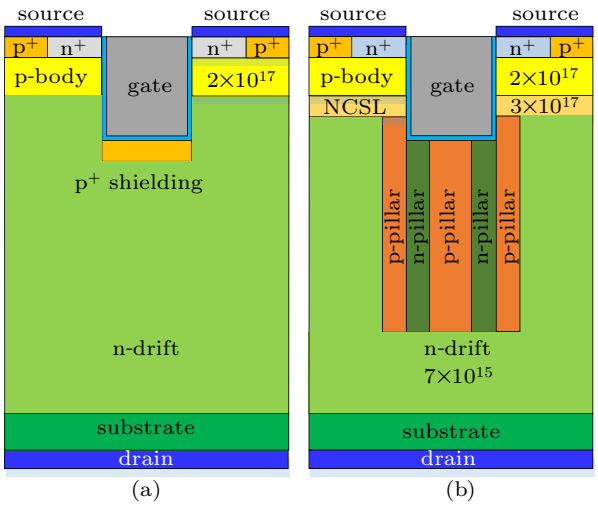


Fig. 1. Structures of studied trench MOSFET: (a) conventional-UMOS, and (b) modified-UMOS.

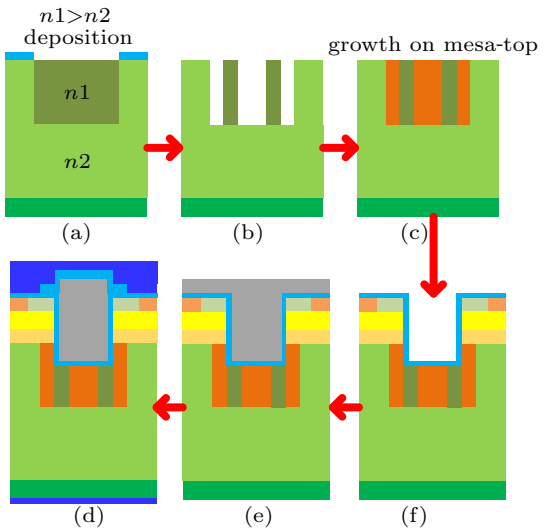


Fig. 2. Key fabrication process for the modified-UMOS.

Table 1. Device parameters for simulations.

Device parameters	Conventional-UMOS	Modified-UMOS
n+source junction depth (μm)	0.2	0.2
p-body junction depth (μm)	0.5	0.5
p+junction depth (μm)	0.2	0.2
Gate trench depth (μm)	1.5	1.5
Thickness of n-drift (μm)	10.0	10.0
Thickness of gate oxide (nm)	50	50
n-type current spreading layer depth (μm)	–	0.2
n-pillar depth (μm)	–	6.0
p-pillar depth (μm)	–	6.0
Width of trench (μm)	2.0	2.0
Width of mesa (μm)	2.5	2.5
n-drift doping concentration (10^{15} cm^{-3})	7.0	7.0
p-body doping concentration (10^{17} cm^{-3})	2.0	2.0
n-type current spreading layer doping concentration (10^{17} cm^{-3})	–	3.0
p-pillar doping concentration (10^{16} cm^{-3})	–	4.0
n-pillar doping concentration (10^{16} cm^{-3})	–	4.0

3. Results and discussion

In this work, the physical 4H-SiC MOSFET models, including the FLDMOB and ANALYTIC mobility models, are used. The FLDMOB is a parallel, E-field-dependent model, that requires the modeling of any type of velocity saturation effect; the ANALYTIC model is a concentration-temperature-dependent model; the Shockley–Read–Hall and AUGER models are composite models that are used to solve the electron/hole continuity equation, as well as the Poisson equation; IMPACT SELB is a Selberherr model and is recommended for most situations; and INCOMPLETE is an ionization model.[24]

3.1. Static performance

The two structures' typical output characteristic curves of $V_{gs} = 8$ V, $V_{gs} = 12$ V, $V_{gs} = 16$ V, and $V_{gs} = 20$ V are shown in Fig. 3. The $R_{on,sp}$ of the modified-UMOS and the conventional-UMOS are estimated as ~ 1.9 mΩ·cm^2 and ~ 2.4 mΩ·cm^2 at $V_{gs} = 16$ V and $V_{ds} = 1$ V, respectively. The n-type conductive pillars and a thin NCSL provide two paths, which suppress the depletion region. The smaller the depletion region, the wider the current path for the electrons is. Moreover, a thin light doping of the NCSL causes the electrons to spread in the horizontal direction earlier. In addition, n-pillars under the gate allow the current to flow in the vertical direction. Therefore, the modified structure reduces the $R_{on,sp}$. Comparing with the conventional-UMOS, the $R_{on,sp}$ of the modified structure decreases by 22.2%. In the modified-UMOS, the n-type conductive pillars under the gate increase the electron concentration of the channel region, while the depletion region is reduced in order to increase the current path in the modified structure as shown in Fig. 4.

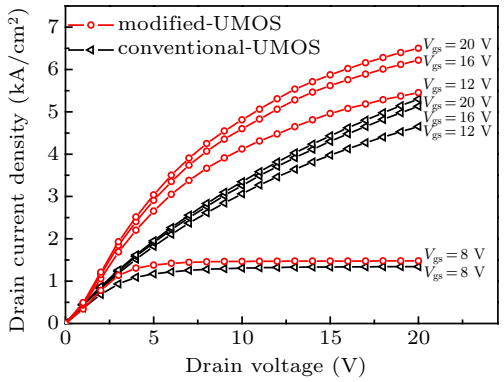


Fig. 3. Typical output characteristic curves of two structures.

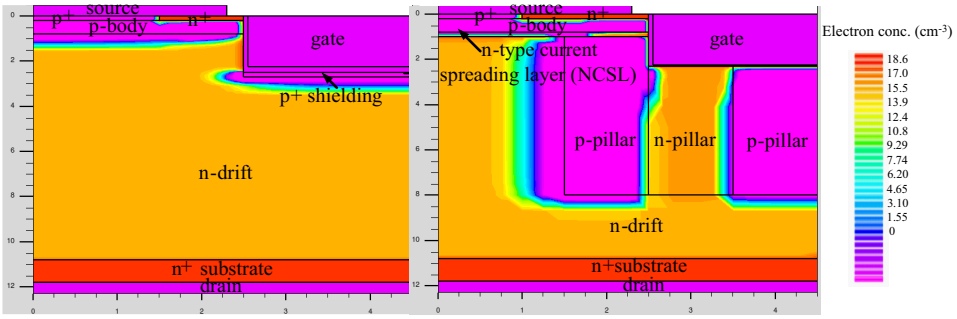


Fig. 4. Distribution of electron concentration (Conc.) for (a) conventional-UMOS and (b) modified-UMOS.

The equation of the $R_{on,sp}$ can be described as

$$R_{on,sp} = \left(\frac{W_D}{q\mu_n N_D}\right), \tag{1}$$

where W_D is the maximum depletion width and the μ_n is the electrons mobility.

Figure 5 shows reverse breakdown characteristic contours (at $V_{gs} = 0$ V). The V_{BR} of the two structures are calculated to be ~ 1167 V and ~ 1413 V respectively. The modified structure has a higher V_{BR}, because the n-pillar and p-pillar at the bottom of the trench are configured to have a substantial charge balance in an SJ structure. When the doping density of the n-type conductive pillars is equal to the surface doping density of the p-type conductive pillars, the mutual depletion of the n-pillar and the p-pillar under the gate trench can achieve the charge balance of the SJ structure.

For the conventional-UMOS, the peak E-field ($\sim$ 3.3 MV/cm) occurs in the corner of the gate trench, whereas in the modified structure, the peak E-field (~ 2.6 MV/cm) occurs at the bottom of the p-pillars. The critical gate oxide E-field of a conventional UMOS is ~ 2.1 MV/cm, which is higher than the ~ 1.2 MV/cm belonging to the modified-UMOS as shown in Fig. 6. This difference occurs because the protruding p-pillar has an excellent shielding effect. During the simulation, the breakdown voltage for the modified-UMOS has an improvement of 21.1% compared with the the breakdown voltage of the conventional-UMOS.

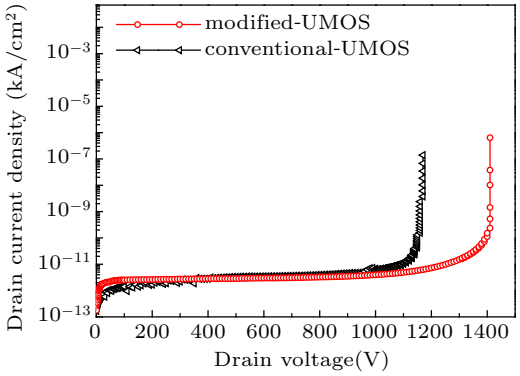


Fig. 5. Reverse breakdown characteristic (at $V_{gs} = 0$ V) curves of two structures.

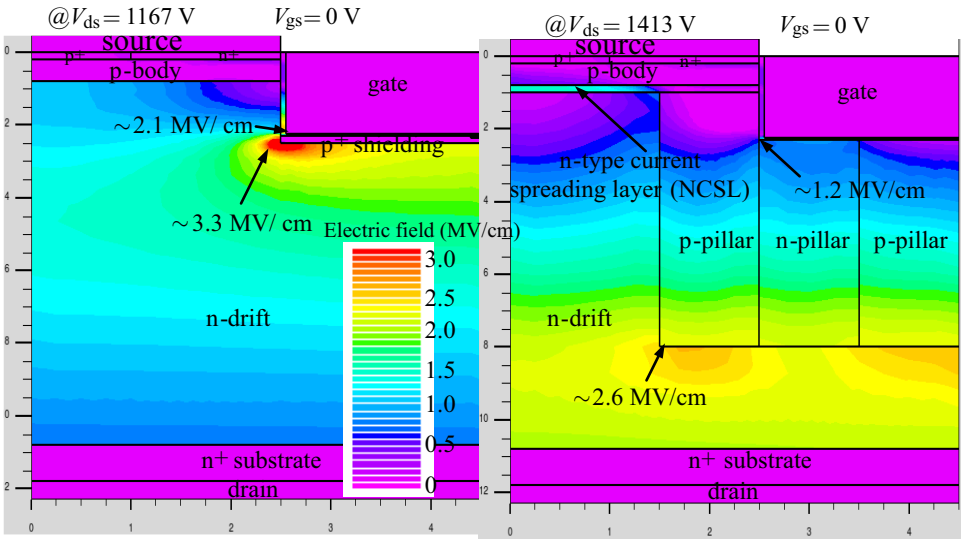


Fig. 6. OFF-state critical E-field curves of (a) conventional-UMOS, (b) modified-UMOS.

3.2. Dynamic performance

Figure 7 shows the curves of the input capacitance C_{iss}[$C_{iss} = C_{gd}$ (gate–drain capacitance) + C_{gs} (gate–source capacitance)] and the reverse transfer capacitance ($C_{rss} = C_{gd}$).[25,26] The smaller C_{gd} helps improve the switching characteristic.

The small ac signal works at 1 MHz to extract the capacitance,[27,28] and the capacitance cures of the modified-UMOS are not linear.[29,30] When $V_{ds} < V_t$ (at $V_t = 75$ V), the C_{rss} is small because of the protruding p-pillar on the left, which shields C_{gd}. Thus, the capacitance at the bottom of the gate trench is mainly C_{gs}. When $V_{ds} > V_t$, the p-pillar region will shrink, the shielding effect will be weakened and C_{rss} will slowly increase.

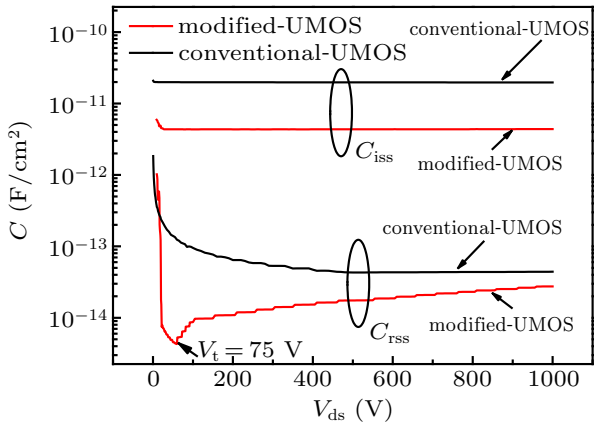


Fig. 7. Small signal capacitances C_{iss} and C_{rss} of two structures.

Figure 8 shows gate charge characteristic curves of the two structures. In the simulation, the test circuit is indicated as an inset in Fig. 8. The FOM $R_{on,sp} \times Q_{gd}$ is widely used.[31,32] Since the substantial charge balance of the SJ structure is achieved when the surface doping density in the p-type conductive pillar, the Q_{gd} of the improved structure is a little smaller than that of the conventional-UMOS as can be seen in this figure. When the modified-UMOS is turned off, the two-dimensional fast depletion of the n-type conductive pillar and p-type conductive pillar enables the charge carriers to be extracted quickly. The FOM $R_{on,sp} \times Q_{gd}$ of the modified-UMOS shows an improvement of 43.3% in comparison with that of the conventional-UMOS. Detailed data are listed in Table 2. Using the double-pulse test (DPT), figure 9 shows the switching performance of the two structures. The area of the SiC MOSFET is set to be 0.09 cm^2. For convenience, some parameters in the following simulation design are given as follows: a gate resistor is $R_g = 20\ \Omega$, the supply voltage is $V_{dd} = 400$ V, the inductive load is $L_L = 200\ \mu$H, and the stray inductance (L_S) is assumed to be 10 mH in the power loop. The gate voltage is switched between 0 V and 20 V in order to turn-on and turn-off the device.

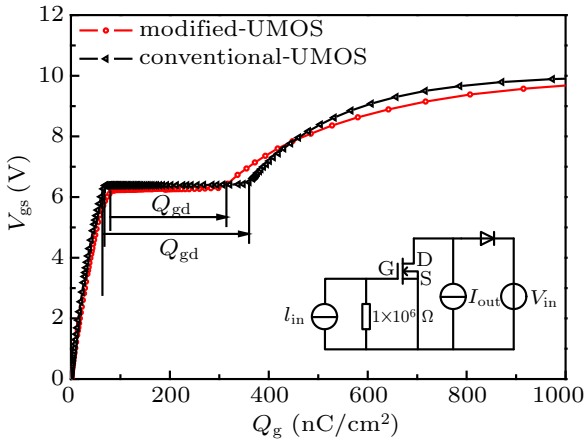


Fig. 8. Gate charge tests on the modified-UMOS (red line) and on conventional-UMOS (black line), with insert showing test circuit.

Figures 10(a) and 10(b) show the switching waveforms of the two structures with a test current of 20 A/cm^2. As can be seen from Fig. 7, the low C_{rss} in the modified-UMOS has

a faster switching speed than that in the conventional-UMOS. Therefore, the conventional-UMOS needs a longer time period to arrive at a high V_{ds} and a high I_{ds} as the switching characteristics are related to the charge and discharge of its C_{iss} and the smaller C_{iss} can improve the switching characteristics.

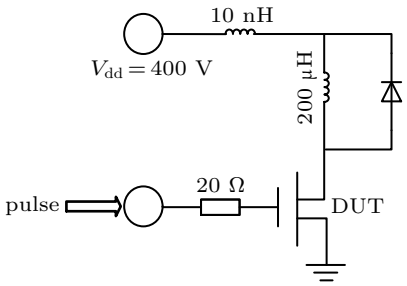


Fig. 9. Double-pulse test circuit.

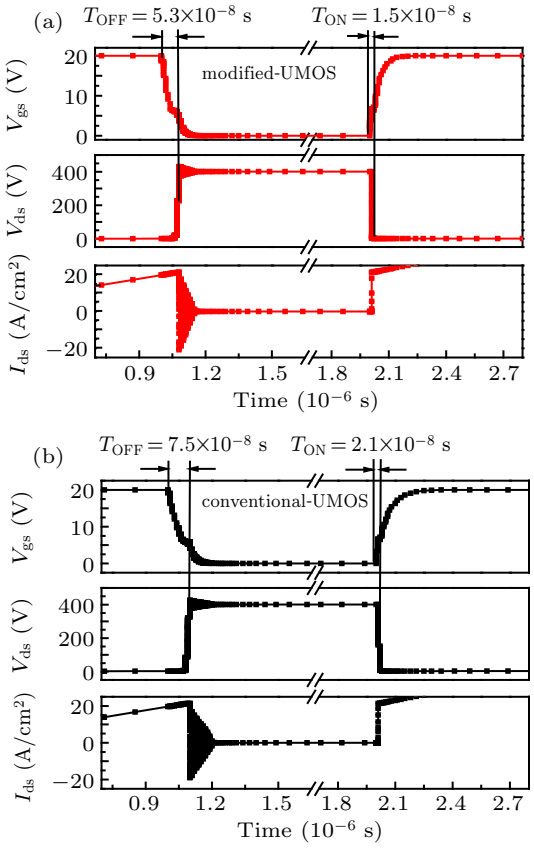


Fig. 10. Switching waveforms for (a) modified-UMOS and (b) conventional-UMOS, showing that improved structure is much faster than conventional-UMOS.

Figure 11 shows the switching energy losses for the conventional-UMOS and modified-UMOS. It can be discerned that in the modified structure, the losses during both turn-on (E_{on}) and turn-off (E_{off}) are reduced. For the modified-UMOS, the calculated value of E_{on} and E_{off} are 33.5 mJ/cm^2 and 32.9 mJ/cm^2, respectively, which correspondingly reduce 33.4% and 8.2% of the counterparts for the conventional-UMOS. The T_{OFF} and T_{ON} of the two structures are listed in Table 2. The E_{on} and E_{off} can be expressed as

$$E_{on} = \int_{T_1}^{T_2} V_{ds} * I_{ds}\,dt, \tag{2}$$

$$E_{off} = \int_{T_3}^{T_4} V_{ds} * I_{ds}\,dt, \tag{3}$$

where T_1 is the time when V_{gs} (on) reaches 10% of its value, T_2 is the time when V_{dd} arrives at 10% of its value, T_3 is the time when V_{gs} (on) rises to 90% of its value, and T_4 is the time when I_{ds} is 2% of its value.

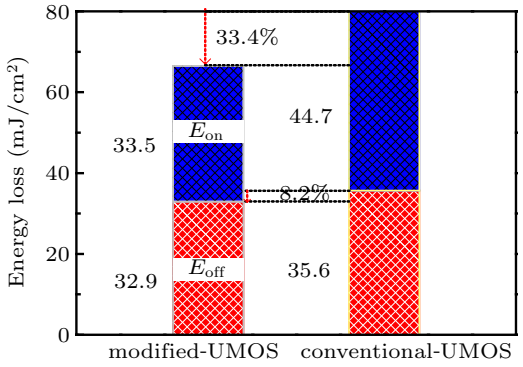


Fig. 11. Switching energy losses of two structures.

Table 2. Static performance and dynamic performance data.

Structure	$Q_{gd,sp}$ (nC/cm^2)	$(V_{BR}^2/R_{on,sp})$ (MW/cm^2)	$R_{on-sp} \times Q_{gd,sp}$ (mΩ·nC)	T_{OFF} (10^{-8} s)	T_{ON} (10^{-8} s)
Modified-UMOS	307	1008	607.8	5.3	1.5
Conventional-UMOS	360	563	871.2	7.5	2.1

3.3. Parameter optimization

Figure 12 shows FOM ($V_{BR}^2/R_{on,sp}$) as a function of N_{rp}, N_n, N_{lp}, and H in the modified-UMOS. The doping concentration (N_{lp}) of the protruding p-pillar, (N_{rp}) the p-pillar at the bottom of gate trench, (N_n), and the n-type conductive pillar, as well as the height (H) of pillars, have a great influence on the device performance. The p-type conductive pillars may have a doping concentration in a range from $\sim 1\times10^{16}$ cm^{-3} to $\sim 1\times10^{17}$ cm^{-3}. The doping concentration of the p-type and n-type pillars are denoted as N_p and N_n, respectively, and the width of the p-type and n-type pillars are represented by W_p and W_n, respectively. The n-type pillar and p-type pillar at the bottom of the gate trench are configured to achieve a substantial charge balance in the SJ structure. This is achieved when the $W_n \cot N_n = W_p \cdot N_p$. If the conductive pillar is the one affected by the incomplete ionization, the current density is highly reduced, and the risk is that this leads to the total depletion of the p-type pillar, and consequentially, to no current flowing in the device.[33] The protruding p-pillar plays a critical role in shielding the high E-field of the trench bottom, therefore, the protruding p-pillar must have a high doping concentration in order to have the necessary efficacy to shield the high E-field. The N_n can be raised appropriately to reduce $R_{on,sp}$ and when increasing the doping concentrations of these pillars, N_{rp} and N_{lp} can also be appropriately optimized to improve V_{BR}.

The maximum figure of merit values appear at $N_{rp} = N_n = 4\times10^{16}$ cm^{-3}, and $N_{lp} = 6\times10^{16}$ cm^{-3}. Figure 13 shows

the maximum figure of merit values of the modified-UMOS at $H = 6$ μm. When the value of H is greater than 6 μm, the epitaxial layer is likely to be cut through. Therefore, $H = 6$ μm is selected for designing the n-pillars and p-pillars. Finally, the parameters in the above simulation and discussion are used. The figure of merit values of the two structures are calculated to be ~ 1.008 kV^2/(mΩ· cm^2) and ~ 0.563 kV^2/(mΩ· cm^2), respectively. The modified-UMOS is 79.0% higher than that of the conventional-UMOS.

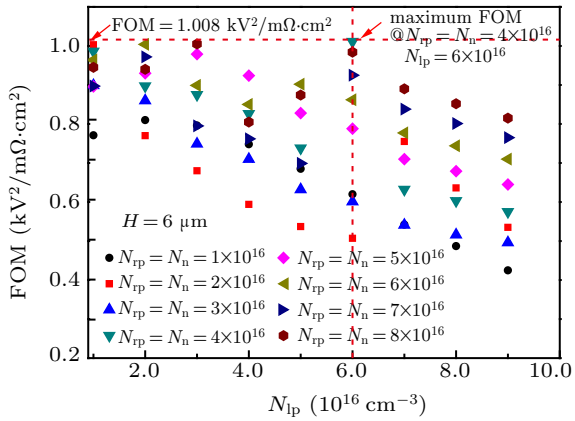


Fig. 12. FOM ($V_{BR}^2/R_{on,sp}$) as a function of N_{rp}, N_n, and N_{lp}, and with pillar height $H = 6$ μm.

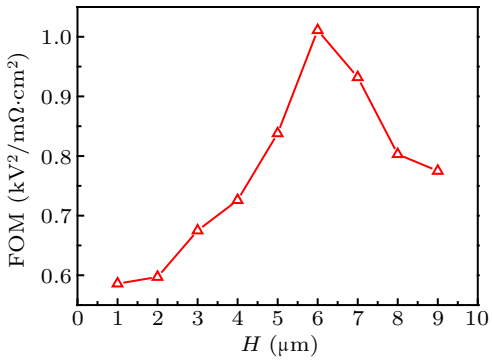


Fig. 13. FOM *versus* column height of modified UMOS.

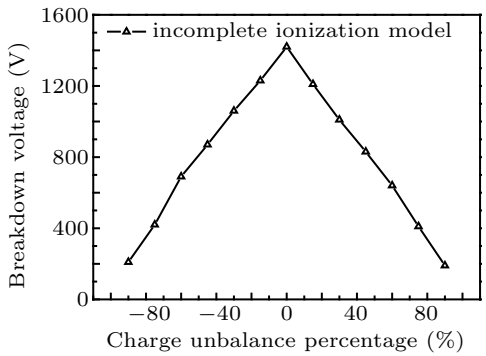


Fig. 14. Simulated V_{BR} *versus* unbalance ratio for device structure with the impact ionization model.

Figure 14 shows that the simulated V_{BR} *versus* unbalance ratio for the device structure with the impact ionization models, where the unbalance ratio is defined as $100 \times \text{abs}(N_D - N_A)/\max(N_A, N_D)$. For the balanced device, its charge imbalance (C.I.) is equal to 0% and is characterized by $N_D = N_A = 4 \times 10^{16}$ cm^{-3}. The unbalance is indicated as a percentage and defined as

$$\text{C.I.} = \begin{cases} 100 \times \dfrac{N_D - N_A}{N_D}, & N_D \geq 4\times10^{16};\ N_A = 4\times10^{16}, \\ 100 \times \dfrac{N_A - N_D}{N_D}, & N_D = 4\times10^{16};\ N_A \leq 4\times10^{16}. \end{cases} \tag{4}$$

3.4. Gauss-doped super-junction shield region

The doping distribution in the super-junction shield region is shown in Fig. 15(a), in which the doping concentration in uniform-doped super-junction shield region is 4×10^{16} cm^{-3}, the doping concentration in Gauss-doped super-junction shield region is 1.0×10^{17} cm^{-3}, the doping concentration reduces 5.9×10^{15} cm^{-3}. Figure 15(b) shows the OFF-state characteristic curve of the Gauss-doped and uniform-doped region. The V_{BR} of the Gauss-doped is improved to 10.4% compared with that of the uniform-doped region.

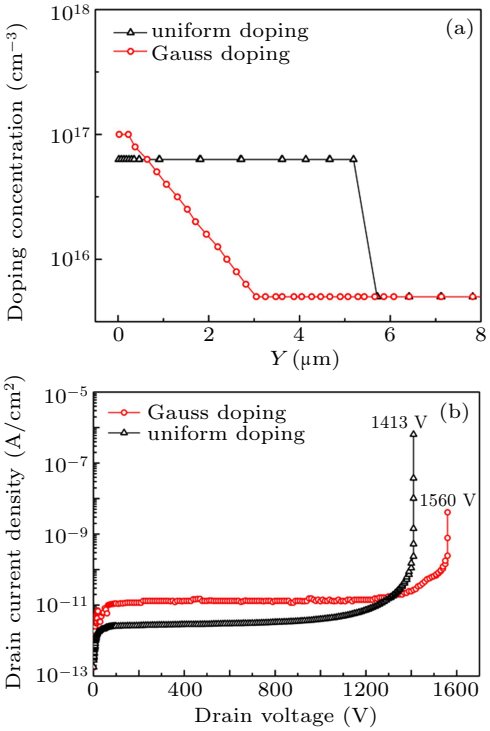


Fig. 15. (a) Variation of the doping concentration at super-junction of two structures with Y axis and (b) variation of drain current density with drain voltage in Gauss-doped region and uniform-doped region.

To compare the gate charges of the Gauss-doped and uniform-doped super-junction shield region, the gate charges of the two are simulated on condition that the total charge quantity of super-junction is the same, and the other parameters of the device are also the same. The time-varying curve of Q_g and V_{gs} of the super-junction shield region are shown in Fig. 16. According to the calculation, the Q_{gd} of uniform-doped super-junction shield region and Gauss-doped super-junction shield region are 307 nC/cm^2 and 327 nC/cm^2. It can be seen that under the condition of the same total charge quan-

tity of super-junction, gate-drain charge quantity in Gauss-doped and uniform-doped super-junction shield region are the same.

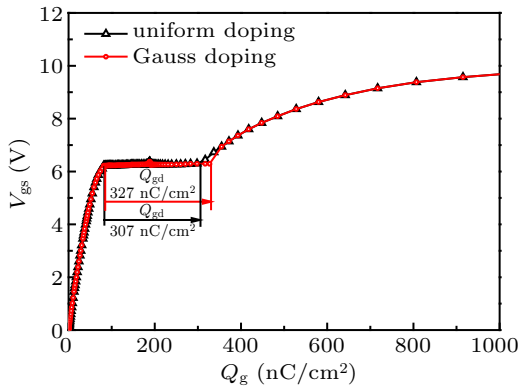


Fig. 16. Simulation curve of gate charge characteristics of Gauss-doped and uniform-doped super-junction shield region.

4. Conclusions

In this paper, an improved 4H-SiC UMOSFET with alternate n-pillars and p-pillars under the trench is investigated. The $R_{on,sp}$ of the modified structure reduces 22.2% compared with that of the conventional-UMOS. Moreover, the critical gate oxide E-field of the conventional-UMOS is higher than that of the modified-UMOS. The results in the breakdown voltage is improved by 21.1% in comparison with the results of the conventional-UMOS, thus avoiding a premature breakdown of the trench gate oxide. Furthermore, the modified structure shows excellent dynamic characteristics and reduces the switching energy loss. The calculated values of E_{on} and E_{off} for the modified-UMOS are 33.5 mJ/cm^2 and 32.9 mJ/cm^2, respectively, which show a decrease of 33.4% and 8.2% respectively, in comparison with the results of conventional-UMOS. The modified-UMOS structure shows a significant improvement over the conventional-UMOS. In addition, the Gauss-doped super-junction shield region can increase the V_{BR} of the device without degradation of dynamic performance. For device stability as well as switching speed considerations, we believe that the modified structure is more attractive and shows more promising for high power applications.

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