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Characteristics and mechanisms of subthreshold voltage hysteresis in 4H-SiC MOSFETs*

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In order to investigate the characteristics and mechanisms of subthreshold voltage hysteresis ($\Delta V_{\rm th,sub}$) of 4H-SiC metal–oxide–semiconductor field-effect transistors (MOSFETs), 4H-SiC planar and trench MOSFETs and corresponding P-type planar and trench metal–oxide-semiconductor (MOS) capacitors are fabricated and characterized. Compared with planar MOSFEF, the trench MOSFET shows hardly larger $\Delta V_{\rm th,sub}$ in wide temperature range from 25 °C to 300 °C. When operating temperature range is from 25 °C to 300 °C, the off-state negative $V_{\rm gs}$ of planar and trench MOSFETs should be safely above −4 V and −2 V, respectively, to alleviate the effect of $\Delta V_{\rm th,sub}$ on the normal operation. With the help of P-type planar and trench MOS capacitors, it is confirmed that the obvious $\Delta V_{\rm th,sub}$ of 4H-SiC MOSFET originates from the high density of the hole interface traps between intrinsic Fermi energy level ($E_{\rm i}$) and valence band ($E_{\rm v}$). The maximum $\Delta V_{\rm th,sub}$ of trench MOSFET is about twelve times larger than that of planar MOSFET, owing to higher density of interface states ($D_{\rm it}$) between $E_{\rm i}$ and $E_{\rm v}$. These research results will be very helpful for the application of 4H-SiC MOSFET and the improvement of $\Delta V_{\rm th,sub}$ of 4H-SiC MOSFET, especially in 4H-SiC trench MOSFET.

Keywords: 4H-SiC MOSFET, subthreshold voltage hysteresis, P-type MOS capacitor, density of interface states

PACS: 85.30.Tv, 43.66.Ed, 71.20.–b, 68.35.Dv **DOI:** 10.1088/1674-1056/abd391

1. Introduction

With the developments of silicon carbide (SiC) device processing and substrate crystal growth technique, many issues of SiC metal–oxide–semiconductor field-effect transistors (SiC MOSFETs) have been alleviated, such as low channel mobility, poor reliability and low yield. At present, 4H-SiC MOSFETs with voltages rating from 600 V to 1700 V are commercially available from several vendors. Generally speaking, higher power density can be achieved by either increasing the switching frequency of the converter to reduce the sizes of passive components or pushing the operating temperature of the power devices to simplify the cooling system.[1] Hence, 4H-SiC MOSFETs have been promising candidates to further improve the efficiency and power density of power electronic systems,[1] such as main inverter for vehicles,[2] industrial motor drives,[3] and traction converter. Due to the advantages of low power loss, high operating temperature, and high switching frequency.

With the increasing of switching frequency and operating temperature, the gate voltage oscillation of 4H-SiC MOSFET aggravates due to the existence of inevitable parasitic inductance in the package. Meanwhile, the threshold voltage ($V_{\rm th}$) of 4H-SiC MOSFET decreases due to the negative temperature coefficient of $V_{\rm th}$. When the gate–source voltage ($V_{\rm gs}$) spike is higher than the $V_{\rm th}$, the fault turn-on case of 4H-SiC MOSFET is triggered. In practical applications, the off-state negative $V_{\rm gs}$ is expected to be lower, enabling a wider voltage safety margin between $V_{\rm gs}$ spike and $V_{\rm th}$ to avoid fault turn-on case of devices. However, when a lower negative $V_{\rm gs}$ is used as turn-off voltage, there is an obvious subthreshold voltage hysteresis ($\Delta V_{\rm th,sub}$) case in commercial 4H-SiC MOSFEF,[4,5] especially in 4H-SiC trench MOSFET.[6] The $\Delta V_{\rm th,sub}$ causes a drain current overshoot at high $\mathrm{d}V/\mathrm{d}t$, as the overdrive $V_{\rm gs}$–$V_{\rm th}$ is momentarily higher.[7,8] On the other hand, the $\Delta V_{\rm th,sub}$ causes higher short-circuit peak current and higher energy dissipation during the short-circuit process, especially if a large number of chips is connected in parallel,[9] leading to the degradation of short-circuit withstanding time of 4H-SiC MOSFET.[10] Hence, it is very meaningful to investigate the characteristics and underlying mechanisms of $\Delta V_{\rm th,sub}$ in 4H-SiC MOSFETs for higher power density of power electronic systems.

At present, the high-temperature applications of 4H-SiC MOSFETs develop towards 300 °C.[11,12] However, the off-state negative $V_{\rm gs}$ dependence of $V_{\rm th,sub}$ in 4H-SiC MOSFET at 300 °C has not been studied.[5,13–16] On the other hand, the $\Delta V_{\rm th,sub}$ of 4H-SiC MOSFET could be caused by the interface traps or oxide traps in channel region.[6,17] As we all know,

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the commercial 4H-SiC MOSFEFs are n-channel, whose P-well region is formed by high temperature aluminum ion implantation. Hence, compared with N-type MOS capacitor, P-type MOS capacitor could be a better choice to investigate the properties of interface trap and gate oxide of 4H-SiC MOSFET. However, the P-type MOS capacitor has never been used to investigate the origin of $\Delta V_{\rm th,sub}$ in 4H-SiC MOSFET.

In this paper, the off-state negative $V_{\rm gs}$ dependence of $\Delta V_{\rm th,sub}$ is systematically investigated for 4H-SiC planar and trench MOSFET in wide temperature range from 25 °C to 300 °C. Considering the $\Delta V_{\rm th,sub}$ phenomenon could be caused by the interface traps or oxide traps in channel region, the P-type planar and trench MOS capacitors are fabricated following the planar and trench MOSFETs processing, respectively. With the help of P-type planar and trench MOS capacitors, interface traps properties of channel regions in 4H-SiC planar and trench MOSFETs are extracted while underlying mechanisms of $\Delta V_{\rm th,sub}$ in the corresponding MOSFETs are investigated.

This paper is organized as follows. In Section 2, the fabrication and measurements of devices are presented briefly. In Section 3, the $\Delta V_{\rm th,sub}$ characteristics of planar and trench MOSFETs are presented, and the physical mechanisms of $\Delta V_{\rm th,sub}$ are discussed and analyzed in detail. In Section 4 conclusions are drawn.

2. Experiments and measurements

2.1. Device fabrication

The 4H-SiC planar and trench MOSFETs are fabricated on the N-type, 4° off (0001) oriented, 4H-SiC epitaxial wafers using an industrial process. The gate oxide in planar MOSFET is thermally grown in dry oxygen at 1300 °C, and that in trench MOSFET is deposited via chemical vapor deposition, then they are post-annealed in 10% nitric oxide diluted in nitrogen. The thicknesses of fabricated gate oxide in planar and trench MOSFETs are 55 nm and 60 nm, respectively. In this experiment, the P-type planar and trench MOS capacitors are fabricated on the same epitaxial wafers following the processes of planar and trench MOSFETs, respectively.

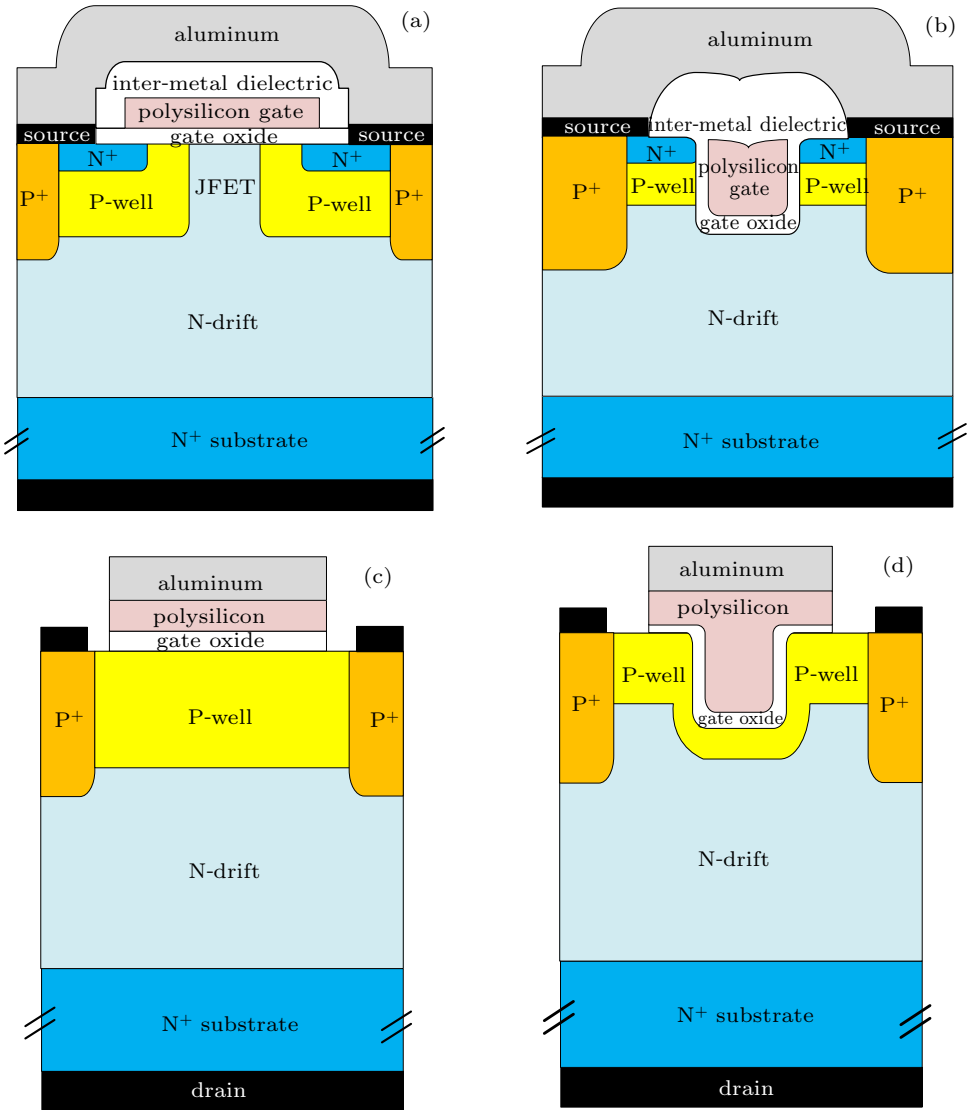


Fig. 1. Schematic cross-sections of the fabricated (a) planar MOSFET, (b) trench MOSFET, P-type (c) planar MOS, and (d) trench MOS capacitors.

In particular, the P-type body regions of P-type MOS capacitors are formed by the high temperature aluminum ion implantation. The gate oxide processes of P-type planar and trench MOS capacitors are the same to that of the corresponding MOSFETs, respectively. In addition, these P-type MOS capacitors undergo the same thermal budgets to the corresponding MOSFETs, including post-implantation high-temperature activation and ohmic contact formation processes. Hence, the P-type planar and trench MOS capacitors can be used to represent the properties of SiO_2/SiC interface of channel region in 4H-SiC planar and trench MOSFETs, respectively. The schematic cross-sections of aforementioned devices are shown in Fig. 1.

2.2. Device measurement

All the characteristics of devices are measured by using Agilent B1505A device analyzer with cascade MPS150 COAX probe station and temperature controller ATT systems. The off-state negative V_{gs} dependence of bidirectional drain–source current (I_{ds})–V_{gs} characteristics is evaluated on the planar and trench MOSFET at 25 °C, 150 °C, and 300 °C, respectively. In the measurement of bidirectional I_{ds}–V_{gs} curves, the up-sweep starts from different off-state negative V_{gs} to on-state positive V_{gs}, then returns to the same off-state negative V_{gs}. During this sweep, the drain voltage (V_d) is 0.1 V, and V_{gs} is switched by a value of 0.1 V every 100 ms for the V_{gs} sweep. The $\Delta V_{th,sub}$ is extracted from the bidirectional I_{ds}–V_{gs} curves as shown in Fig. 2. Here, the $V_{th,sub}$ is defined as V_{gs} at $I_{ds} = 10$ nA.

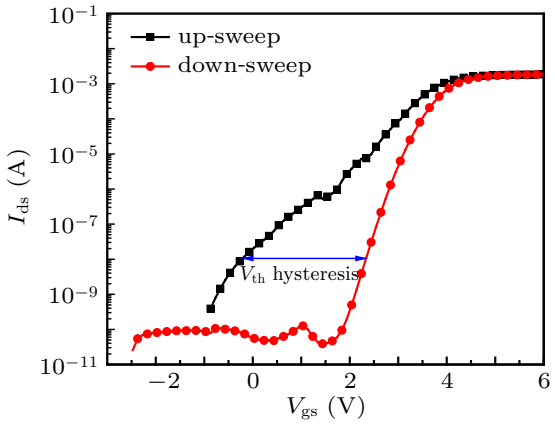


Fig. 2. Bidirectional I_{ds}–V_{gs} curves of 4H-SiC trench MOSFET at 25 °C.

The capacitance–voltage (C–V) hysteresis caused by negative gate voltage bias is evaluated on the P-type planar and trench MOS capacitor at 25 °C and 300 °C, respectively. The tested frequency is 100 kHz. The gate voltage starts from −25 V to 10 V, then returns to −25 V. The distribution of density of interface states (D_{it}) in bandgap are extracted by high-low method at different temperatures. As the paper[18] reported, the distribution of D_{it} near valence band (E_v) can be determined at 25 °C while that near middle bandgap can be determined at 300 °C. The high frequency (100 kHz) and quasi-static C–V ($QSCV$) curves of P-type planar and trench MOS capacitors are measured at 25 °C and 300 °C, and the sweep direction of C–V is from accumulation to depletion.

3. Results and discussion

3.1. $\Delta V_{th,sub}$ characteristics of planar and trench MOSFETs

The off-state negative V_{gs} dependences of $\Delta V_{th,sub}$ at 25 °C, 150 °C, and 300 °C are shown in Fig. 3. For planar MOSFET, the maximum $\Delta V_{th,sub}$ is −0.25 V, −0.12 V, and −0.05 V at 25 °C, 150 °C, and 300 °C, respectively. For trench MOSFET, the maximum $\Delta V_{th,sub}$ is −3.0 V, −3.1 V, and −2.6 V at 25 °C, 150 °C, and 300 °C, respectively. Compared with planar MOSFET, the trench MOSFET shows larger $\Delta V_{th,sub}$ at 25 °C, 150 °C, and 300 °C. In addition, whether it is planar or trench MOSFET, the maximum $\Delta V_{th,sub}$ decreases with temperature increasing from 25 °C to 300 °C. On the other hand, it is obvious that the minimum saturation negative V_{gs} of $\Delta V_{th,sub}$ in trench MOSFET is lower than that of planar MOSFET. Meanwhile, whether it is planar or trench MOSFET, the minimum saturation negative V_{gs} of $\Delta V_{th,sub}$ decreases with temperature increasing from 25 °C to 300 °C. When the operating temperature is ranging from 25 °C to 300 °C and $\Delta V_{th,sub}$

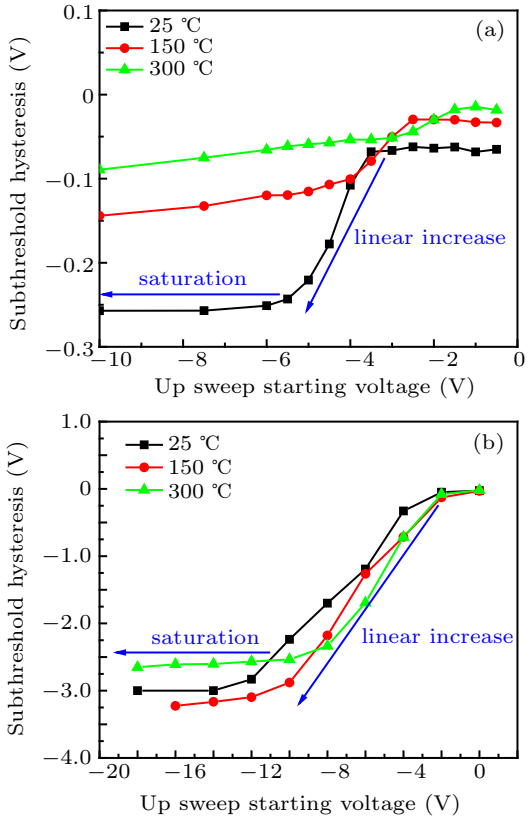


Fig. 3. Dependence of $\Delta V_{th,sub}$ of SiC MOSFETs on off-state negative V_{gs} at different temperatures: (a) planar MOSFETs, (b) trench MOSFETs.

is less than 0.1 V, the off-state negative V_{gs} of planar and trench MOSFETs should be above −4 V and −2 V, respectively. In other words, in order to alleviate $\Delta V_{th,sub}$, the off-state negative V_{gs} of planar MOSFET is accepted above −4 V while trench MOSFET above −2 V.

3.2. *C–V* hysteresis of planar and trench MOS capacitor

The measured *C–V* hysteresis caused by negative gate voltage bias is shown in Fig. 4. When the *C–V* sweep is from −25 V to 10 V, there is a shift toward the negative direction in the *C–V* curves. It is indicated that the holes are captured at negative gate voltage stress bias, which affect actually the net charge of the MOS system. Because the voltage sweep is too fast for interface to reach the thermodynamic equilibrium.[5] As a result, a measurable *C–V* hysteresis appears in the P-type MOS capacitor. Compared with planar MOS capacitor, the trench MOS capacitor shows larger *C–V* hysteresis at 25 °C and 300 °C. As figure 3 shows, the maximum $\Delta V_{th,sub}$ in trench MOSFET is also larger than that in planar MOSFET. Thus, it is confirmed that the tendency for *C–V* hysteresis to occur depending on the gate oxide of the P-type MOS capacitor is in accord with maximum $\Delta V_{th,sub}$ of the corresponding MOSFET. It is indicated that the P-type MOS capacitor can be utilized to instead of 4H-SiC MOSFET to investigate the $\Delta V_{th,sub}$ properties. On the other hand, with the temperature increasing from 25 °C to 300 °C, the *C–V* hysteresis decreases in trench MOS capacitor. It is indicated that the net charge at the SiO_2/SiC interface can reach easily thermodynamic equilibrium due to the decrease of emission constant time of trapped hole. This tendency is also similar to maximum $\Delta V_{th,sub}$ in trench MOSFET.

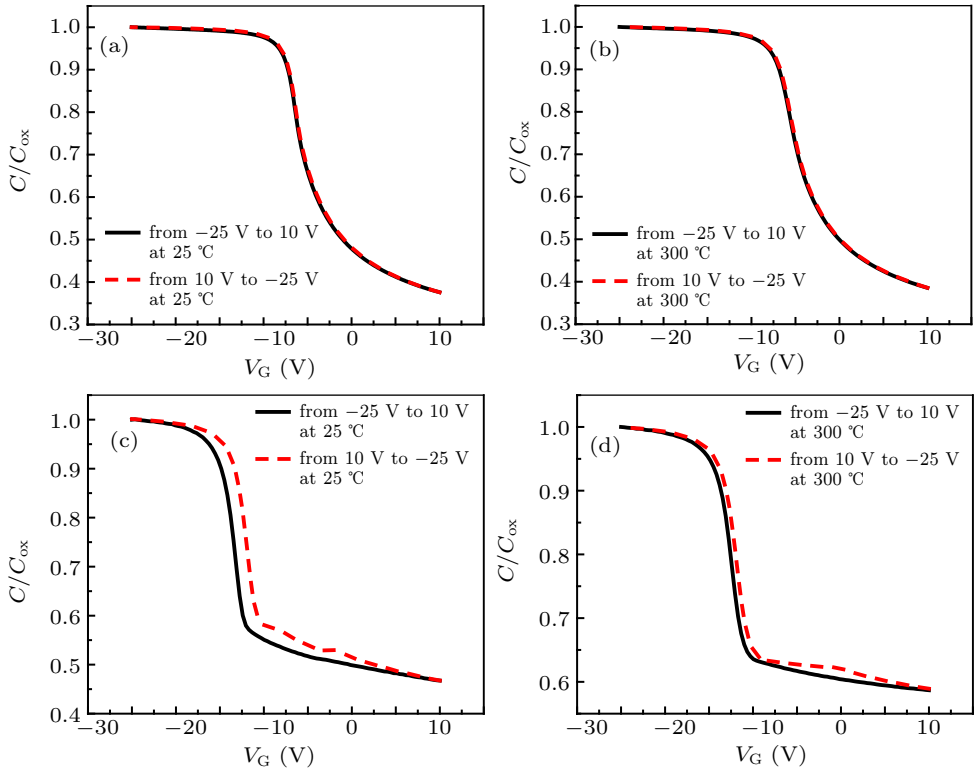


Fig. 4. High frequency (100 kHz) *C–V* cycle curves of P-type MOS capacitors at 25 °C and 300 °C: (a)–(b) planar MOS capacitor, (c)–(d) trench MOS capacitor.

3.3. Traps distribution at SiO_2/SiC interface

The high frequency (100 kHz) *C–V* and *QSCV* at 25 °C and 300 °C are shown in Fig. 5. Whether it is P-type planar or trench MOS capacitor, the C/C_{ox} value at 100 kHz is lower than that of the quasi-static one. It could be explained by that the holes are trapped at starting negative gate voltage bias and functioned as series resistance to the MOS capacitor. With the *C–V* frequency increasing from quasi-static to 100 kHz, the series resistance shows more obvious influence on the C/C_{ox} value. Whether it is 25 °C or 300°C, the different C/C_{ox} between 100 kHz and quasi static ($\Delta C/C_{ox}$) in the trench MOS capacitor is larger than that in the planar one. It is indicated that more holes are trapped in the trench MOS capacitor at negative gate voltage bias. Whether it is planar or trench MOS, the $\Delta C/C_{ox}$ value decreases with temperature increasing from 25 °C to 300 °C. It could be explained by that the emission constant times of trapped holes near E_v decrease with the increase of temperature. The emission constant time for trapped hole from an interface state to the E_v in a P-type semiconductor can be written as[18]

$$\tau_p(E) = \frac{1}{\sigma_p \upsilon_T N_v} \exp\left(\frac{E - E_v}{kT}\right), \tag{1}$$

where σ_p is the capture cross section for hole, υ_T is the thermal velocity, N_v is the effective density of states in the E_v, κ is Boltzmann's constant, T is the absolute temperature, and $E - E_v$ is the energy of the interface state relative to the E_v. With the temperature increasing form 25 °C to 300 °C, the τ_p for trapped hole decreases so that a part of trapped holes near the E_v is fast enough emitted into E_v during high frequency (100 kHz) C–V sweep. Consequently, less trapped holes are functioned as series resistance, resulting in the decrease of $\Delta C/C_{ox}$.

The distribution of D_{it} is extracted by using high-low method at different temperatures, as shown in Fig. 6. The D_{it} in SiO_2/4H-SiC interface is about two orders higher than that in SiO_2/Si interface. On the other hand, the bandgap of 4H-SiC is 3.26 eV, which is three times wider than that of silicon. As equation (1) described, the interface traps near the middle bandgap of 4H-SiC have longer emission constant time than that of silicon. Consequently, when 4H-SiC MOSFET is at the off-state negative V_{gs} bias, more holes are trapped so that the inversion charge in the channel is temporarily enhanced before being gradually neutralized. It could be the root cause of the obvious $\Delta V_{th,sub}$ phenomenon of 4H-SiC MOSFET. Compared with the planar MOS capacitor, trench MOS capacitor shows one order of magnitude higher D_{it} in the energy level range from 1.63 eV to 3 eV. Therefore, the maximum $\Delta V_{th,sub}$ of trench MOSFET is larger than that of planar MOSFET. The maximum $\Delta V_{th,sub}$ can be written as[7]

$$\text{maximum}\,\Delta V_{th,sub} = \frac{t_{ox}}{\varepsilon_r \varepsilon_0}\left(q\int_{E_1}^{E_2} D_{it}(E)\,\mathrm{d}E\right), \qquad (2)$$

where maximum $\Delta V_{th,sub}$ is the maximum subthreshold voltage hysteresis, ε_r is the relative dielectric constant of SiO_2, ε_0 is the vacuum permittivity, t_{ox} is the gate oxide thickness, q is the hole charge, D_{it} is the density of interface states, E_1 is intrinsic Fermi energy level (E_i), and E_2 is Fermi energy level at minimum saturation off-state negative V_{gs} bias. For planar MOSFET, the minimum saturation off-state negative V_{gs} is −6 V at 25 °C, −4 V at 150 °C, and −3 V at 300 °C. The corresponding E_2 can be calculated as 2.8 eV at 25 °C, 2.3 eV at 150 °C, and 2.08 eV at 300 °C. According to the Eq. (2), the maximum $\Delta V_{th,sub}$ in planar MOSFET can be calculated as 0.2 V at 25 °C, 0.04 V at 150 °C, and 0.02 V at 300 °C, respectively, which have similar trend to the tested values. For trench MOSFET, the minimum saturation off-state negative V_{gs} is −14 V at 25 °C, −12 V at 150 °C, and −10 V at 300 °C. The corresponding E_2 can be calculated as 3.16 eV at 25 °C, 3.08 eV at 150 °C, and 3 eV at 300 °C. Because of limitation of high frequency (100 kHz), only the D_{it} between 1.6 eV and 3.06 eV can be extracted. As a result, only the maximum $\Delta V_{th,sub}$ in trench MOSFET at 300 °C can be calculated as 4.51 V. Based on the above analysis, the $\Delta V_{th,sub}$ phenomenon of 4H-SiC MOSFET originates from the high density of hole interface traps between E_i and E_v.

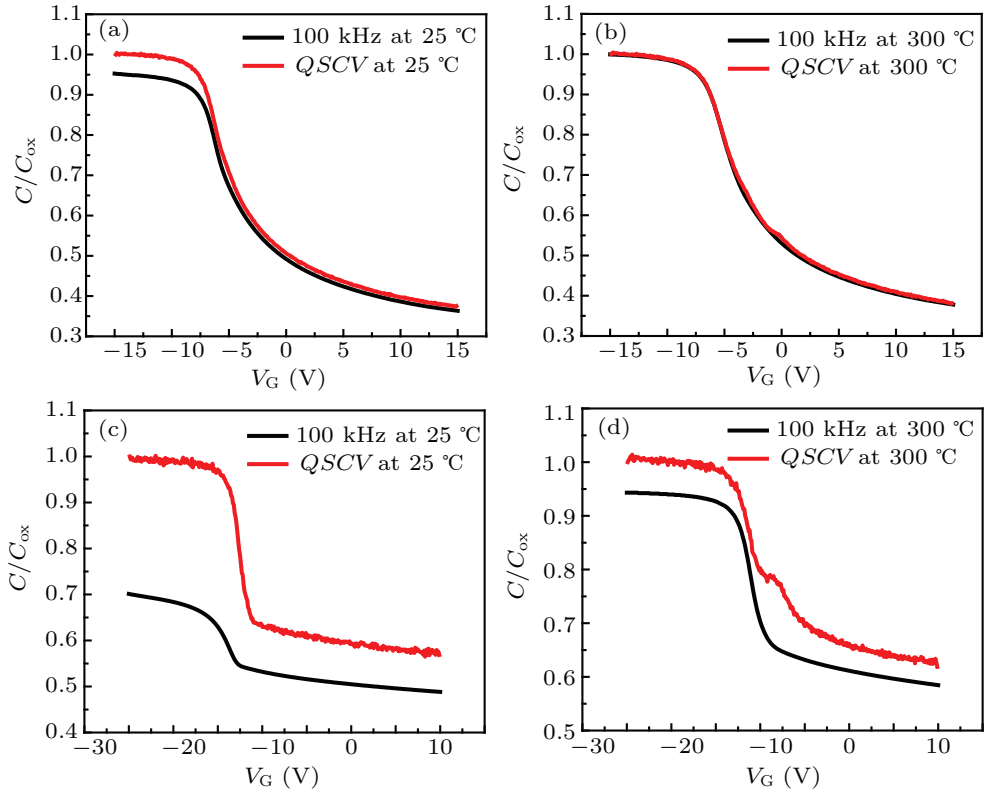


Fig. 5. High frequency (100 kHz) and quasi static C–V curves of P-type MOS capacitors at 25 °C and 300 °C: (a)–(b) planar MOS capacitor, (c)–(d) trench MOS capacitor.

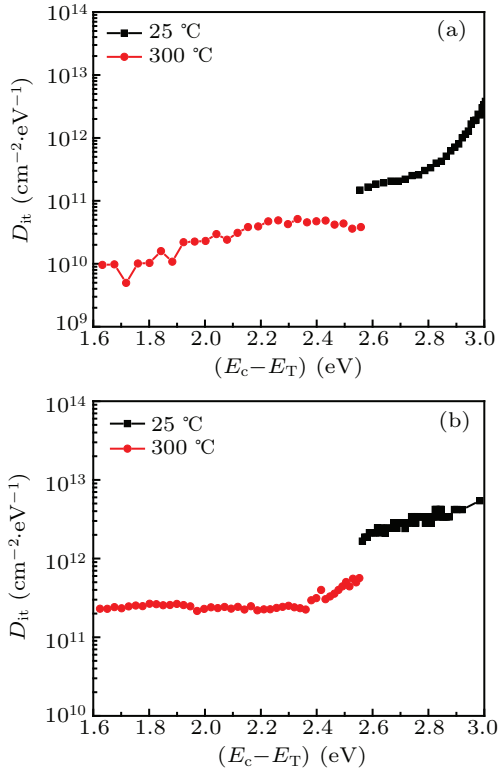


Fig. 6. D_{it} as a function of the energy on P-type MOS capacitors: (a) planar MOS capacitor, (b) trench MOS capacitor.

4. Conclusion

In this paper, the characteristics and mechanisms of $\Delta V_{th,sub}$ are investigated for 4H-SiC planar and trench MOSFETs. Compared with planar MOSFEF, trench MOSFET shows larger $\Delta V_{th,sub}$ in the temperature range from 25 °C to 300 °C. Furthermore, whether it is planar or trench MOSFET, both maximum $\Delta V_{th,sub}$ and corresponding saturation negative V_{gs} decreases with temperature increasing from 25 °C to 300 °C. In order to alleviate the effect of $\Delta V_{th,sub}$ on normal operation, the off-state negative V_{gs} of planar and trench MOSFET should be above −4 V and −2 V, respectively. Furthermore, it is confirmed that the tendency for *C*–*V* hysteresis to occur depending on the gate oxide of the P-type MOS capacitor is in accord with maximum $\Delta V_{th,sub}$ of the corresponding MOSFET. The obvious $\Delta V_{th,sub}$ of 4H-SiC MOSFET is caused by the high density of hole interface traps between E_i and E_v. The maximum $\Delta V_{th,sub}$ of trench MOSFET is about twelve times larger than that of planar MOSFET, owing to the one order of magnitude higher D_{it}. In order to improve the $\Delta V_{th,sub}$ of 4H-SiC MOSFET, the high D_{it} between E_i and E_v should be further improved, especially in 4H-SiC trench MOSFET.

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