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Citation: Chin. Phys. B, 2021, 30 (**4**): 047401. DOI: 10.1088/1674-1056/abd2a2
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Device physics and design of FD-SOI JLFET with step-gate-oxide structure to suppress GIDL effect*

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(Received 17 August 2020; revised manuscript received 7 December 2020; accepted manuscript online 11 December 2020)

A novel n-type junctionless field-effect transistor (JLFET) with a step-gate-oxide (SGO) structure is proposed to suppress the gate-induced drain leakage (GIDL) effect and off-state current I_{off}. Introducing a 6-nm-thick tunnel-gate-oxide and maintaining 3-nm-thick control-gate-oxide, lateral band-to-band tunneling (L-BTBT) width is enlarged and its tunneling probability is reduced at the channel–drain surface, leading the off-state current I_{off} to decrease finally. Also, the thicker tunnel-gate-oxide can reduce the influence on the total gate capacitance of JLFET, which could alleviate the capacitive load of the transistor in the circuit applications. Sentaurus simulation shows that I_{off} of the new optimized JLFET reduced significantly with little impaction on its on-state current I_{on} and threshold voltage V_{TH} becoming less, thus showing an improved I_{on}/I_{off} ratio (5×10^4) and subthreshold swing (84 mV/dec), compared with the scenario of the normal JLFET. The influence of the thickness and length of SGO structure on the performance of JLFET are discussed in detail, which could provide useful instruction for the device design.

Keywords: junctionless field-effect transistor (FET), gate-induced drain leakage (GIDL), step-gate-oxide, off-state current

PACS: 74.55.+v, 85.30.Tv, 85.30.De **DOI:** 10.1088/1674-1056/abd2a2

1. Introduction

Scaled down into nanometers, conventional Si MOSFETs are facing the problems of forming ultra-steep doping profile in p–n junctions,[1–4] and field-effect transistors (FETs) without junctions, *i.e.*, junctionless FETs (JLFETs) were proposed to eliminate the stringent requirement.[5–10] Unlike "regular" p–n junction-based FET, the JLFET usually has the same uniform doping concentration in the source, channel and drain region. The metal with large work function is introduced as gate electrode to deplete the entire channel region at zero biased gate voltage ($V_{GS} = 0$ V).[11–13] In the on-state, the depletion region under the gate dies away and the entire channel region becomes neutral, allowing carriers to flow from drain to source. Therefore, the JLFET is working in the flatband mode or accumulation mode, which is very different from the inversion mode-mechanism of MOSFET. Due to these reasons, the JLFET fetures simplified fabrication process, large on-state current I_{on}, excellent drive capability and is a promising candidate as crucial components for the future electronics industry.

However, to ensure the full depletion of the channel by gate at zero bias, the gate electrode with large work function (such as 5.1 eV for n-JLFET, 4.3 eV for p-JLFET, *etc.*) and the channel with thin thickness is preferred. Thus, a serious gate-induced drain leakage (GIDL) effect is caused due to the considerable lateral band-to-band tunneling (L-BTBT)[14,15] at channel–drain surface in the off-state, thus increasing the off-state current I_{off} finally.[16–18]

To suppress the GIDL effect in JLFET, several efforts have been made to reduce the tunneling probability $T(E)$ of L-BTBT, such as JLFET with hole sink layer (HS JLFET),[19] JLFET with hetero-dielectric buried oxide (HDB JLFET),[20] JLFET with hetero-gate dielectric (HGD JLFET),[21] JLFET with dual material gate (DMG JLFET),[14] JLFET with core-shell architecture (CS JLFET),[22] JLFET with tunnel dielectric (TD JLFET),[23] *etc*. However, these devices usually cause other issues, hindering their applications. The HS JLFET consisting of a doped p–n junction suffers the creation of such an abrupt junction and its on-state current is low ($\sim$ 3.3 times) as compared with the SOI JLFET's. In the HDB JLFET, the interface between the high-k dielectric and SiO_2 in the buried oxide (BOX) region must be appropriately aligned with the channel–drain interface, which requires a stringent control of the wafer fabrication process. The HGD JLFET encountered the same issues, fabricating the hetero-gate dielectric and alignment of the hetero-dielectric interface in the middle of the channel region are the major issues concerning the HGD JLFETs. The DMG JLFET is also facing the fabrication problem, since achieving distinct gate materials within a span of 20 nm itself is a technological challenge. The CS JLFET also needs to

*Project supported by the National Natural Science Foundation of China (Grant No. 61704130) and the Fund from the Science and Technology on Analog Integrated Circuit Laboratory, China (Grant No. JCKY2019210C029).

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create an abrupt junction at the core–shell interface through using the industry standard ion implantation process which is not feasible and has the same technological challenges faced while fabricating nanowires. Due to the defects and traps introduced by TD in the center of the channel, the TD JLFET faces the problems of dielectric semiconductor interface which should be further suppressed. To solve the issues above, we have proposed two types of JLFET based on fully depleted SOI (FD-SOI) substrate with field plate (FP) structure[24] and lightly doped drain (LDD) structure,[25] respectively, to suppress the GIDL effect, but the FP structure needs additionally another type of metal to enhance the performance of the device, and LDD structure causes the on-state resistance to increase, thus reducing the on-state current of the device.

In this paper, a novel n-type JLFET based on FD-SOI with a step-gate-oxide (SGO) structure is proposed to suppress the GIDL effect and $I_{\rm off}$. With the help of step-gate-oxide, the tunneling width in the region where drain and channel are overlapped is enlarged and the tunneling probability is reduced, which leads the GIDL current to be suppressed significantly. The Sentaurus simulation results indicate that the $I_{\rm off}$ of the SGO-JLFET decreases significantly with little impaction on its on-state current $I_{\rm on}$ and threshold voltage $V_{\rm TH}$. So its $I_{\rm on}/I_{\rm off}$ ratio is enhanced by 37 times compared with that of the normal JLFET, and subthreshold swing (*SS*) increases to 84 mV/dec. Meanwhile, the thicker tunnel-gate-oxide can weaken the influence on the total gate capacitance of JLFET, which can alleviate the capacitive load of the transistor in the circuit applications. The influences of the structure of step-gate-oxide, such as $T_{\rm Toxide}$ (thickness of the tunnel oxide), $L_{\rm Toxide}$ (length of the tunnel oxide), $L_{\rm Coxide}$ (length of the control oxide) are discussed in detail, which could provide useful instruction for the device design.

2. Device structure and simulation parameters

Figure 1 shows the cross-section of the normal JLFET and step-gate-oxide JLFET (SGO JLFET), respectively. Comparing with the normal JLFET, the gate oxide in the SGO JLFET is composed of two parts: control oxide and tunnel oxide. Just as in the normal JLFET, The control oxide near source region in the novel JLFET is used to shut down the device when $V_{\rm GS} = 0$ V, and the tunnel oxide near drain region is used to reduce the tunneling probability $T(E)$ of L-BTBT between channel and drain. When $V_{\rm GS}$ is increasing, the depletion region under tunnel oxide vanishes first, and then the depletion region under control oxide vanishes, turning the device on.

The simulation device parameters are listed in Table 1. Simulations are carried out by using the Sentaurus TCAD. In the simulations, the length and thickness of the tunnel oxide are chosen to be 10 nm and 6 nm, respectively, and the thickness of control oxide and channel are 3 nm and 7 nm, respectively. The channel of the normal JLFET and novel JLFET are uniformly doped (1×10^{19} cm^{-3}) and the metal of gate electrode is Au to ensure that the channel is fully depleted in off-state. High-k material of HfO2 is used as gate dielectric for both control oxide and tunnel oxide.

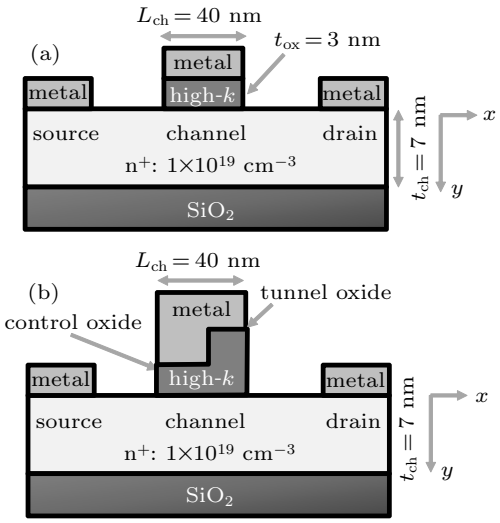


Fig. 1. Cross-section of device structures of (a) normal JLFET and (b) SGO JLFET.

Table 1. Simulated device parameters used in this study.

Parameter	SGO JLFET	Normal JLFET
Gate length $L_{\rm ch}$ (nm)	40	40
Tunnel oxide thickness $T_{\rm Toxide}$ (nm)	6	/
Tunnel oxide length $L_{\rm Toxide}$ (nm)	10	/
Gate work function (eV)	5.1	5.1
Source/drain/channel doping (10^{19} cm^{-3})	1	1
Device layer thickness $T_{\rm ch}$ (nm)	7	7
Control oxide thickness $T_{\rm Coxide}$ (nm)	3	3

The simulation models used in Ref. [26] are implanted into our simulations. The nonlocal BTBT model is considered for the band-to-band tunneling of charge carriers between drain and channel. Due to the high doping level, the bandgap narrowing (BGN) model is also included, because the effective bandgap directly influences the tunneling current. Also, the Shockley–Read–Hall (SRH) recombination model is included due to the presence of high impurity atom concentration in the channel, and Fermi–Dirac statistics is included to calculate the intrinsic carrier concentration. For more accurate current calculations, the field-dependent and doping-dependent mobility degradation models and the drift-diffusion current transport model, are also considered.

3. Results and discussion

Figure 2 shows the transfer curves of normal JLFET and SGO JLFET. For normal JLFET at $V_{\rm DS} = 1$ V, with the decrease of the gate voltage $V_{\rm GS}$, the drain current first decreases until it reaches its minimum value, and then starts to increase again due to GIDL effect, resulting in an off-state current with a value of 4.4×10^{-7} A/μm. However, for the SGO JLFET, an

off-state current of 1.23×10^{-8} A/μm is achieved at $V_{GS}=0$ V, $V_{DS}=1$ V due to step-gate-oxide structure, decreased by 37 times compared with that in normal JLFET. Meanwhile, since the little influence of step-gate-oxide on channel in the on-state, both of the extracted threshold voltage (V_{TH}) of SGO JLFET and normal JLFET are 0.25 V by the trans-conductance (g_m) derivative method at $V_{DS}=0.1$ V,[27] and the on-state current remains almost the same (6×10^{-4} A/μm) compared with that in the normal JLFET. Therefore, the SGO JLFET exhibits a high I_{on}/I_{off} ratio (5×10^4) compared with the normal JLFET (1.4×10^3). The extracted average subthreshold swing (SS) of SGO JLFET is 84mV/decade, which is also much better than the value of 190 mV/decade in normal JLFET.

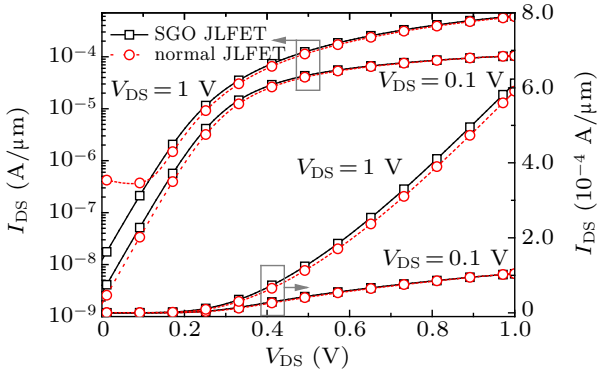


Fig. 2. Transfer characteristics of normal JLFET and SGO JLFET.

Figure 3 shows the comparison of the energy band diagram at the surface of the SGO JLFET with that at the surface of normal JLFET at $V_{DS}=1$ V, $V_{GS}=0$ V. The T_{w1} and T_{w2} represent the tunneling width of normal JLFET and SGO JLFET respectively. It can be observed that T_{w2} is much larger than T_{w1}. An enlarged tunneling width leads the tunneling of electrons from the channel region to the drain region to decrease, resulting in a significantly reduced BTBT probability $T(E)$ as shown in Fig. 4. Figure 4 shows the surface BTBT probability at channel–drain interface between the SGO JLFET and normal JLFET when $V_{DS}=1$ V and $V_{GS}=0$ V. It can be seen that the largest $T(E)$ in the SGO JLFET reduces about 5 orders of magnitude over that in the normal JLFET.

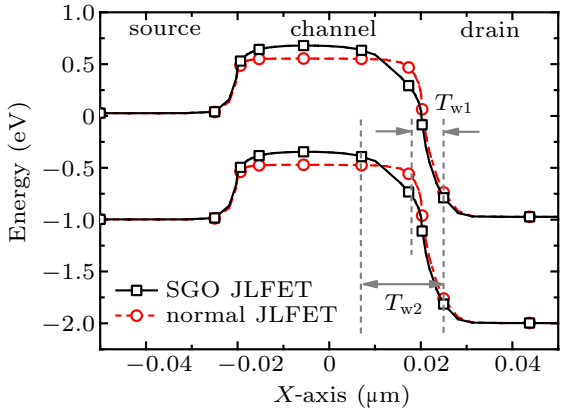


Fig. 3. Surface band diagram of normal JLFET and SGO JLFET at $V_{DS}=1$ V and $V_{GS}=0$ V.

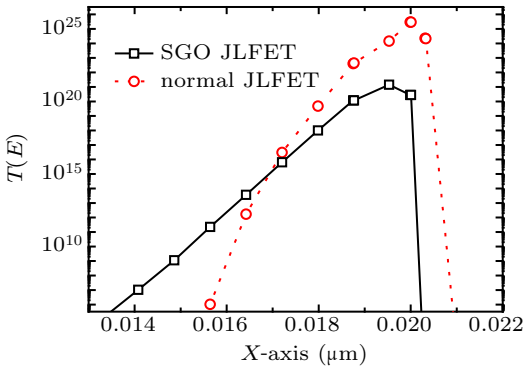


Fig. 4. Surface BTBT probability plot at gate/drain interface when $V_{DS}=1$ V and $V_{GS}=0$ V.

Figure 5 shows the curve of surface hole density *versus* V_{GS} in the channel of SGO JLFET and normal JLFET at $V_{GS}=0$ V, $V_{DS}=1$ V. It can be clearly seen that the value of hole density under tunnel oxide in the SGO JLFET is much lower than that in the same region of the normal JLFET, resulting in the enlargement of tunneling width as shown in Fig. 3. Meanwhile, it can be seen that the hole density under the control oxide in the SGO JLFET is also less than that in the normal JLFET, which is mainly caused by the reduction of total gate capacitance (C_{gg}).

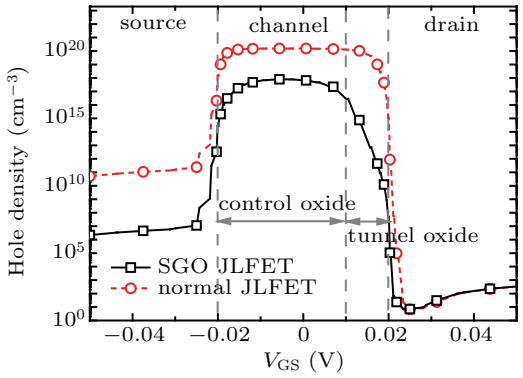


Fig. 5. Surface hole concentration of normal JLFET and SGO JLFET at $V_{GS}=0$ V and $V_{DS}=1$ V.

Figure 6 shows the total gate capacitance of the SGO JLFET and the normal JLFET by computing the frequency-dependent admittance matrix in mixed-mode simulations. The total gate capacitance of the SGO JLFET can be calculated by

$$\frac{1}{C_{gg}}=\frac{1}{C_{ox}}+\frac{1}{C_s}, \tag{1}$$

where C_s is the depletion capacitance given by ε_{Si}/T_{ch} and C_{ox} is the gate oxide capacitance given by

$$C_{ox}=C_{ox1}+C_{ox2}=\frac{\varepsilon_{ox}}{T_{Coxide}}+\frac{\varepsilon_{ox}}{T_{Toxide}}. \tag{2}$$

It can be seen from Eqs. (1) and (2) that a larger T_{Toxide} results in a less value of C_{gg}. Therefore, the total gate capacitance of SGO JLFET is smaller than that of normal JLFET as shown in Fig. 6.

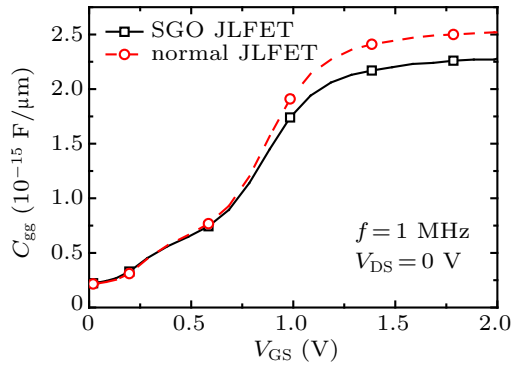


Fig. 6. Total gate capacitance of normal JLFET and SGO JLFET.

To show the influence of step-gate-oxide structure on I_{off} more clearly, the variation of the I_{DS}–V_{GS} curves with T_{Toxide} are simulated and shown in Fig. 7. It can be seen from the figure that the off-state current decreases from 4.4×10^{-7} A/μm to 1.2×10^{-8} A/μm without sacrificing the on-state current as T_{Toxide} increases from 3 nm to 6 nm. Since the increment increase of T_{Toxide} reduces the surface hole density under the tunnel oxide, the GIDL in SGO JLFET is inhibited and then I_{off} decreases as discussed above. With the increase of T_{Toxide}, the value of *SS* gradually decreases from 190 mV/dec to 84 mV/dec, and the I_{on}/I_{off} ratio increases from 1.3×10^4 to 4.9×10^4 as shown in Fig. 8.

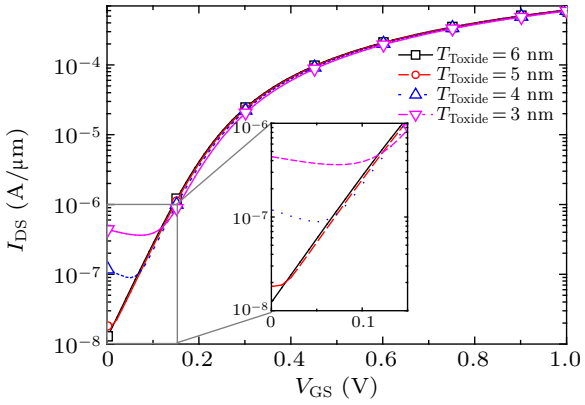


Fig. 7. Variation of I_{DS}–V_{GS} curves with V_{GS} for different values of T_{Toxide} in SGO JLFET.

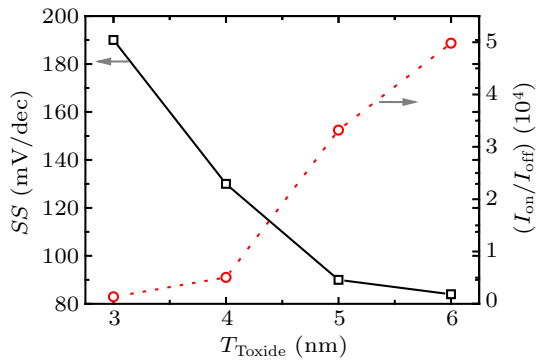


Fig. 8. Variation of *SS* and I_{on}/I_{off} ratio with T_{Toxide} in SGO JLFET.

Figures 9 and 10 show the influence of L_{Toxide} on I_{DS}–V_{GS}, *SS*, and I_{on}/I_{off} ratio at $V_{DS} = 1$ V clearly. A larger L_{Toxide} results in a wider tunnel path at $V_{GS} = 0$ V, and restricts GIDL more significantly. So, when L_{Toxide} is changed from 5 nm to 10 nm, the off-state current I_{off} of SGO JLFET at $V_{GS} = 0$ V decreases from 5×10^{-8} A/μm to 1.23×10^{-8} A/μm with influence on the on-state current weakening, thus, reducing the *SS* from 109 mV/dec to 84 mV/dec and increasing the I_{on}/I_{off} ratio from 1.2×10^4 to 5×10^4 as shown in Fig. 10. However, A larger L_{Toxide} shortens the length of control oxide due to $L_{ch} = L_{Toxide} + L_{Coxide}$, which means the effective depletion length of channel determined by L_{Coxide} in the off-state decreases with the L_{Toxide} increasing, so the off-state current I_{off} increases again and obtains a value of 3.24×10^{-8} A/μm, the *SS* and I_{on}/I_{off} ratio reach a value of 91 mV/dec and 1.9×10^4 at $L_{Toxide} = 20$ nm, respectively.

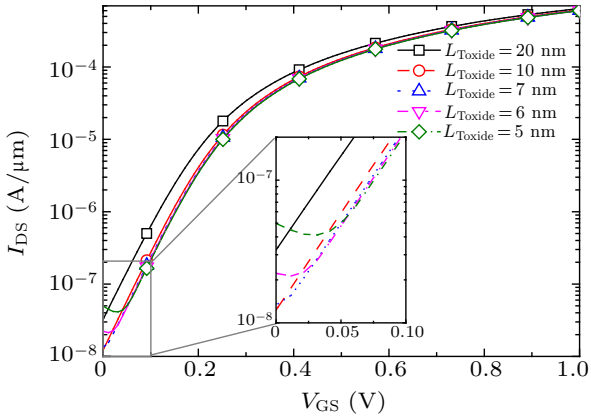


Fig. 9. Variations of I_D–V_{GS} curves for different values of L_{Toxide} in SGO JLFET.

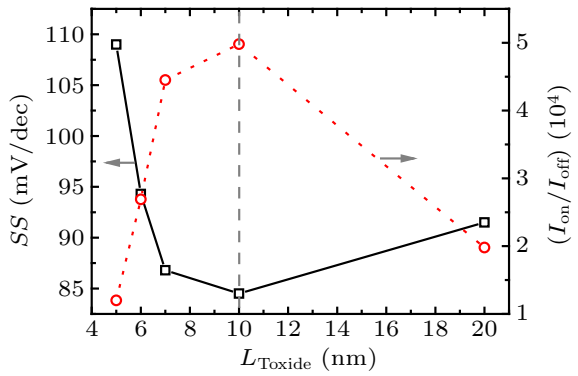


Fig. 10. *SS* and I_{on}/I_{off} ratio *versus* L_{Toxide} in SGO JLFET.

To clearly show the influence of L_{Coxide} on the performance of the SGO JLFET, the I_{DS}–V_{GS} curves of SGO JLFET with L_{Coxide} changing from 10 nm to 30 nm in steps of 10 nm are shown in Fig. 11. As indicated in Fig. 11, the change of the control gate length L_{Coxide} has little effect on the on-state current. However, since the length of depletion region under control oxide decreases with L_{Coxide} decreasing, the off-state current I_{off} changes from 1.23×10^{-8} A/μm to 1.03×10^{-5} A/μm, and the I_{on}/I_{off} ratio changes from 5×10^4 to 59, thereby deteriorating the performance of the SGO JLFET.

Figure 12 shows the output characteristics of the SGO JLFET with different gate voltages. The drain current I_{DS}

separately at $V_{GS} = 0.25$ V, 0.5 V, 0.75 V, and 1 V first increases and then reaches saturation at high drain voltages, and I_{DS} at $V_{DS} = 1$ V increases from 1.12×10^{-5} A/μm to 6.12×10^{-4} A/μm as V_{GS} increases from 0.25 V to 1 V, showing good conduction characteristics.

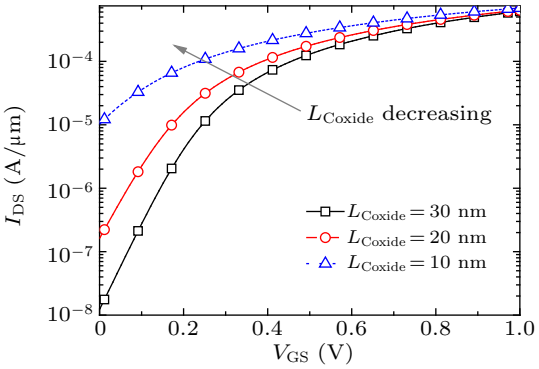


Fig. 11. Transfer curves for different values of L_{Coxide} in SGO JLFET.

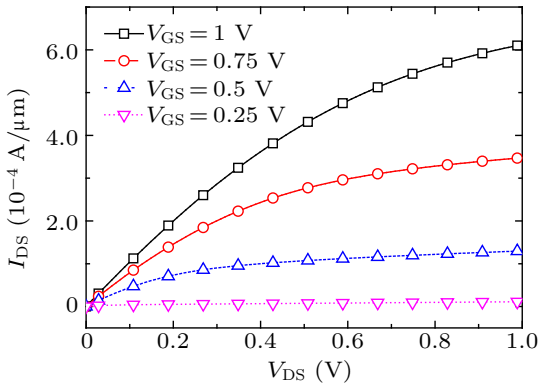


Fig. 12. I_{DS}–V_{DS} curves in SGO JLFET for different values of V_{GS}.

4. Conclusions

In this paper, a novel FD-SOI JLFET with step-gate-oxide structure is proposed to improve the *I*–*V* performance. Using the Sentaurus TCAD tool, the new step-gate-oxide architecture is demonstrated to be able to effectively broaden the tunneling width of L-BTBT in the drain–channel overlap region, thereby reastricting the GIDL effect. Thus, compared with the normal JLFETs, the proposed architecture reduces the off-state current and does not deteriorate the on-state current or V_{TH}, resulting in a significant enhancement of *SS* and I_{on}/I_{off} ratio. The influence of T_{Toxide}, L_{Toxide}, and L_{Coxide} on the performance of SGO JLFET are also examined, which could provide useful instructions for designing the device.

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