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Lateral depletion-mode 4H-SiC n-channel junction field-effect transistors operational at 400 °C*

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This paper presents the development of lateral depletion-mode n-channel 4H-SiC junction field-effect transistors (LJFETs) using double-mesa process toward high-temperature integrated circuit (IC) applications. At room temperature, the fabricated LJFETs show a drain-to-source saturation current of 23.03 μA/μm, which corresponds to a current density of 7678 A/cm^2. The gate-to-source parasitic resistance of 17.56 kΩ · μm is reduced to contribute only 13.49% of the on-resistance of 130.15 kΩ · μm, which helps to improve the transconductance up to 8.61 μS/μm. High temperature characteristics of LJFETs were performed from room temperature to 400 °C. At temperatures up to 400 °C in air, it is observed that the fabricated LJFETs still show normally-on operating characteristics. The drain-to-source saturation current, transconductance and intrinsic gain at 400 °C are 7.47 μA/μm, 2.35 μS/μm and 41.35, respectively. These results show significant improvement over state-of-the-art and make them attractive for high-temperature IC applications.

Keywords: junction field-effect transistors, high temperature, 4H-SiC, depletion-mode

PACS: 85.30.Tv, 85.40.Ls **DOI:** 10.1088/1674-1056/abc0df

1. Introduction

Aerospace, automotive, energy production, and other industrial systems are calling for electronics that can operate reliably in harsh environments, including high temperatures (above 300 °C).[1] Due to the large bandgap, silicon carbide (SiC) materials not only shine in the field of high-power devices,[2–4] but also attract much attention for devices which can operate under harsh environment.[5] Over the past decade, significant progress has already been made in the high-temperature devices and integrated circuits (ICs). High-temperature ICs based on metal-oxide-semiconductor field-effect transistors (MOSFETs),[6,7] bipolar junction transistors (BJTs),[8,9] and junction field-effect transistors (JFETs)[10,11] have already been reported. High stability of threshold (V_{TH}) within a wide temperature range and being free from oxide reliability problem give JFET based ICs very high robustness for harsh environment applications. Packaged 4H-SiC JFET-based logic ICs with two level interconnects are reported.[12] So far, 4H-SiC lateral trench JFETs (LTJFETs) operating at 450 °C have also been developed for harsh environment applications.[13] More recently, for reducing power loss, 400 °C normally-on and normally-off operation of n-channel and p-channel junction field-effect transistors (JFETs) or complementary JFET (CJFET) fabricated by ion implantation into a common high-purity semi-insulating silicon carbide (SiC) substrate has been demonstrated.[14,15]

Expect for LTJFETs and CJFETs, the most common reported JFET ICs are based on 4H-SiC p-type wafer, and the backside metallization to the p-type substrate facilitates more direct control of the electrical potential of the p-type epilayer immediately beneath the JFET n-channel.[10–12] However, the backside contact needs extra diffusion barrier metallization (such as $TaSi_2$/Pt metallization) to prevent the migration of bond pad Au and atmospheric oxygen toward the ohmic contact/SiC interface, otherwise devices will lose their backside contact in high temperature environment.[16,17] What's more, the inter-metallic mixing between the introduced diffusion barrier system and the underlying ohmic contact metallization is another dominant failure mechanism at high temperature. It will reduce the challenges of high temperature packaging and long-term stability of ICs by bringing the back-side body contact to front side, as shown in Fig. 1. In this work, 4H-SiC n-channel LJFETs based on n-type wafer are demonstrated to operate with well-behaved characteristics at temperatures ranging from room temperature to 400 °C.

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2. Device fabrication

Figure 1 shows the schematic cross section of a fabricated 4H-SiC lateral JFET structure. The devices were fabricated using customer-ordered heavily doped n-type 4H-SiC wafers with three different epi-layers. The thickness and doping concentration of individual epilayers are given in Fig. 1. The fabrication process starts from the dry etching of the p^+ gate finger mesa structure with depth of 0.3 μm by inductively coupled plasma (ICP) etching. Then, to reduce the gate-to-source and gate-to-drain series resistance ($R_{S/D}$), nitrogen (N) ions are implanted with a box profile. To achieve better source/drain ohmic contact, high temperature nitrogen implant is also used to form the n^+ contact area to the source and drain, with doses of 7.3×10^{14}, 5.7×10^{14} and 4.0×10^{14} cm^{-2}, respectively. Then the second ICP etching with depth of 0.8 μm was performed to form the active region and to isolate the devices. In order to form p^+ ohmic contact region in the bulk layer, a series of high temperature aluminum (Al^+) implants were also performed with doses of 8.6×10^{14}, 5.6×10^{14} and 3.3×10^{14} cm^{-2}, respectively. The implantation annealing was performed at 1700 °C for 30 min with carbon film protection. After sacrificial oxidation, the surface passivation was accomplished by a three-hour oxidation process at 1100 °C, followed by a 1-μm PECVD SiO_2 layer. After the surface passivation layer opening, a 200 nm nickel (Ni) thin layer was sputtered in the contact regions and annealed to form the metal ohmic contacts. An 800-nm-thick layer of Al was deposited and patterned to form the metal interconnects. Finally, 4-μm-thick Al metal was patterned for the pad. Figures 2(a) and 2(b) show the layout (not including the pad layer) and the optical image of a fabricated 4H-SiC lateral JFET with gate length $L = 6$ μm and gate width $W = 120$ μm. All the metal contacts are protected by the surface passivation layer for better device operating lifetime.

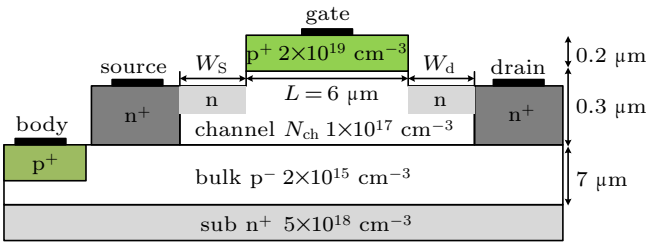


Fig. 1. Schematic cross section of the fabricated 4H-SiC lateral JFET device.

The electrical properties of the devices were measured on-chip using a probe station (Cascade MPS150) and a digital ceramic hot plate to heat the samples from room temperature to 400 °C in air. A semiconductor parameter analyzer (Agilent B1500A) was used to measure the current–voltage (I–V) characteristics of the devices. At each temperature point, the LJFET device and adjacent TLM structures are tested together.

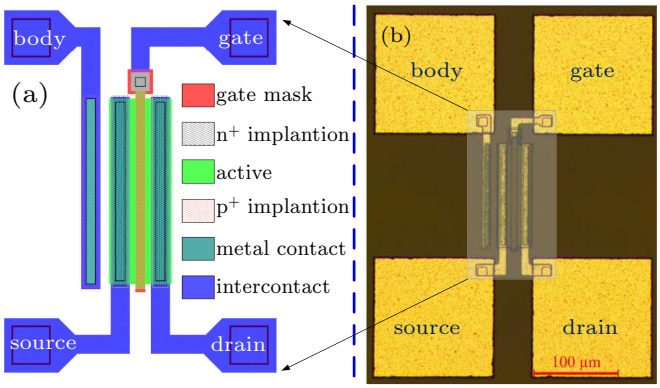


Fig. 2. (a) Layout and (b) optical micrograph of a fabricated device of a typical JFET with $L = 6$ μm and $W = 120$ μm.

3. Results and discussion

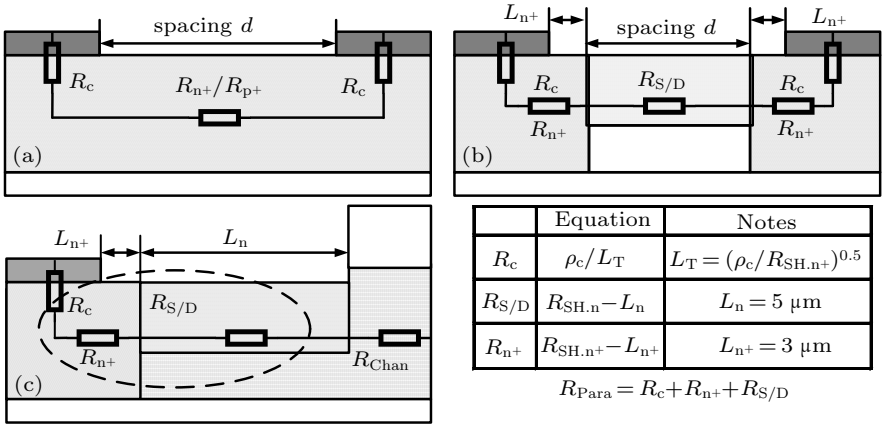
3.1. Ohmic contact characteristics at high temperature

Ohmic contact is a key step in achieving high-performance SiC LJFETs. In this work, on-wafer transmission line measurement (TLM) structures (consisting of six identical metal pads with area of 150×150 μm^2 and spacing d of 20, 40, 60, 80, 100 μm) were used to extract specific contact resistance ρ_c and sheet resistance R_{SH}.

The TLM structure in Fig. 3(a) was used to measure the ρ_c of the Ni n^+/p^+ contact (given n^+ contact resistance R_c) and the sheet resistance $R_{SH.n^+}$ of the n^+ layer (given n^+ region resistance R_{n^+}). The TLM structure in Fig. 3(b) was used to measure the sheet resistance $R_{SH.n}$ of the light nitrogen (N) implanted layer (given gate-to-drain/gate-to-source series resistance $R_{S/D}$). Figure 3(c) shows each extrinsic resistance component's contribution to the parasitic resistance R_{Para} of the device.

Figure 4(a) shows the 25 °C on-wafer TLM I–V characteristics of both source/drain n-type and gate p-type ohmic contacts, along with the corresponding TLM fitting curves. For the source/drain n-type contacts, the ρ_c and the $R_{SH.n^+}$ are 6.29×10^{-5} Ω·cm^2 and 0.53 kΩ/□, respectively. For the gate p-type ohmic contact, the eliminate of the metallic contact's Schottky barrier is beneficial for reducing the gate series resistance. The ρ_c and the R_{SH} for the gate p-type ohmic contact are 3.19×10^{-4} Ω·cm^2 and 16.40 kΩ/□, respectively.

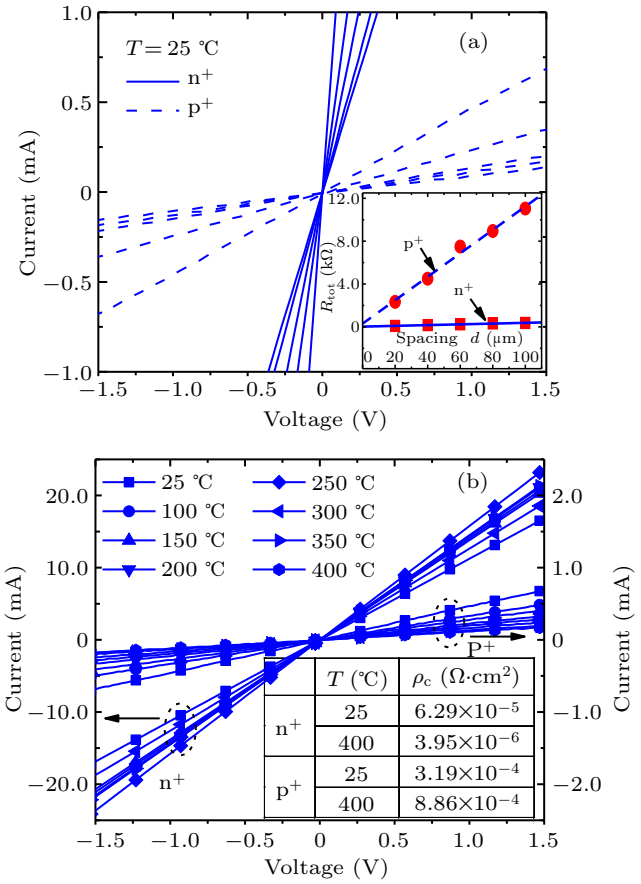
Figure 4(b) shows the on-wafer TLM I–V curves at different temperatures with contact spacing $d = 20$ μm. It is shown that both n-type and p-type contacts remain excellent ohmic behavior at temperature up to 400 °C. At 400 °C, due to increasing average electron kinetic energy, the n-type contacts ρ_c reduce to 3.95×10^{-6} Ω·cm^2. For the p-type ohmic contacts, the ρ_c slightly increases to 8.86×10^{-4} Ω·cm^2. Since the gate current is very small, it is enough to meet the demand. This result indicates that the employed metallic contact scheme can simultaneously form ohmic contact to both source/drain n-type and gate p-type regions with excellent high-temperature Ohmic characteristics up to 400 °C.



	Equation	Notes
R_c	ρ_c/L_T	$L_T=(\rho_c/R_{SH.n+})^{0.5}$
$R_{S/D}$	$R_{SH.n}-L_n$	$L_n=5$ μm
R_{n+}	$R_{SH.n+}-L_{n+}$	$L_{n+}=3$ μm

$R_{Para}=R_c+R_{n+}+R_{S/D}$

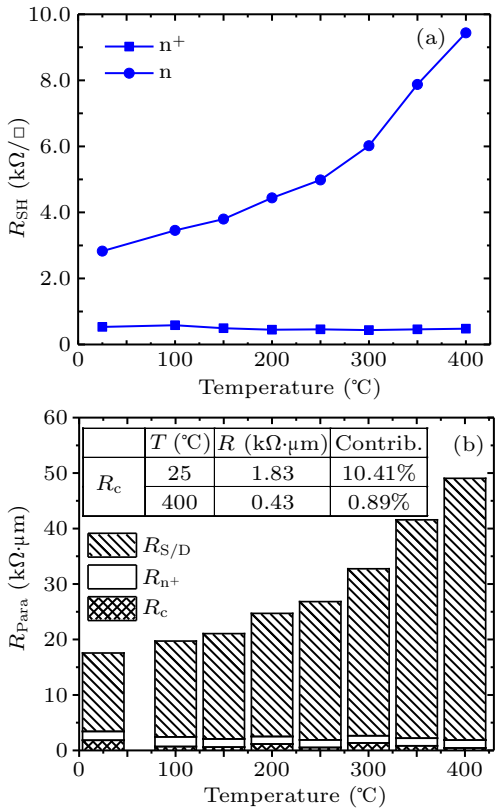
Fig. 3. Schematic of TLMs to measure (a) ρ_c between Ni metal and n^+/p^+ 4H-SiC along with the corresponding R_c, and $R_{SH.n^+}$ along with the corresponding R_{n^+}. (b) Light doped N layer $R_{SH.n}$ along with the corresponding $R_{S/D}$. (c) Schematic of extrinsic resistance components. The contributions to and equation for R_{Para} are also given.



	T (℃)	ρ_c ($\Omega\cdot cm^2$)
n+	25	6.29×10^{-5}
	400	3.95×10^{-6}
p+	25	3.19×10^{-4}
	400	8.86×10^{-4}

Fig. 4. On-chip TLM I–V measurements of the source/drain n-type and gate p-type ohmic contacts characteristics: (a) 25 °C I–V curves and TLM fitting curves (inset), (b) I–V curves at different temperatures with spacing $d=20$ μm.

As described above in the device fabrication section, to minimize the gate-to-source and gate-to-drain series resistance influence, a light doped n-type layer between the gate and source/drain has been created using N^+ implantation. As shown in Fig. 5(a), at room temperature this light n-type layer sheet resistance $R_{SH.n}$ is extracted from on-wafer TLM to be 2.83 kΩ/□, and much greater than n^+ source/drain layer sheet resistance $R_{SH.n^+}$ of 0.53 kΩ/□. Compared with the reported light n-type layer sheet resistance data,[18] $R_{SH.n}$ in our work is effectively reduced by optimization of the dose of light nitrogen implants. As temperature increases to 400 °C, the higher the doping concentration, the lower the dopant activation, and the ionized dopant concentration increase is compensated for by the mobility lowering,[19] therefore $R_{SH.n}$ gradually increases to 9.44 kΩ/□ while $R_{SH.n^+}$ swings to 0.48 kΩ/□.



	T (℃)	R (kΩ·μm)	Contrib.
R_c	25	1.83	10.41%
	400	0.43	0.89%

Fig. 5. Variation of (a) R_{SH} for n^+ and n layer, (b) R_{Para} and contribution of each component at different temperatures.

According to Fig. 5(b), R_{Para} of 17.56 kΩ · μm is obtained at 25 °C, which is mainly contributed by $R_{S/D}$ of 14.14 kΩ · μm, and the contribution of R_c to the total R_{Para} is only 10.41%. As temperature increases to 400 °C, R_{Para} increases to 47.18 kΩ · μm and the contribution of R_c decreases

to 0.89%, which is dominated by the increase of $R_{S/D}$. This result indicates that the light nitrogen implantation process is a very critical step for fabrication SiC JFETs in high temperature applications.

3.2. Electrical characterization at high temperature

Figures 6(a) and 6(b) show the typical drain-to-source current versus drain-to-source voltage (I_{DS}–V_{DS}) curves (output characteristics) of the fabricated 4H-SiC LJFET at room temperature and 400 °C. The drain I_{DS}–V_{DS} characteristics were measured at a body-to-source (V_{BS}) bias of 0 V and a gate-to-source (V_{GS}) bias of −8 to 0 V with −1 V steps. It can be seen that the fabricated 4H-SiC LJFET shows good transistor performance. At 25 °C, this fabricated LJFET conducts 23.03 μA/μm drain-to-source saturation current I_{Dsat} at V_{DS} of 20 V, and V_{GS} of 0 V, corresponding to a very large drain current density J_{DS} of 7678 A/cm^2 by considering that the channel layer is 300 nm and the channel width is 120 μm (for a cross-sectional area of 3.6×10^{-7} cm^2). At 400 °C, the developed device remains good transistor performance. As temperature increases to 400 °C, I_{Dsat} decreases to 7.47 μA/μm, which is mainly caused by the decrease of electron mobility with increasing temperature.

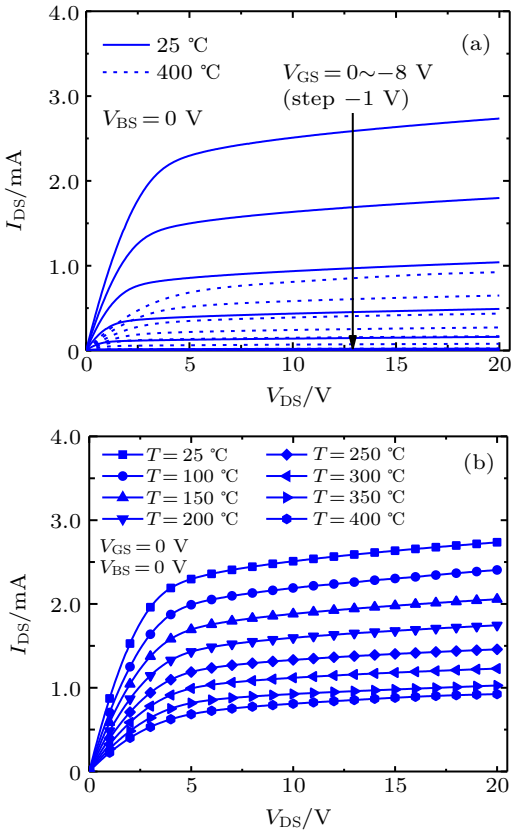


Fig. 6. Typical measured drain I_{DS}–V_{DS} curves (output characteristics) for $V_{BS}=0$ V (a) at 25 °C and 400 °C, and (b) for $V_{GS}=0$ V at different temperatures of the fabricated 4H-SiC LJFET with $L=6$ μm and $W=120$ μm at 25 °C.

On-resistance R_{on} of the fabricated device is extracted at V_{DS} of 0.5 V, V_{GS} and V_{BS} of 0 V. As shown in Fig. 7, at room temperature, R_{on} is extracted to be 130.15 kΩ · μm, and mainly contributed by channel resistance R_{Chan} of 95.03 kΩ · μm or 73.02%. R_{Para} of 17.56 kΩ · μm is contributed by R_{on} of only 13.49%. Considering $R_{S/D}$ of the devices without light nitrogen implants can be estimated to be at least 79 kΩ · μm (it is assumed that the thickness and doping concentration in the gate-to-drain/gate-to-source region is the same as that in the channel region). $R_{S/D}$ is significantly reduced by the adopted light nitrogen implants, thus R_{Para} is reduced greatly. As temperature increases to 400 °C, caused by electron mobility lowering, R_{on} and R_{Chan} increase up to 499.24 kΩ · μm and 401.14 kΩ · μm, respectively. The contribution of R_{Para} is around 10% within the measured temperature range (13.19%–9.28% at 25–250 °C, respectively). This result indicates that R_{Para} is effectively reduced by the applied ohmic contacts and light nitrogen implants.

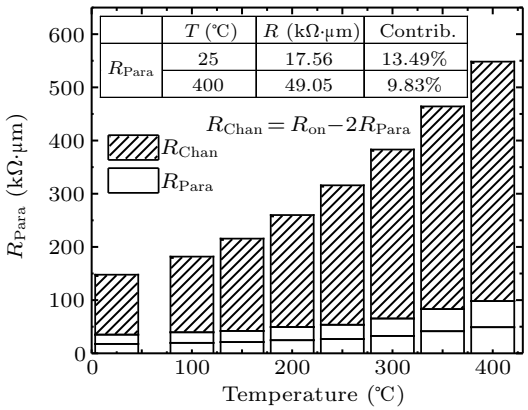


Fig. 7. Variation of R_{on} at different temperatures. The contributions to R_{on} and the equation are also given.

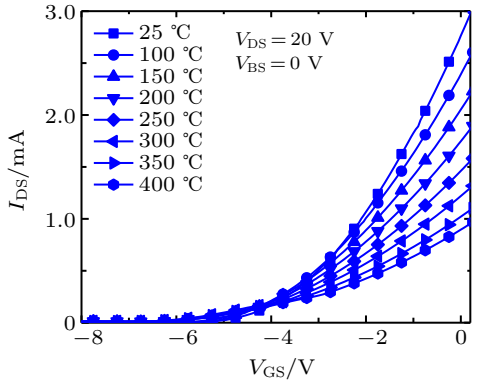


Fig. 8. Measured typical drain I_{DS}–V_{GS} curves (transfer characteristics) of the fabricated 4H-SiC LJFET with $L=6$ μm and $W=120$ μm at different temperatures for $V_{SUB}=0$ V and $V_{DS}=20$ V.

Figure 8 shows the typical transfer characteristics of the fabricated 4H-SiC LJFET at different temperatures for $V_{DS}=20$ V and $V_{BS}=0$ V. The V_{TH} is extracted to be −5.31 V, at 25 °C. At 400 °C, the V_{TH} decreases to −7.06 V, which is affected by the decrease of built-in voltage and the increase of effective channel thickness.[20] The off-state current I_{off} for $V_{GS}=-8$ V and $V_{DS}=20$ V is 2.44×10^{-3} mA at room

temperature, and increases up to 6.23×10^{-3} mA as temperature increases to 400 °C, due to the increasing intrinsic carrier concentration.[21] $I_{\rm off}$ is significantly larger than the value theoretically predicted. The excessive $I_{\rm off}$ is also reported by NASA.[22,23] We surmise that $I_{\rm off}$ is caused by unexpected process failure, and further studies of this problem, which are well beyond the scope of this work, are warranted.

In the typical design of JFET ICs, $V_{\rm BS}$ is not always biased at 0 V. As shown in Figs. 9(a) and 9(b), the JFET I–V curves have a dependence on the applied $V_{\rm BS}$, because the $V_{\rm BS}$ modifies the width of the depletion region at the p–n junction, decreasing the effective conducting channel thickness. At room temperature, as $V_{\rm BS}$ decreases to −20 V, $I_{\rm Dsat}$ decreases to 14.75 μA/μm and $V_{\rm TH}$ increases to −3.75 V. At 400 °C, for $V_{\rm BS}=-20$ V, $I_{\rm Dsat}$ is 4.45 μA/μm and $V_{\rm TH}$ is −4.50 V. This result together with Fig. 8 indicates that this device remains effective, and the normally-on operation under tested temperature and bias range is beneficial for circuit applications.

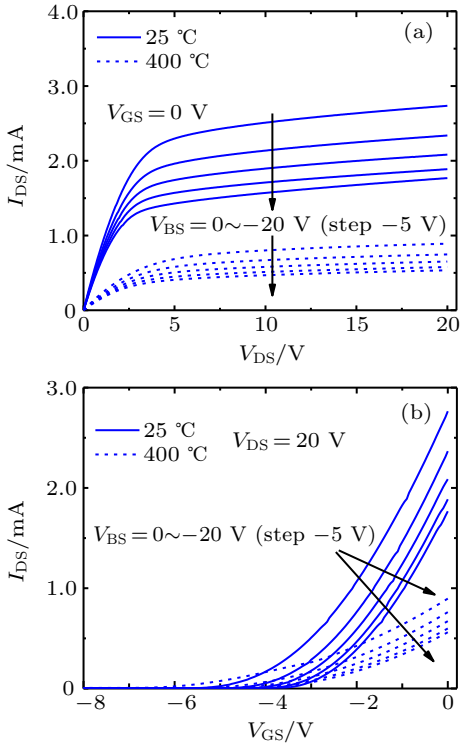


Fig. 9. (a) The typical measured drain $I_{\rm DS}$–$V_{\rm DS}$ curves at 25 °C and 400 °C for $V_{\rm GS}=0$ V (output characteristics), and (b) the $I_{\rm DS}$–$V_{\rm GS}$ curves for $V_{\rm DS}=20$ V, with different $V_{\rm BS}$ of the fabricated 4H-SiC LJFET for $L=6$ μm and $W=120$ μm.

As shown in Fig. 10, the value of transconductance $g_{\rm m}$ is extracted from the measured transfer characteristics by $\partial I_{\rm Dsat}/\partial V_{\rm GS}$ and normalized to the channel width of 120 μm. The intrinsic transconductance $g_{\rm m.int}$ is calculated using the equation shown in Fig. 10. At 25 °C, $g_{\rm m}$ of 8.61 μS/μm for $V_{\rm GS}=0$ V is among the highest value in the reported devices with the similar structure.[11] The corresponding $g_{\rm m.int}=10.14$ μS/μm indicates that the reduction caused by the $R_{\rm Para}$ is 15.12%. As temperature increases to 400 °C, $g_{\rm m}$ and $g_{\rm m.int}$ gradually reduce to 2.35 and 2.66 μS/μm, respectively. The reduction caused by $R_{\rm Para}$ is around 10% at different temperatures (15.12%–11.61% at 25 °C and 300 °C, respectively). This result indicates that the improved $g_{\rm m}$ is mainly due to the reduction of $R_{\rm Para}$.

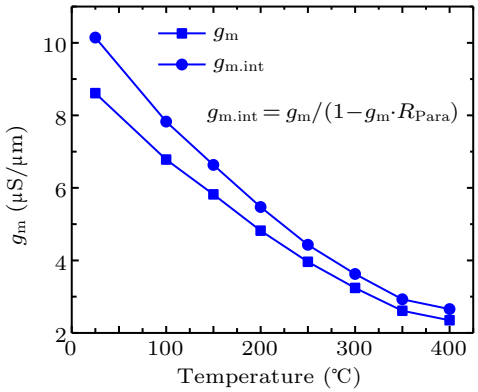


Fig. 10. The temperature dependence of $g_{\rm m}$ and $g_{\rm m.int}$ for the fabricated 4H-SiC LJFET at $V_{\rm GS}=0$ V with $L=6$ μm and $W=120$ μm.

As is shown in Fig. 11, at room temperature, the output resistance r_0 is 5.01×10^4 Ω, corresponding to an intrinsic gain $g_{\rm m}r_0$ of 51.79. Considering today's silicon CMOS technology, $g_{\rm m}r_0$ of short-channel devices is between roughly 5 and 10,[24] it fully meets the demands. As temperature increases to 400 °C, $g_{\rm m}r_0$ slightly decreases to 41.35 because the reduction in $g_{\rm m}$ with increasing temperature is compensated for by the increase of r_0. These results indicate that the developed 4H-SiC LJFET is promising for high temperature electronic applications.

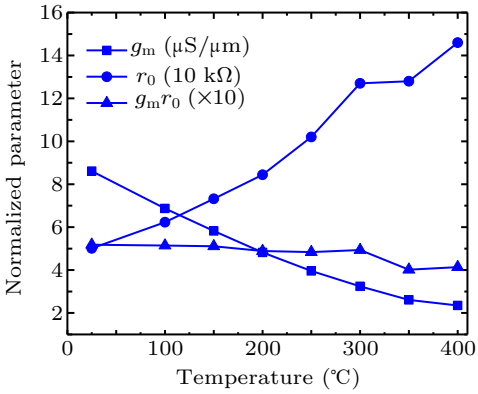


Fig. 11. The temperature dependence of the normalized 4H-SiC LJFET performance parameters for $V_{\rm GS}=0$ V.

4. Conclusion and perspectives

Lateral depletion-mode 4H-SiC n-channel JFETs have been demonstrated to perform well at temperatures up to 400 °C. The gate-to-source parasitic resistance is reduced to 17.56 kΩ · μm by optimized light N^+ implantation process, which is helpful for improving the transconductance up to 8.61 μS/μm at room temperature. At 400 °C, the transconductance and intrinsic gain remain 2.35 μS/μm and 41.35.

This work demonstrates that the developed 4H-SiC JFETs are promising for applications in high-temperature environments.

References

[1] Neudeck P G, Okojie R S and Chen L 2002 *Proc. IEEE* **90** 1065

[2] Song Q W, Zhang Y M, Han J S, Philop T, Sima D, Zhang Y M, Tang X Y and Guo H 2013 *Chin. Phys. B* **22** 027302

[3] Deng Y H, Xie G, Wang T and Sheng K 2013 *Chin. Phys. B* **22** 097201

[4] Chen S and Sheng K 2014 *Chin. Phys. B* **23** 077201

[5] Watson J and Castro G 2015 *J. Mater. Sci.: Mater. Electron.* **26** 9226

[6] Kuhns N, Caley L, Rahman A, Ahmed S, Di J, Mantooth H A, Francis A M and Holmes J 2016 *IEEE Trans. Device Mater. Reliab.* **16** 105

[7] Murphree R, Roy S, Ahmed S, Barlow M, Rahman A, Francis A M, Holmes J, Mantooth H A and Di J 2020 *IEEE Trans. Power Electron.* **35** 913

[8] Zetterling C, Hallen A, Hedayati R, Kargarrazi S, Lanni L, Malm B G, Mardani S, Norstorm H, Rusu A, Suvanam S S, Tian Y and Ostling M 2017 *Semicond. Sci. Technol.* **32** 034002

[9] Tian Y, Lanni L, Rusu A and Zetterling C 2016 *IEEE Trans. Electron Devices* **63** 2242

[10] Patil A C, Fu X, Anupongongarch C, Mehregany M and Garverick S L 2009 *J. Microelectromech. Syst.* **18** 950

[11] Lien W, Damrongplasit N, Paredes J H, Senesky D G, Liu T K and Pisano A P 2014 *IEEE J. Electron Devices Soc.* **2** 164

[12] Spry D J, Neudeck P G, Chen L, Luck D, Chang C W and Beheim G M 2016 *IEEE Electron Device Lett.* **37** 625

[13] Sankin I, Bondarenko V, Sheridan D C, Mazzola M S, Casady J B, Fraley J and Schupbach M 2008 *Mater. Sci. Forum.* **600** 1087

[14] Kaneko M and Kimoto T 2018 *IEEE Electron Device Lett.* **39** 723

[15] Nakajima M, Kaneko M and Kimoto T 2019 *IEEE Electron Device Lett.* **40** 866

[16] Neudeck P G, Garverick S L, Spry D J, Chen L, Beheim G M, Krasowski M J and Mehregany M 2009 *Phys. Status Solidi A* **206** 2329

[17] Spry D J and Lukco D 2012 *J. Electron. Mater.* **41** 915

[18] Spry D J, Neudeck P G, Chen L, Chang C W, Lukco D and Beheim G M 2015 *Electrochem. Soc. Trans.* **69** 113

[19] Lanni L 2014 *Silicon Carbide Bipolar Technology for High Temperature Integrated Circuits* (PhD Dissertation) (KTH Royal Institute of Technology)

[20] Malhan R K, Bakowski M, Takeuchi Y, Sugiyama N and Schoner A 2009 *Phys. Status Solid A* **206** 2308

[21] Sheppard S T, Lauer V, Wondrak W and Niemann E 1998 *Mater. Sci. Forum.* **264** 1077

[22] Neudeck P G, Spry D J, Chen L, Beheim G M, Okojie R S, Chang C W, Meredith R D, Ferrier T L, Evans L J, Krasowski M J and Prokop N F 2008 *IEEE Electron Device Lett.* **29** 456

[23] Spry D J, Neudeck P G, Chen L Y, Evans L J, Lukco D, Chang C W and Beheim G M 2016 *Mater. Sci. Forum.* **858** 1112

[24] Razavi B 2017 *Design of Analog CMOS Integrated Circuits*, 2nd edn (New York: McGraw-Hill) pp. 47–52