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Enhanced mobility of MoS_2 field-effect transistors by combining defect passivation with dielectric-screening effect*

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A facile method of combining the defect engineering with the dielectric-screening effect is proposed to improve the electrical performance of MoS_2 transistors. It is found that the carrier mobility of the transistor after the sulfur treatment on the MoS_2 channel is greatly enhanced due to the reduction of the sulfur vacancies during vulcanization of MoS_2. Furthermore, as compared to those transistors with HfO_2 and SiO_2 as the gate dielectric, the Al_2O_3-gate dielectric MoS_2 FET shows a better electrical performance after the sulfur treatment, with a lowered subthreshold swing of 179.4 mV/dec, an increased on/off ratio of 2.11×10^6, and an enhanced carrier mobility of 64.74 $cm^2/V{\cdot}s$ (about twice increase relative to the non-treated MoS_2 transistor with SiO_2 as the gate dielectric). These are mainly attributed to the fact that a suitable k-value gate dielectric can produce a dominant dielectric-screening effect overwhelming the phonon scattering, increasing the carrier mobility, while a larger k-value gate dielectric will enhance the phonon scattering to counteract the dielectric-screening effect, reducing the carrier mobility.

Keywords: MoS_2 transistor, sulfur vacancy, high-k dielectric, mobility

PACS: 81.65.Rv, 77.22.Ch, 73.20.Hb, 81.15.–z **DOI:** 10.1088/1674-1056/abb30f

1. Introduction

Since the first discovery of graphene in 2004, two-dimensional (2D) materials have been intensively investigated due to their unique structural characteristics and excellent electrical properties.[1–3] Although graphene has been shown to have extremely high carrier mobility, the lack of its bandgap limits its application in logic devices. Unlike graphene, MoS_2 has an appropriate bandgap and is one of the most representative 2D semiconductor materials in transition metal dichalcogenides (TMDs). It has been found that the bulk MoS_2 shows an indirect bandgap of 1.2 eV and the monolayer MoS_2 exhibits a direct bandgap of 1.8 eV,[4–6] which has a wide range of applications in field-effect transistors, memories,[7,8] logic circuits,[9,10] photodetectors,[11] etc.

Theoretical calculations based on the density functional theory demonstrated that the mobility of the monolayer MoS_2 can reach 410 $cm^2/V{\cdot}s$ at room temperature.[12,13] However, experimentally, the mobility of the monolayer MoS_2 as channel material of the field-effect transistor (FET) is still far from its intrinsic limit, which is originated from the effects of some factors, e.g., charged impurities,[14,15] surface defects,[16] phonon scattering,[17] etc. The high-dielectric constant (k) gate dielectrics were widely used to reduce the influence of the charged impurities and can effectively screen their Coulomb scattering, which has been confirmed in many experiments.[6,14,18] Li *et al.*[19] fabricated MoS_2 FET with a back-gate structure on Si substrate with high-k Al_2O_3 as the gate dielectric, and its mobility has been significantly improved as compared with the gate dielectric of SiO_2. On the other hand, the defect engineering is one of the effective ways to further improve the performance of MoS_2 devices. Yu *et al.*[12] found that the sulfur vacancies, which are the main type of intrinsic defects in MoS_2, can be effectively repaired by (3-mercaptopropyl) trimethoxysilane (MPS) under a mild annealing, resulting in a significant reduction of the Coulomb impurity and short-range scatterings. However, these investigations usually focused on one of the influencing factors and rarely combined two or more factors for a comprehensive analysis. Therefore, in this work, we adopt a facile approach to combine the defect engineering with the dielectric-screening engineering to fabricate the back-gated MoS_2 transistors to investigate the effects of the surface passivation of MoS_2 and the high-k gate dielectrics on electrical characteristics of devices, especially on the carrier mobility.

2. Experiments

The device fabrication begins with thermally-growing SiO_2 on the cleaned heavily-doped p^{++}-Si wafers with a resistivity of 0.01 $\Omega{\cdot}cm$, and the thickness of the SiO_2 was measured to be 32 nm by an ellipsometer. The few-layered MoS_2 flakes were obtained by a micromechanical exfoliation of the bulk MoS_2 crystal purchased from SPI,[20] and then transferred to the SiO_2/p^{++}-Si substrates with the help of Scotch tape. The thickness of these MoS_2 flakes can be roughly distinguished by their colors:[21] gray, blue, and purple corre-

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spond to the bulk, multilayer, and few-layered MoS_2, respectively, as shown in Fig. 1(a). Figure 1(b) shows the AFM height image of the few-layered MoS_2 flake with a thicknesses of 5.32 nm ($\sim$ 8 layers). The few-layered MoS_2 flake was chosen to fabricate transistors because it has higher density of states than the monolayer MoS_2, which will result in a rather high drive current.[22,23]

Then, these MoS_2 flakes were vulcanized in a tube furnace. The one gram of sulfur powder was placed downstream in constant-temperature zone and the $MoS_2/SiO_2/p^{++}$-Si substrates were placed upstream $\sim$ 10 cm away from the sulfur powder in the same temperature zone, as shown schematically in Fig. 1(c). During the vulcanization, the furnace temperature was hold at 200 °C (an optimum temperature via experiments) for one hour, and the diffusion rate of the sulfur vapor was controlled by adjusting the flow rate of the carrier gas (N_2).

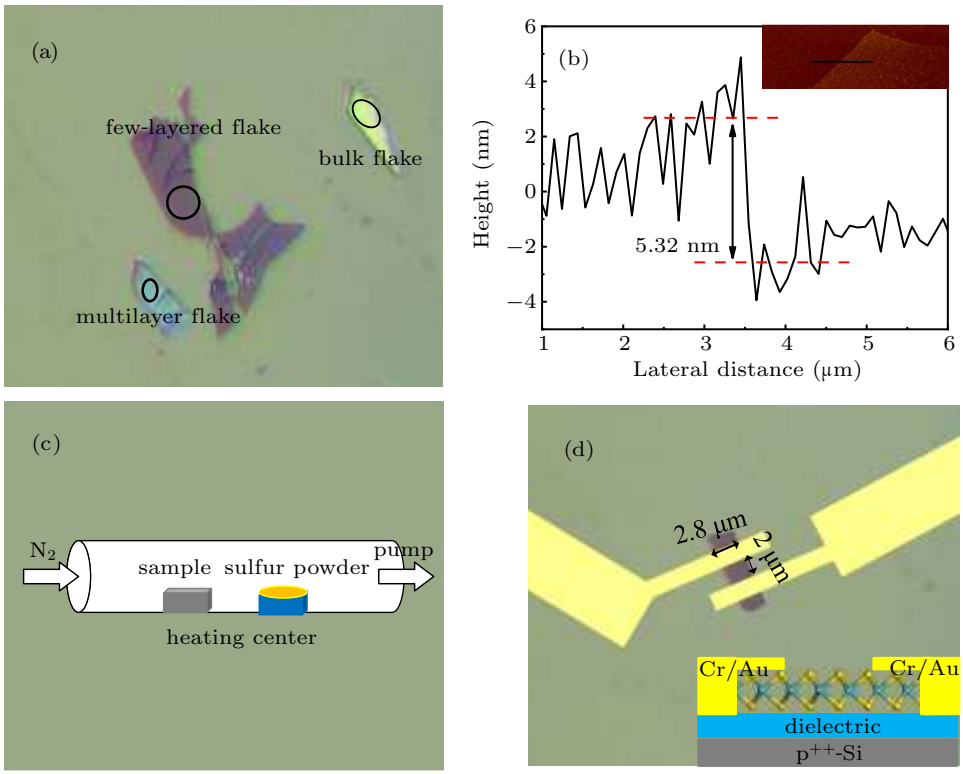


Fig. 1. (a) Optical micrographs of different-thickness MoS_2 flakes on the dielectric; (b) the AFM height image of the few-layered MoS_2 flake; (c) schematic diagram for sulfur treatment on MoS_2 flakes; (d) optical micrographs of MoS_2 transistor with the inset showing its cross-section diagram.

Next, the sulfur-treated MoS_2 flakes were used to fabricate the back-gated FETs. Electron beam lithography was used to pattern the source/drain (S/D) of MoS_2 transistors, and 15-nm Cr/45-nm Au were successively deposited by electron-beam evaporation, followed by a liftoff processing to form S/D electrodes, as shown in Fig. 1(d). The channel length (L) of all transistors was 2 μm and the channel width (W) was 1–4 μm depending on the shapes of the MoS_2 flakes, and the schematic diagram of the transistor structure is shown in the inset of Fig. 1(d). Lastly, the transistors were rapidly annealed at 300 °C for 300 s in a N_2 atmosphere (1500 sccm) with a pressure of 0.2 Torr to reduce the contact resistance between the MoS_2 and the Cr/Au electrodes.[24] For comparison, a transistor with the MoS_2 unexperienced vulcanization was also fabricated as a control sample. Electrical measurements of the transistors were performed using a Keithley 4200-SCS semiconductor parameter analyzer under a light-tight and electrically-shielded condition at room temperature.

3. Results and discussion

To ensure the validity of the measured results, at least four transistors for each sample were measured. Figure 2(a) shows the typical drain current (I_d) versus drain–source voltage (V_{ds}) curves of the transistors with and without the MoS_2 treated by vulcanization. It can be clearly seen that the transistors have good output characteristics with clear cut-off region, transition region, and saturation region. Obviously, the post-vulcanization transistor has higher on-state current than the pre-vulcanization transistor, attributing to the reduction of the sulfur defects during vulcanization of MoS_2. Figure 2(b) is the I_d–V_{ds} curves in the linear region (V_{ds} from -0.1 V to 0.1 V), and a good linear relationship between I_d and V_{ds} can be observed, indicating a good ohmic contact between the MoS_2 and the Cr/Au electrodes. Figures 2(c) and 2(d) are the transfer characteristics of the MoS_2 FETs with $V_{ds} = 0.2$ V in linear scale and in semi-log scale, respectively, and the drain current is normalized to eliminate the effect of different chan-

nel widths on the output current. The threshold voltage (V_{th}) is extracted by the linear extrapolation method through the maximum-slope point of the I_d–V_{ds} curve in Fig. 2(c) to be 1.39 V and 2.43 V before and after vulcanization, respectively. The positive shift of V_{th} after the sulfur treatment is mainly due to the reduction of the sulfur vacancies in the MoS_2 flakes.[25]

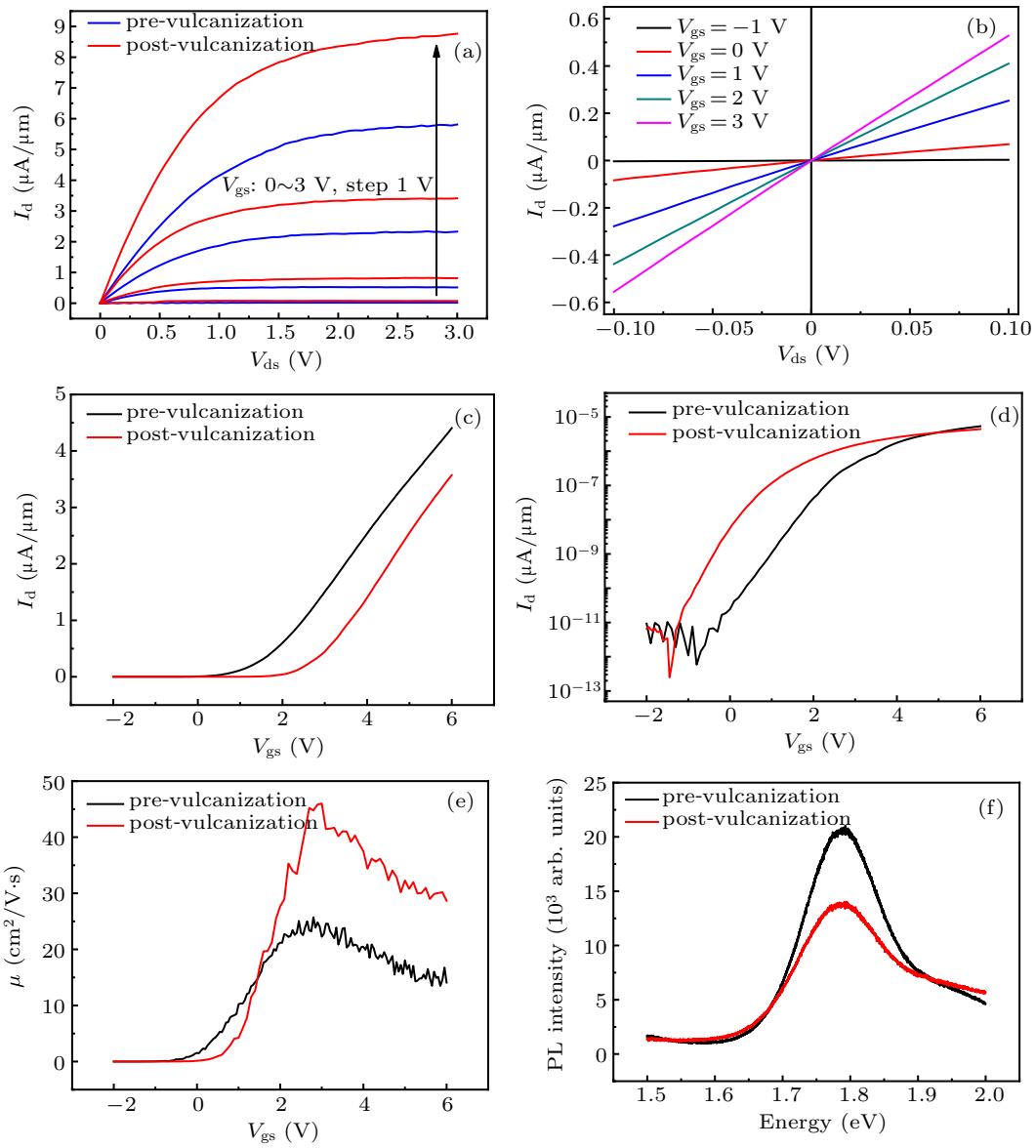


Fig. 2. (a) Output characteristics of MoS_2 FETs with and without sulfur treatment; (b) I_d–V_{ds} curves in the linear region of the back-gated MoS_2 transistor with MoS_2 treated by vulcanization; transfer characteristics with $V_{ds} = 0.2$ V in linear scale (c) and in semi-log scale (d); (e) extracted mobility from the transfer curves in (c); (f) PL spectrum of MoS_2 flakes before and after vulcanization.

From the transfer curves of the two transistors before and after vulcanization, their field-effect mobility can be extracted using by

$$\mu = \frac{1}{C_{ox}V_{ds}} \times \frac{L}{W} \times \frac{\Delta I_{ds}}{\Delta V_{gs}}, \tag{1}$$

where C_{ox} is the oxide capacitance per unit area (1.08×10^{-7} F/cm^2 for 32-nm thick SiO_2), L and W are the channel length and width, respectively, and V_{gs} is the gate–source voltage. As can be seen from Fig. 2(e), the mobility of the transistor with sulfur treatment on MoS_2 is largely enhanced as compared to that of the non-treated MoS_2 transistor (46.03 cm^2/V·s vs. 25.71 cm^2/·V·s). Obviously, this is attributed to the reduction of the sulfur-vacancy defects in MoS_2 by the sulfur treatment, because these defects could act as scattering centers to slow down the carrier transportation in the channel, resulting in low mobility. This can be supported by Raman spectral analysis, because the measured photoluminescence (PL) intensity depends on the surface defect density of MoS_2 and the PL intensity weakens as the surface defects decrease.[26] Clearly, from Fig. 2(f), the PL intensity of the MoS_2 flakes becomes weaker after the sulfur treatment compared to that before the sulfur treatment, indicating the reduction of the defects related to the sulfur vacancies. In addition, the peak of the MoS_2 PL intensity is at 1.78 eV, which is consistent with the forbidden band of the few-layered MoS_2. AFM was employed to analyze the surface morphology of the MoS_2 flakes before and after vulcanization. It was observed

that the surface roughness was decreased by ∼ 0.09 nm after the vulcanization, further indicating the role of the vulcanization. From the above analyses, it can be concluded that the sulfur treatment on MoS_2 can enhance the carrier mobility in the channel due to the reduction of the surface roughness and the defects in the MoS_2 flakes.

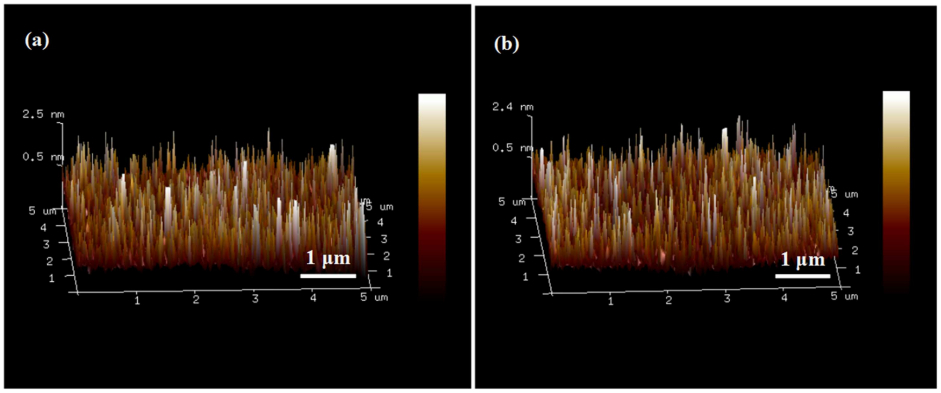


Fig. 3. AFM surface images (5×5 μm^2) of MoS_2 flakes before (a) and after (b) sulfur treatment.

High-k materials, e.g., hafnium dioxide (HfO_2), alumina (Al_2O_3), are widely used in CMOS devices and play an important role as gate dielectrics in MoS_2-based transistors, since they are expected to screen the charged-impurity scattering near the channel, resulting in an enhancement of the carrier mobility.[19,27,28] For this purpose, high-k Al_2O_3 and HfO_2 are employed to replace SiO_2 as the gate dielectric of the MoS_2 transistors respectively to further improve the carrier mobility. The Al_2O_3 and HfO_2 thin films were grown by atomic layer deposition (ALD) at 200 °C with TDMA-Hf ($Hf(N(CH_3)_2)_4$), TMA ($Al(CH_3)_3$), and H_2O as Hf, Al, and O precursors, respectively, and N_2 as the carrier/purge gas. The injection schedule for one cycle of Al_2O_3 and HfO_2 deposition was 0.02 s–15 s–0.015 s–15 s of TMA–N_2–H_2O–N_2 and 0.15 s–15 s–0.015 s–15 s of TDMA–Hf–N_2–H_2O–N_2, respectively. The Al_2O_3 and HfO_2 thin films with a thickness of 32 nm were obtained after 291 and 311 deposition cycles, respectively. The metal/Al_2O_3 or HfO_2/Si MOS capacitors with an area of 7.85×10^{-5} cm^2 were fabricated using gold as the gate electrode to characterize the dielectric properties of the two films.

Figure 4 shows the typical high-frequency (1 MHz) C–V curves for the metal/HfO_2/p^{++}-Si and metal/Al_2O_3/p^{++}-Si MOS capacitors. The accumulation (or oxide) capacitances of the HfO_2 and Al_2O_3 MOS capacitors are 37 pF and 27 pF, respectively. According to the formula $k = (C_{ox}t_{ox})/(A\varepsilon_0)$, where ε_0 is the vacuum permittivity, A is the electrode area, and t_{ox} is the physical thickness of the HfO_2 or Al_2O_3, the equivalent k-value of the gate dielectric is extracted to be 11.51 and 6.91 for the HfO_2 and Al_2O_3 gate dielectrics, respectively. Correspondingly, the calculated capacitance-equivalent thickness (CET $= (\varepsilon_{ox}/k)t_{ox}$, ε_{ox} is the relative dielectric constant of SiO_2) of the HfO_2 dielectric is smaller than that of the Al_2O_3 dielectric (10.84 nm vs. 18.06 nm), which is beneficial for enhancing the dielectric-screening effect and scaling down the MoS_2-based transistor. Even so, the k-value of Al_2O_3 is more suitable for balancing the charged-impurity scattering and the phonon scattering on electrons in the MoS_2 channel, because the high-k dielectrics can reduce the Coulomb scattering through the dielectric-screening effect but simultaneously can also cause a serious phonon scattering.[17] Moreover, as can be seen from Fig. 4, the C–V hysteresis of the Al_2O_3 sample is much smaller than that of the HfO_2 sample, implying the fewer defect states in the former than the latter.

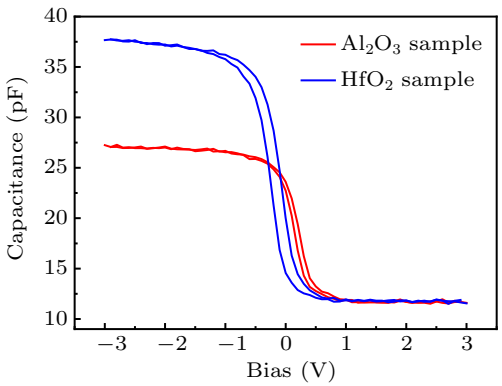


Fig. 4. The C–V curves of metal/Al_2O_3/ p^{++}-Si and metal/HfO_2/ p^{++}-Si MOS capacitors.

Figures 5(a) and 5(b) show the typical transfer characteristics of the MoS_2 transistors with different gate dielectrics before and after the sulfur treatment on MoS_2, respectively, and the corresponding changes of their mobility with V_{gs} are depicted in Figs. 5(c) and 5(d). The extracted on/off current ratio, peak mobility (μ), and subthreshold swing (SS) for these transistors are listed in Table 1. It can be seen that the transistors with different gate dielectrics (SiO_2, Al_2O_3, and HfO_2) have a similar on/off current ratio before the MoS_2 vulcanization. After the sulfur treatment on MoS_2, the on/off current ratios of the transistors are increased, with the maximum obtained in the transistor with Al_2O_3 gate dielectric (2.11×10^6).

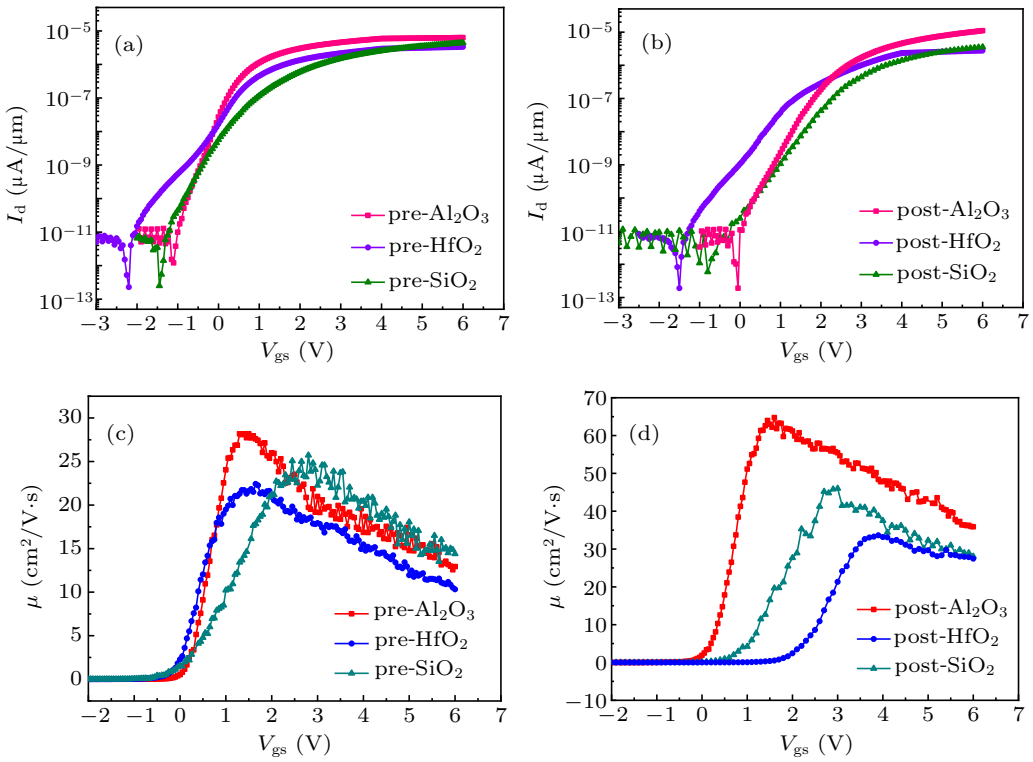


Fig. 5. Typical transfer characteristics of MoS_2 transistors with different gate dielectrics (a) before and (b) after sulfur treatment on MoS_2; the extracted mobility of MoS_2 transistors with different gate dielectrics (c) before and (d) after sulfur treatment on MoS_2.

Table 1. Electrical properties of the MoS_2 FETs with SiO_2, HfO_2, and Al_2O_3 as the gate dielectric respectively before and after the sulfur treatment.

Sample	μ (cm^2/V·s)	SS (mV/dec)	I_{on}/I_{off} (10^6)
Pre-SiO_2	25.71	253.4	1.02
Post-SiO_2	46.03	229.7	1.58
Pre-HfO_2	22.42	245.2	0.81
Post-HfO_2	33.63	201.3	1.17
Pre-Al_2O_3	28.18	212.1	1.33
Post-Al_2O_3	64.74	179.4	2.11

The extracted SS's for the transistors with SiO_2, HfO_2, and Al_2O_3 gate dielectrics are 253.4 mV/dec, 245.2 mV/dec, and 212.1 mV/dec before the sulfur treatment on MoS_2 and become 229.7 mV/dec, 201.3 mV/dec, and 179.4 mV/dec, respectively, after the sulfur treatment on MoS_2, i.e., the SS is significantly lowered after the MoS_2 vulcanization as compared with that before the vulcanization, with the minimum obtained in the transistor with Al_2O_3 gate dielectric. The small SS implies a good interface quality between MoS_2 and Al_2O_3 because the SS is related to the interface-state density (D_{it})

$$SS = (\ln 10)\left(\frac{k_B T}{q}\right)\left(1+\frac{C_s + C_{it}}{C_{ox}}\right), \tag{2}$$

$$D_{it} = \frac{C_{it}}{q^2}, \tag{3}$$

where C_s is the barrier capacitance per unit area at the MoS_2 surface and can be ignored because the SS is generally extracted in the deep subthreshold region; C_{it} is the interface-state capacitance per unit area; k_B is the Boltzmann constant, and q is the electronic charge. According to Eqs. (2) and (3), the calculated interface-state density between MoS_2 and Al_2O_3 is 3.50×10^{12} eV^{-1}·cm^{-2} before the sulfur treatment and 2.75×10^{12} eV^{-1}·cm^{-2} after the treatment.

The mobility of the MoS_2 transistor is a main concern. The extracted peak mobility for the transistors with SiO_2, HfO_2, and Al_2O_3 as the gate dielectric and the sulfur treatment on MoS_2 is 46.03 cm^2/V·s, 33.63 cm^2/V·s, and 64.74 cm^{2}V·s, respectively, which is significantly improved as compared to their counterparts without the sulfur treatment on MoS_2 (1.5–2.3 times). The high-k oxides are usually used as the gate dielectrics to suppress the Coulomb scattering owing to their dielectric-screening effect. Therefore, the significant improvement for the transistor with Al_2O_3 as the gate dielectric can be attributed to the dielectric-screening effect. However, an opposite trend is observed for the MoS_2 transistor with HfO_2 as the gate dielectric, which has an even lower mobility than its counterpart with SiO_2 as the gate dielectric. Ma *et al.*[17] reported this similar phenomenon and argued that although the high-k dielectrics can reduce the Coulomb scattering by their dielectric-screening effect at room temperature, an enhanced surface-phonon scattering produced by them counteracts this advantage. When the phonon scattering is negligible, the carrier mobility is almost limited by the Coulomb scattering and is enhanced as the k-value of the gate dielectric increases. However, when the k-value is too large, the electrons in the channel are more likely to excite the phonons in the surrounding dielectric through the remote Coulomb interactions, so that the channel carriers are more strongly affected by the phonon scattering, resulting in the reduction of the mobility. Based on

the explanation, the MoS_2 transistors with Al_2O_3 and HfO_2 as the gate dielectric exhibit the enhanced and reduced mobility, respectively, as compared with their counterpart with SiO_2 as the gate dielectric, because the former has a suitable k-value so that the dielectric-screening effect is dominant, and the latter has a larger k-value so that the phonon scattering overwhelms the dielectric-screening effect. The same phenomenon was also demonstrated in Konar's research on the effect of the high-k gate dielectric on the charge transport in the graphene FETs.[29]

4. Conclusion

In summary, the sulfur-treated few-layered MoS_2 back-gated FETs with different gate dielectrics have been fabricated and their electrical properties are compared. It is found that the transistors with the sulfur treatment on MoS_2 channel exhibit a greatly enhanced carrier mobility as compared to their counterparts without the sulfur treatment. This is mainly owing to the reduction of the defects related to the sulfur vacancies during the vulcanization of the MoS_2. Further, it is found that when the high-k Al_2O_3 and HfO_2 are used to replace SiO_2 as the gate dielectric, the mobility of the relevant transistors gets enhanced and reduced, respectively. The involved mechanisms lie in that a suitable k-value of the former leads to an effective dielectric-screening effect and a larger k-value of the latter induces an enhanced phonon scattering over the dielectric-screening effect. For the Al_2O_3-gate dielectric MoS_2 FET, its carrier mobility is tripled after the sulfur treatment on MoS_2 (64.74 $cm^2/V{\cdot}s$) as compared to that before the sulfur treatment, and also its on/off current ratio and subthreshold swing are improved. Therefore, the sulfur treatment on MoS_2 provides a facile solution to improve the mobility of the MoS_2 FETs, especially for the transistor with a reasonable k-value gate dielectric, e.g., Al_2O_3.

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