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Influences of increasing gate stem height on DC and RF performances of InAlAs/InGaAs InP-based HEMTs*

Zhi-Hang Tong(童志航)[1,2], Peng Ding(丁芃)[1,2], Yong-Bo Su(苏永波)[1,2], Da-Hai Wang(王大海)[1], and Zhi Jin(金智)[1,2,†]

[1] *High-Frequency High-Voltage Device and Integrated Circuits Center, Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*
[2] *University of Chinese Academic of Sciences, Beijing* 100049, *China*

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The T-gate stem height of InAlAs/InGaAs InP-based high electron mobility transistor (HEMT) is increased from 165 nm to 250 nm. The influences of increasing the gate stem height on the direct current (DC) and radio frequency (RF) performances of device are investigated. A 120-nm-long gate, 250-nm-high gate stem device exhibits a higher threshold voltage (V_{th}) of 60 mV than a 120-nm-long gate devices with a short gate stem, caused by more Pt distributions on the gate foot edges of the high Ti/Pt/Au gate. The Pt distribution in Schottky contact metal is found to increase with the gate stem height or the gate length increasing, and thus enhancing the Schottky barrier height and expanding the gate length，which can be due to the increased internal tensile stress of Pt. The more Pt distributions for the high gate stem device also lead to more obvious Pt sinking, which reduces the distance between the gate and the InGaAs channel so that the transconductance (g_m) of the high gate stem device is 70 mS/mm larger than that of the short stem device. As for the RF performances, the gate extrinsic parasitic capacitance decreases and the intrinsic transconductance increases after the gate stem height has been increased, so the RF performances of device are obviously improved. The high gate stem device yields a maximum f_t of 270 GHz and f_{max} of 460 GHz, while the short gate stem device has a maximum f_t of 240 GHz and the f_{max} of 370 GHz.

Keywords: InP-based HEMT, gate stem height, Pt/Ti Schottky contact, gate parasitic capacitances

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1. Introduction

In last several years, demand for high frequency transistor is increasing for high speed applications such as in high frequency wireless systems, broadband satellite communication and high speed optical-fiber communication system. The InAlAs/InGaAs InP-based high electron mobility transistors (InP-based HEMTs) can be one of the best candidate devices to achieve the ultrahigh-speed operation because of their high electron mobility, high electron velocities, and high sheet electron densities, which have been successfully used in high frequency, low noise, high gain IC designs, and widely applied to high frequency systems.[1–4] A variety of effective methods have been reported to greatly improve the device performances, for example electron beam lithography scaling down gate length, improving Ohmic contact process, and accurately controlling gate recess.[5,6] Up to date, high current gain cutoff frequency (f_t) over 600 GHz and power gain cutoff frequency (f_{max}) in excess of 1 THz have been achieved by scaling gate length down to sub 50 nm.[7–9]

With the gate length shrinking, the influences of device parasitic parameters on limiting the direct current (DC) and radio frequency (RF) performances of InP-based HEMTs become more and more non-negligible, so minimizing the parasitic parameters of the devices has become an important subject for further improving the performances of InP-based HEMTs, including the reductions of source/drain parasitic resistances and gate parasitic resistances and capacitances. Optimization of structure and size of gate and gate recess, has always been beneficial and worth studying for minimizing the parasitic parameters of InP-based HEMT. Yun *et al.* investigated the influence of the source-to-drain spacing (L_{ds}) on DC and high frequency characteristics of $L_g = 87$ nm InP-based HEMT, improving the DC and RF responses of these devices as the L_{SD} was scaled down to 0.8 μm and yielding $f_t = 519$ GHz, and $f_{max} = 645$ GHz.[10] Moran *et al.* adopted a self-aligned T-gate process to reduce the proximity of the Ohmic contact to the 50-nm gate, making the self-aligned gate device exhibit an extremely high g_m of 1900 mS/mm and f_t of 490 GHz.[11] Endoh *et al.* reported that the g_m and f_t of 30-nm-gate InP-based HEMT increase with gate–drain spacing (L_{gd}) decreasing down to 50 nm, exhibiting an extremely high ft of 547 GHz.[12] The aforementioned studies have revealed that the DC and RF characteristics of InP-based HEMTs can be much improved by shrinking the size of gate recess, which reduces the source/drain parasitic resistances but at cost of increasing the gate parasitic capacitances. Therefore, minimizing the gate parasitic capacitances can be meaningful for further improving the performances of InP based

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†Corresponding author. E-mail: jinzhi@ime.ac.cn
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HEMTs. Takahashi *et al.* adopted a cavity structure around gate for eliminating parasitic capacitance and obtained superior RF and noise characteristics of InP-based HEMTs, but the fabrication complexity of the devices was increased.[13] In comparison, increasing T-shape gate stem height can be a more straightforward method to reduce the gate parasitic capacitances. Yoshida *et al.* fabricated T-gates with different gate stem heights by changing the deposition condition of the SiCN molds, and revealed that the higher T-gate stem is beneficial to the decreasing of the parasitic gate delay time of InP based HEMT.[14] Besides, the large gate metal height is also helpful in enhancing the breakdown voltage of device.[15] However, the increase of gate stem height of T gate through the conventional widely used tri-layer resist process, and the influence of increasing the gate stem height on the DC and RF performance of InP-based HEMT, still need further studying.

In this work, we increase the gate stem height of T gate by increasing the bottom layer resist thickness of tri-layer resist. The DC and RF characteristics of InP-based HEMTs are demonstrated for the devices with different gate stem heights. Differences in DC performance among the different gate stem height devices are found to be caused by the differences in Pt distribution of Schottky contact metal among T gates with different gate stem heights. As for the RF performances, a small signal model is adopted to extract the intrinsic parameters of devices, and an analytical model of f_t is used to analyze the device delay, therefore the influence of increasing T-shape gate stem height on the RF performances of devices can be fully explained.

2. Device fabrication

The epitaxial layer of InP-based HEMT is shown in Fig. 1, which was grown by molecular beam epitaxy (MBE) on 3-inch-thick (1 inch = 2.54 cm) InP substrate. From bottom to top, the layers are a 500-nm-thick $\ln_{0.52}Al_{0.48}As$ buffer layer, 15-nm-thick $\ln_{0.53}Ga_{0.47}As$ channel layer, 3-nm-thick unstrained $\ln_{0.52}Al_{0.48}As$ spacer layer, Si delta doping layer with 5×10^{12} cm^{-2} doping concentration, 8-nm-thick unstrained $\ln_{0.52}Al_{0.48}As$ Schottky barrier layer, 4-nm-thick InP etch-stop layer for preventing excessive etching and the 20-nm-thick Si-doped $\ln_{0.53}Ga_{0.47}As$ composite capping layer. The Hall measurements were made at room temperature, showing a carrier mobility of 8000 cm^2/(V·s) and a two-dimensional sheet density of 3.26×10^{12} cm^2. The fabrication process of InP HEMTs mainly contained four steps including mesa isolation, Ohmic contact formation, T-shape gate, and gate recess process. Firstly, isolating mesa was made by the phosphorus acid-based wet chemical etching. Next, the source and drain were spaced by 2.3 μm through a lithography process. And then Ti/Pt/Au was evaporated to satisfy the requirement for Ohmic contact by electron beam evaporation without being annealed, and its contact resistance was measured to be 0.032 Ω·mm. The key process was the fabricating of gate recess and different heights of T-shape gate. A 15-nm-thin SiO_2 film was evaporated on the cap layer by plasma enhanced chemical vapor deposition (PECVD). The advantages of introducing SiO_2 film were the improving of resist adherence, the determining of gate footprint and the enhancing of mechanical support for T-shape gate.[16] A tri-layer electronic beam (EB) resist consisting of ZEP520A/PMGI/ZEP520A was coated on the SiO_2 film. For the increasing of the T-shape gate stem height, the thickness of the bottom resist layer of ZEP520A was increased by slowing down the resist coating speed from 6000 rpm/s to 4000 rpm/s, while the upper two coated resist layers keep the same thickness. Then, EB exposure was carried out to determine the gate footprint pattern length for the different thickness values of tri-layer resists. The single step electron beam lithography (EBL) process for the T-shape gate fabrication was performed by JEOL JBX-5000LS EBL system.[17] The EB exposure line width which defines the gate foot was varied between 20 nm and 50 nm and the exposure dose for the gate foot was varied between 700 μC/cm^2 and 800 μC/cm^2.

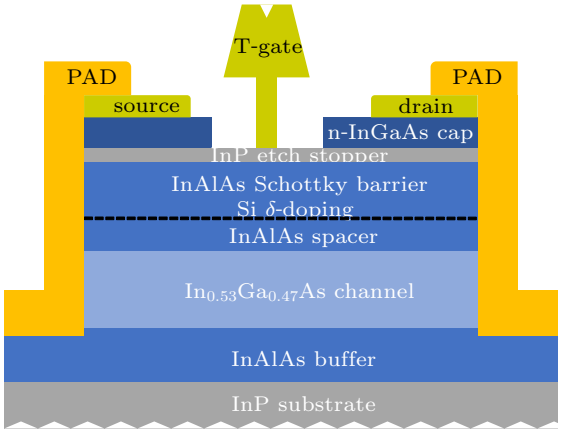


Fig. 1. Schematic cross-section of InP-based HEMTs.

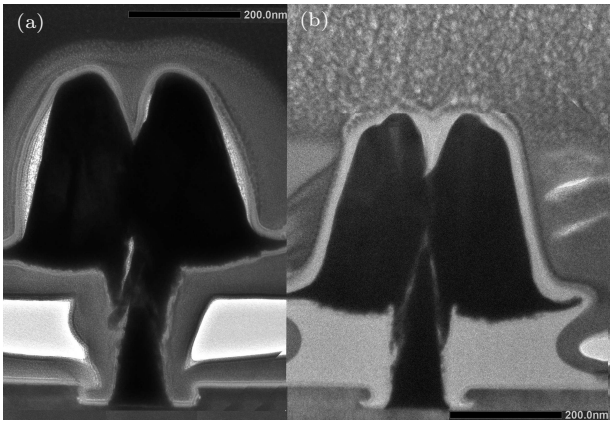


Fig. 2. TEM images of cross section of InP-based HEMTs with different gate stem heights: (a) device A with gate length 120 nm and gate stem height 250 nm, and (b) device B with gate length 120 nm and gate stem height 165 nm.

The 4 groups of EB exposure conditions were used in our experiments as listed in Table 1. After the EBL process, the bottom of the T-shape gate pattern was replicated on the SiO_2 film by reactive ion etching (RIE). The gate recess was formed by wet-chemical etching through using an aqueous solution of phosphate and hydrogen peroxide mixture, then Ti/Pt/Au (3 nm/25 nm/350 nm) was evaporated and lifted off to fabricate the T-shape gate. Finally, after using hydrofluoric acid (HF) to completely clean the SiO_2 film, the devices were fully passivated by an ultrathin Si_3N_4 layer (20 nm in thickness).

In order to obtain the sizes of T-shape gate, we adopted focused ion beam (FIB) to obtain the gate cross-section of InP-based HEMTs of each group. Figures 2(a) and 2(b) show the transmission electron microscope (TEM) images of the cross section of T-shape gates with the same gate length and the different gate stem heights: for the higher T-shape gate shown in Fig. 2(a), the gate length was 120 nm and the gate stem height was 250 nm; for the shorter one shown in Fig. 2(b), the gate length and gate stem height were respectively 120 nm and 165 nm. The gate lengths and gate stem heights of all the groups are summarized in Table 1. For the convenience of analyzing the influence of increasing gate stem height on height on the DC and RF performances of devices, the device of group 3 is called device A, while the device of group 1 is named device B.

Table 1. Features of T-shape gates with different gate stem dimensions (gate length and gate stem height) fabricated under different EB exposure conditions.

Group	Exposure dose ($\mu C/cm^2$)	Exposure line width (nm)	Tri-layer resist	Gate length (nm)	Gate stem height (nm)
1	700	20	thin	120	165
2	700	20	thick	100	250
3	700	50	thick	120	250
4	800	50	thick	135	250

3. Result and discussion

3.1. DC characteristics

The DC characteristics of device A and device B are measured on wafer by using an HP4155A semiconductor parameter analyzer at room temperature. Figure 3(a) displays the DC output characteristics of device A and device B, showing that V_{gs} increases from -1 V to 0.2 V in steps of 0.1 V and V_{ds} increases from 0 V to 1.5 V. The drain current of device A and device B are respectively 1047 mA/mm and 1027 mA/mm at $V_{gs} = 0.2$ V and $V_{ds} = 1.5$ V, a kink effect is well suppressed due to the full passivation of devices. Figure 3(b) shows the transconductance and transfer characteristics of device A and device B at $V_{ds} = 1.5$ V, V_{gs} from -1 V to 0.2 V. The extracted V_{th} of device A is -0.73 V, while the V_{th} of device B is -0.79 V. Besides, the peak transconductance (g_{m_max}) of device A is 1270 mS/mm at $V_{gs} = -0.45$ V, higher than 1200 mS/mm of device B at $V_{gs} = -0.35$ V. Therefore, in our experiment, the positive shift of V_{th} is found to be about 60 mV and the g_{m_max} is increased by 70 mS/mm after increasing the gate stem height of InP-based HEMTs. As is well known that the V_{th} of InP-based HEMT is determined by the one-dimensional structure under the gate metal, while the g_m is synergistically affected by carrier density, carrier mobility, and parasitic resistance. The V_{th}, intrinsic and extrinsic transconductances ($g_{m,int}$ and $g_{m,ext}$) for InP-based HEMTs can be expressed respectively as follows:

$$V_{th} = \phi_b + \frac{E_{f0}}{q} - \frac{q \cdot n_d \cdot d}{\varepsilon} - \frac{\Delta E_c}{q}, \tag{1}$$

$$g_{m,int} = \frac{\mu_n \cdot w \cdot \xi_n \cdot \xi_0}{L_g \cdot d} \cdot (V_{gs} - V_{th}) \propto \mu_n \cdot n_s, \tag{2}$$

$$g_{m,ext} = \frac{g_{m,int}}{1 + g_{m,int} \cdot R_s}, \tag{3}$$

where ϕ_b is the Schottky barrier potential; E_{f0} is the fermi-level at zero two-dimensional electron gas (2DEG) density; n_d is the ionized donor charge; d is the distance between gate metal and InGaAs channel; ΔE_c is the conduction band discontinuity of heterojunction; μ_n is the carrier mobility; L_g is the gate length, W is the gate width, ε_n is relative dielectric constant of the material between channel and gate; ε_0 is the vacuum dielectric constant.

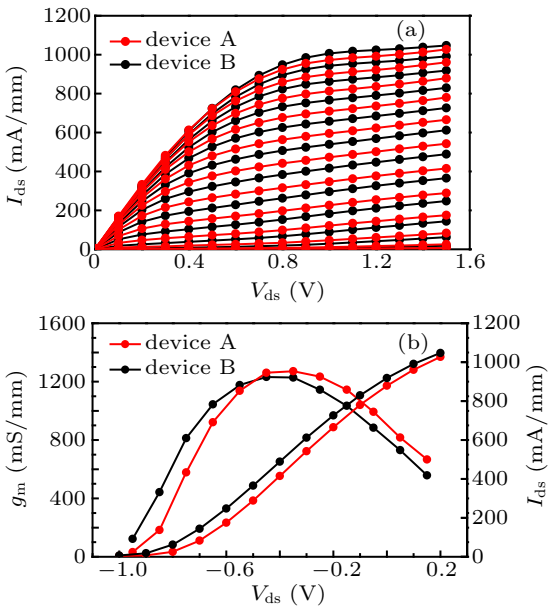


Fig. 3. (a) DC output characteristic of device A and device B; (b) transconductance and transfer characteristics of device A and device B.

In order to investigate the influences of increasing the gate

stem height on the V_{th} and g_m of device, higher resolution TEM images of cross section of gate foot of device A and device B are shown in Figs. 4(a) and 4(b). It can be clearly seen that the length of the gate foot is expanded at the metal–semiconductor interface, caused by metal at the gate foot edges spreading into the gate recess during the gate metal evaporation. So the 120-nm metallurgical gate length of device A and device B have accounted into the gate length expanded by the metal spreading. What is more, in Fig. 4(a), obvious dark areas which are marked with two red ellipses can be observed in the InP etch-stopper layer, which is the typical phenomenon of metal sinking, while the phenomenon of metal sinking is not obvious for device B in Fig. 4(b). Obviously, the dark area and the white area of gate foot are respectively corresponding to Pt and Ti, so the occurrence of Pt sinking reflects that the Schottky contact metals contain not only Ti but also Pt. Compared with device B, device A has a high V_{th}, which can be attributed to the higher ratio of Pt/Ti in Schottky contact metal, which increases the ϕ_b of Ti-based Schottky junction because the Pt-based Schottky junction has a higher ϕ_b than the Ti-based Schottky junction.[18] Besides, the smaller d of device A caused by "Pt sinking" can also increase the V_{th} and g_{m_max}.[19–22] Therefore, the formation of Pt distribution in Schottky contact metal can be explained as being due to the middle metal layer Pt spreading into the gate recess during the gate metal evaporation, which not only expands the gate length but also increases the Ti-based Schottky barrier height. The differences in V_{th} and g_{m_max} between device A and device B are exactly caused by the differences in Pt distribution.

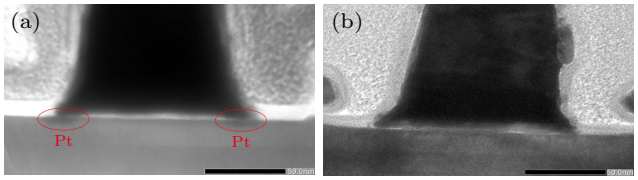


Fig. 4. TEM images of cross section of gate foot of InP-based HEMTs for (a) device A and (b) device B.

Differences in DC performance between the devices of group 2 and group 4 can further reveal that the influence of Pt spreading into the gate recess is different as the gate stem size is changed. Figures 5(a) and 5(b) show the comparisons of transconductance and transfer characteristics of devices of group 2 and group 4 with those of device A at $V_{ds} = 1.5$ V. As shown in Fig. 5 and Table 1, the L_g increases from 100 nm of device of group 2 to 120 nm of device A to 135 nm of device of group 4 with all the gate stems having equal height, which reflects that the bottom pattern of the tri-layer resist replicated on the SiO_2 film becomes wider with EB exposure line width or the EB exposure dose increasing. Meanwhile, the V_{th} is positively shifted from −0.86 V of device of group 2 to −0.73 V of device A to −0.68 V of device of group 4, and the g_{m_max} increases from 1220 mS/mm of device of group 2 to 1270 mS/mm of device A and device of group 4 despite L_g increasing. Comparing with the influence of increasing the gate stem height, similar increases in V_{th} and g_{m_max} are also found with increasing the gate length, illustrating that the influence of Pt spreading on the gate recess at the gate foot edges increases with the bottom pattern of the thick tri-layer resist widening. Through comparing the device of group 2 with that of device B, it can be found that the L_g of device of group 2 is smaller than that of device B, so the thick tri-layer resist seems to be easier to obtain the narrower bottom pattern than the thin tri-layer resist under the same EBL exposure conditions. The reason is that the thin resist is not thick enough to cover the whole SiO_2 film under the unexposed resist in the RIE process, which causes the SiO_2 film to be excessively etched, and thus widening the bottom pattern replicated on the SiO_2 film.[23] In addition, the smaller V_{th} and g_{m_max} of device of group 2 reflect that the Pt spreading is limited by the narrowed bottom pattern of the thick tri-layer resist of group 2, and so is the "Pt sinking". Therefore, comparing device A with device B, it can be found that a wider exposure line width of 50 nm is needed for the thick tri-layer resist to make the L_g of device A equal to that of device B. The more Pt distributions in Schottky contact metal of device A can be explained as the fact that the slightly narrower bottom pattern of the thick tri-layer resist is obtained after the EBL exposure, and for the thick tri-layer resist of device A, the influence of Pt spreading into the gate recess is larger, which expands the gate length to the same value of device B. Up to here, it can be concluded that the influence of the spreading metal at the gate foot edges can be increased with gate stem height or the gate length increasing, leading the devices to manifest the differences in the DC performances. However, as for the further reason for the difference in spreading metal among different gate stem sizes,

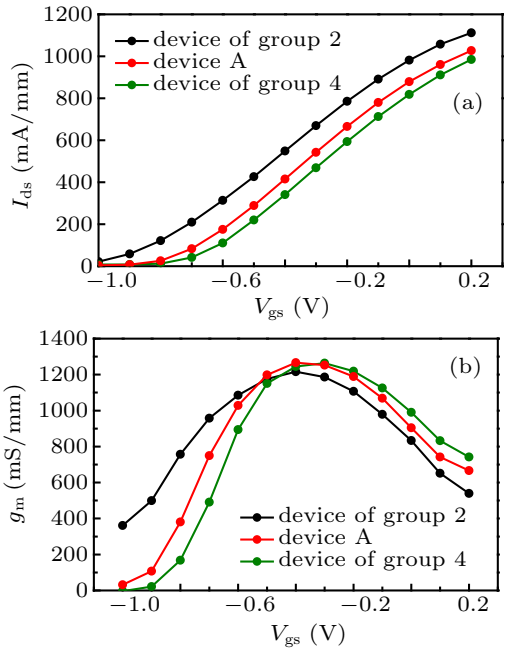


Fig. 5. (a) DC output characteristic of device A, devices of group 2 and group 4; (b) transconductance and transfer characteristics of device A, devices of group 2 and group 4.

we believe that it is the result of internal stress balance among the different metal layers in gate. The Pt is subjected to tensile stress in the Ti/Pt/Au gate stem,[24] which can increase with gate stem height or the gate length increasing, thus leading the more obvious phenomenon of Pt to spread into the gate recess.

3.2. Microwave characteristics

Microwave performances of device A and device B are characterized via Agilent 8363B PNA vector network analyzer. Their *S*-parameters are measured and extracted at certain bias points. The test frequency range is limited from 0.1 GHz to 40 GHz. On-wafer open and short methods are used to exclude the effects of pad capacitances and inductances from the measured device *S*-parameters. The cutoff frequency f_t and the maximum oscillation frequency f_{max} are obtained by extrapolating the curve of current gain (H_{21}) followed by a slope of 20 dB/dec and Masaon's unilateral gain (U_g) followed by a slope of 20 dB/dec. Figures 6(a) and 6(b) show the H_{21}, maximum available gain, and maximum stable gain (MAG/MSG), (U_g), and stability factor (k) against frequency for device A and device B at $V_{ds} = 1.0$ V, $V_{gs} = -0.3$ V, where the maximum value of f_t ($f_{t,max}$) is achieved. From Figs. 6(a) and 6(b), the $f_{t,max}$ and the f_{max} of device A are 270 GHz and 440 GHz, respectively, while the $f_{t,max}$ and the f_{max} of device B are 240 GHz and 367 GHz, respectively. The RF characteristics are found to be obviously improved after the gate stem height of devices has been increased. The f_t and f_{max} are expressed as

$$f_t = \frac{g_{mi}}{2\pi(C_{gs}+C_{gd})[1+g_{oi}(R_s+R_d)]+C_{gd}\cdot g_m(R_s+R_d)}, \quad (4)$$

$$f_{max} = \frac{f_{t,int}}{2\sqrt{g_{oi}(R_g+R_s)+\pi\cdot f_{t,int}\cdot C_{gd}(R_g+R_s)}}, \quad (5)$$

where C_{gs} is the parasitic capacitance between gate and source; C_{gd} is the parasitic capacitance between gate and drain; R_g, R_d, and R_s are respectively the parasitic resistances of gate, drain, and source; g_{mi} is the intrinsic transconductance; g_{oi} is the conductance between the drain and the source; $f_{t,int}$ is the value of f_t for the core part of HEMT without any parasitic resistance, and capacitance. It is obvious that the f_t and f_{max} of InP-based HEMT are influenced by the intrinsic transconductance, parasitic resistance, and capacitance, which are related to the passivation layer, the shape of gate and the gate recess design. In our experiments, since the process of passivation and the gate recess of all devices are the same, so the main factor that influences the RF performances of InP-based HEMTs is the shape of gate. In order to explain the increase in f_t and f_{max}, a small signal model based on InP-HEMTs biased at $f_{t,max}$ is developed by using the deembedded *S*-parameters.[25] The small signal model parameters are tuned repeatedly until the measured and simulated *S*-parameters are fitted very well, which is shown in Fig. 5. The main small signal model parameters are summarized in Table 2.

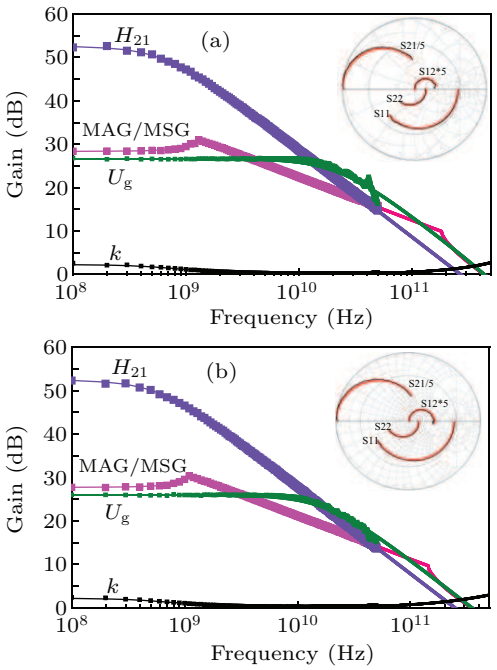


Fig. 6. RF characteristics of InP-based HEMTs for (a) device A at $f_{t,max}$ and (b) device B at $f_{t,max}$.

Table 2. Parameters of small signal equilibrium circuit of device A and device B biased at $f_{t,max}$.

Device	C_{gs} (fF)	C_{gd} (fF)	g_{mi} (mS)	g_{oi} (mS)	R_d (Ω)	R_s (Ω)	R_g (Ω)	f_t (GHz)	f_{max} (GHz)
A	68	11.7	144	13.3	1.5	0.5	2.3	270	460
B	71	15.1	140	13.5	1.5	0.5	2.5	240	370

Based on the small signal model, after increasing the gate stem height, the value of g_{mi} increases from 1400 mS/mm to 1440 mS/mm at the bias of $f_{t,max}$, while the values of C_{gs} and C_{gd} decrease from 71 fF to 68 fF and from 15.1 fF to 11.7 fF, respectively. The higher gate resistance of device B can be influenced by the voids formed in gate head during the gate metal evaporation. The increase of g_{mi} for the high gate device is because of the reduced distance between the gate metal and the InGaAs channel, resulting from the occurrence of the Pt sinking. And the parasitic capacitances C_{gs} and C_{gd} decrease because the distance between gate-source and gate–drain increases with the gate stem height of device increasing. According to Eqs. (4) and (5), the f_t and f_{max} are both proportional to g_{mi} and inversely proportional to the C_{gs} and C_{gd}. Therefore, the decreasing of parasitic capacitance of T-shape gate can be a very effective way of improving the RF performances of InP-based HEMT, because the smaller parasitic capacitances have shorter charge–discharge time, which makes

the RF frequency response of device faster. For further explaining the improvement of RF frequency response brought by increasing the gate stem height, an analytical model of f_t based on small signal equivalent circuit is adopted and shown in Fig. 7, which consists of extrinsic parameters R_d, R_s, C_{gsext}, and C_{gdext} and intrinsic parameters C_{gsi}, C_{gdi}, g_{mi}, and g_{oi}.[26] All the parameters can be substituted into the expression of f_t, and the total delay τ can be divided into three parts, which can be given as

$$f_t = \frac{g_{mi}}{2\pi\left\{C_{gs}+C_{gd}+C_{gd}g_{mi}(R_s+R_d)\left[1+\left(1+\frac{C_{gs}}{C_{gd}}\right)\frac{g_{oi}}{g_{mi}}\right]\right\}},$$

$$C_{gs} = C_{gsi}+C_{gsext}, \quad C_{gd} = C_{gdi}+C_{gdext}, \tag{6}$$

$$\tau = \frac{1}{2\pi f_t} = \tau_t + \tau_{ext} + \tau_{par}, \tag{7}$$

$$\tau_t = \frac{C_{gsi}+C_{gdi}}{g_{mi}} = \frac{L_g}{V_e}, \tag{8}$$

$$\tau_{ext} = \frac{C_{gsext}+C_{gdext}}{g_{mi}}, \tag{9}$$

$$\tau_{ext} = C_{gd}(R_s+R_d)\left[1+\left(1+\frac{C_{gs}}{C_{gd}}\right)\frac{g_{oi}}{g_{mi}}\right], \tag{10}$$

where τ_t is the transit time proportional to intrinsic capacitance and inversely proportional to g_{mi}; V_e is the average electronic velocity under T-shape gate; τ_{ext} is the parasitic delay proportional to extrinsic capacitance and inversely proportional to g_{mi}; τ_{ext} is the delay mainly associated with R_d and R_s;[7] τ_t is equal to L_g/V_e, so the τ_t is the same for device A as that for device B. But because of the larger g_{mi} of device A, the intrinsic capacitance of device A must also be larger than that of device B to ensure that they have the same τ_t, which is caused by the Pt sinking. What is more, for device A, the whole parasitic capacitances C_{gs} and C_{gd} are smaller than those for device B, so it can be deduced that the extrinsic capacitances C_{gsext} and C_{gdext} should be also smaller than those for device B from Eq. (6), which is obviously due to the increasing of the height of gate stem. So far, based on Eq. (9), it can be determined that the τ_{ext} of device A decreases compared with that of device B. As for the τ_{par} in the total delay, through calculation, the τ_{par} of device A can be smaller than that of device B because of the smaller parasitic capacitances C_{gs} and C_{gd} and the larger g_{mi} for device A.

Through the analytical model of f_t, it can be concluded that one main reason for the improvement in RF performance brought by increasing the gate stem height is the effective decrease of the C_{gsext} and C_{gdext}. More specifically, as the distance between the gate head and the source/drain increases, the external parasitic capacitance between them decreases. Another reason is the larger g_{mi} of the high gate device, caused by the closer distance between Pt in Schottky metal and the channel. Apart from the increasing of the gate stem height, other methods are also adopted for minimizing the gate parasitic capacitance in our experiments: the SiO_2 layer, which is usually used to help to fabricate the T-shape gate, is removed after the gate has been fabricated, thus eliminating the the influence of the SiO_2 layer on increasing parasitic capacitance. Furthermore, the 20-nm-ultra-thin Si_3N_4 layer is used to fully passivate the surface of device so that the value of g_m can be increased and meanwhile the increase of C_{gd} can be limited by the ultra-thin passivation layer.[27]

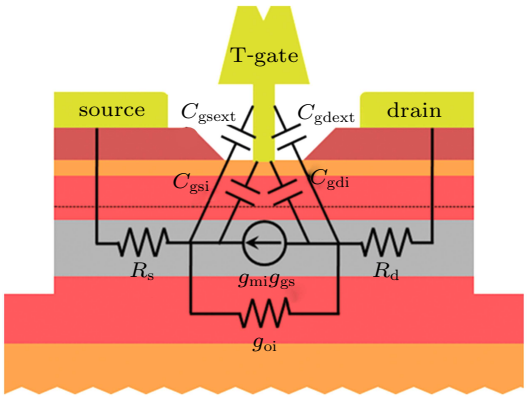


Fig. 7. Small signal equivalent circuit model.

4. Conclusions

In this paper, we investigated the influences of increasing the gate stem height of T-gate fabricated by tri-layer resist process on the DC and RF performances of InP-based HEMTs. The gate stem height of InP-based HEMT with a gate 120 nm in length is increased from 165 nm to 250 nm through increasing the thickness of the bottom resist layer in our experiments. The distribution of Pt in Schottky contact metal of the gate foot edges of the high gate stem device is found to be more than that of short gate system, leading the Schottky barrier to rise and the "Pt sinking to occur". So the threshold voltage and the transconductance of the high gate stem device are larger than that of the short gate system. The distribution of Pt in the Schottky metal is because the middle layer metal Pt in Ti/Pt/Au gate spreads into the gate recess to form a Schottky contact, which varies with the gate stem height or the gate length. We find that the spreading Pt in Schottky contact metal of gate foot edges can be increased with increasing the gate stem height or the gate length, which further expands the gate length. Therefore, it is suggested that the control of the expanded gate length deserves attention while the gate stem height is increased. As for the RF performances, the high gate stem device exhibits higher f_t and f_{max} than the short gate stem device because of the lower extrinsic parasitic capacitance and the higher intrinsic transconductance, both of which would be essential in reducing the parasitic delay in the total delay of device. As the parasitic delay plays a more and more important role in improving the RF performance by scaling

down the gate length, the increasing of the gate stem height can be an adoptable method to further improve the RF performances of InP-based HEMT. Moreover, with radiation damage mechanism studied adequately and the effective anti-radiation hardness proposed, the the InP-based HEMTs' applications in space can be expected in near future.[28]

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