

PBTI stress-induced *1/f* noise in n-channel FinFET

Dan-Yang Chen(陈丹旸), Jin-Shun Bi(毕津顺), Kai Xi(习凯), and Gang Wang(王刚)
Citation: Chin. Phys. B, 2020, 29 (**12**): 128501. DOI: 10.1088/1674-1056/abaee4
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Carbon nanotube-based nanoelectromechanical resonatoras mass biosensor

Ahmed M. Elseddawy, Adel H. Phillips, Ahmed S Bayoumi
Chin. Phys. B, 2020, 29 (**7**): 078501. DOI: 10.1088/1674-1056/ab888f

Negative gate bias stress effects on conduction and low frequency noise characteristics in p-type poly-Si thin-film transistors

Chao-Yang Han(韩朝阳), Yuan Liu(刘远), Yu-Rong Liu(刘玉荣), Ya-Yi Chen(陈雅怡), Li Wang(王黎), Rong-Sheng Chen(陈荣盛)
Chin. Phys. B, 2019, 28 (**8**): 088502. DOI: 10.1088/1674-1056/28/8/088502

Analysis of tail bits generation of multilevel storage in resistive switching memory

Jing Liu(刘璟), Xiaoxin Xu(许晓欣), Chuanbing Chen(陈传兵), Tiancheng Gong(龚天成), Zhaoan Yu(余兆安), Qing Luo(罗庆), Peng Yuan(袁鹏), Danian Dong(董大年), Qi Liu(刘琦), Shibing Long(龙世兵), Hangbing Lv(吕杭炳), Ming Liu(刘明)
Chin. Phys. B, 2018, 27 (**11**): 118501. DOI: 10.1088/1674-1056/27/11/118501

Low frequency noise and radiation response in the partially depleted SOI MOSFETs with ion implanted buried oxide

Liu Yuan, Chen Hai-Bo, Liu Yu-Rong, Wang Xin, En Yun-Fei, Li Bin, Lu Yu-Dong
Chin. Phys. B, 2015, 24 (**8**): 088503. DOI: 10.1088/1674-1056/24/8/088503

Low frequency noise in asymmetric double barrier magnetic tunnel junctions with a top thin MgO layer

Guo Hui-Qiang, Tang Wei-Yue, Liu Liang, Wei Jian, Li Da-Lai, Feng Jia-Feng, Han Xiu-Feng
Chin. Phys. B, 2015, 24 (**7**): 078504. DOI: 10.1088/1674-1056/24/7/078504

PBTI stress-induced $1/f$ noise in n-channel FinFET*

Dan-Yang Chen(陈丹旸)[1], Jin-Shun Bi(毕津顺)[1,2,†], Kai Xi(习凯)[2], and Gang Wang(王刚)[3]

[1] *University of Chinese Academy of Sciences, Beijing* 100049, *China*
[2] *Institute of Microelectronics of the Chinese Academy of Sciences, Beijing* 100029, *China*
[3] *Semiconductor Manufacturing International Corporation, Shanghai* 201203, *China*

(Received 1 May 2020; revised manuscript received 1 August 2020; accepted manuscript online 13 August 2020)

The influence of positive bias temperature instability (PBTI) on $1/f$ noise performance is systematically investigated on n-channel fin field-effect transistor (FinFET). The FinFET with long and short channel ($L = 240$ nm, 16 nm respectively) is characterized under PBTI stress from 0 s to 10^4 s. The $1/f$ noise features are analyzed by using the unified physical model taking into account the contributions from the carrier number and channel mobility fluctuations. The I_d–V_g, I_d–V_d, I_g–V_g tests are conducted to support and verify the physical analysis in the PBTI process. It is found that the influence of the channel mobility fluctuations may not be neglected. Due to the mobility degradation in a short-channel device, the noise level of the short channel device also degrades. Trapping and trap generation regimes of PBTI occur in high-k layer and are identified based on the results obtained for the gate leakage current and $1/f$ noise.

Keywords: PBTI, $1/f$ noise, FinFET, mobility fluctuation

PACS: 85.40.Qx, 85.30.–z, 85.30.De, 85.35.–p **DOI:** 10.1088/1674-1056/abaee4

1. Introduction

Since the advent of the 22-nm complementary metal–oxide–semiconductor (CMOS) process node, the fin field-effect transistor (FinFET) structure has been introduced into mass-market production and become a dominant device architecture in 16/14 nm and down to 5-nm process node due to their superior electrostatic control over the short-channel effects[1] as described in the 2017 International Roadmap for Devices and Systems (ITDS).[2] To date, high-k and metal-gate (HKMG) has been widely used in FinFET fabrication due to its superior performance in terms of drive current and leakage current.[3] However, it has been also reported that the bulk defect density of HfO_2 is approximately one order of magnitude higher than that of SiO_2.[4] Moreover, the reliability issues related to the gate dielectric such as bias temperature instability (BTI), trap-assisted tunneling (TAT) and low frequency noise (LFN) have become increasingly serious with the dimensions of the process node decreasing.[5–8]

As is well known, the gate oxide quality and reliability strongly depend on the type of high-k material and the interfacial oxide layer.[9] The measuring of low-frequency noise also known as $1/f$ noise is usually used as a non-destructive technique for evaluating the quality of the oxide–semiconductor interface and channel layers.[10,11] Many studies reported in the literature have pointed out that carrier number fluctuation (Δn) and correlated mobility fluctuation ($\Delta\mu$) are the main physical mechanisms that give rise to the $1/f$ noise phenomena.[12–14] The current fluctuations in nano-scale transistors brings about the random telegraph noise (RTN) dominated by the single-type traps which also leads to the generation of a Lorentz-like $1/f$ noise spectrum.[15]

With the HfO_2 widely used as high-k gate dielectric layer, the positive bias temperature instability (PBTI) becomes an increasingly critical reliability issue, severely affecting device performance and lifetime.[16–18] It is well established that the charging of the pre-existing traps (trapping-TP) and newly generated traps in bulk oxide (trapping generation-TG) are the intrinsic mechanisms of PBTI.[19–21]

Most of previous studies focused either on the effects of the $1/f$ noise or on the effects of PBTI, and few studies have examined the relationships between $1/f$ noise and PBTI. In this work, the effect of PBTI on the $1/f$ noise is studied in detail, particularly the performances of FinFETs with different channel lengths. The changes in sub-threshold swing (ΔSS), drain current (ΔI_d), and gate leakage current (ΔI_g) in the PBTI process are also fully characterized in order to determine the physical origin of the $1/f$ noise induced by PBTI stress.

2. Device structure and measurement flow

2.1. Device structure

The n-FinFETs investigated in this work were fabricated on the conventional FinFETs integration flow by using the replacement metal gate (RMG) process. To form ultra-thin fins with relaxed pitch, the self-aligned double pattern method was implemented. Fin shallow trench isolation (STI) and punch-through stop doping were carried out. The width (T_{fin}) and height (H_{fin}) of the fins were 15 nm and 42 nm, respectively. The atomic layer deposition (ALD) process was utilized to

*Project supported by the National Natural Science Foundation of China (Grant No. 61634008).
†Corresponding author. E-mail: bijinshun@ime.ac.cn
© 2020 Chinese Physical Society and IOP Publishing Ltd

form a sequential SiO_2/HfO_2/TiN/TiAl/TiN/W multilayer as the gate and dielectric layer. The equivalent oxide thickness (EOT) of the test devices was 1.47 nm. The effect channel lengths of the two groups of test devices were $L_l = 240$ nm and $L_s = 16$ nm, respectively. Both groups have 3 test devices. All of the FinFETs in the tested devices had 10 fins ($N_{fin} = 10$). The effective device width was given by $N_{fin} \cdot (2H_{fin} + T_{fin})$ and was equal to approximately 990 nm. The FinFET structure is illustrated in Fig. 1(a), while the transmission electron microscopy image (TEM) of the FinFET is shown in Fig. 1(b).

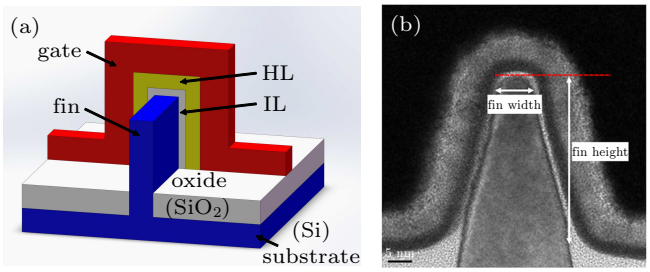


Fig. 1. Schematic illustration and TEM image of the tested FinFETs, with IL referring to interfacial layer (SiO_2), and HL denoting high-k layer (HfO_2).

2.2. Measurement flow

A series of experiments was performed to characterize the changes in the various electrical parameters of the tested devices. As shown in Fig. 2, the pre-set BTI program of Keysight B1500A was used for PBTI test with the internal threshold voltage (V_{th}) monitor. The total PBTI stress time was 10^4 s. When the accumulated stress time reached 0, 10, 10^2, 10^3, and 10^4 s, the PBTI stress was suspended and a series of tests was performed, including the I_d–V_g, I_d–V_d, I_g–V_g tests by using the Keysight B1500A system and the $1/f$ noise tests by using the Proplus 9812DX noise measurement system. The $1/f$ noise characteristics were measured under the bias condition of $V_d = 0.1$ V and $V_g = V_{th} + 0.1$ V, with V_{th} calculated by the g_m/I_d method on the I_d–V_g data.[22]

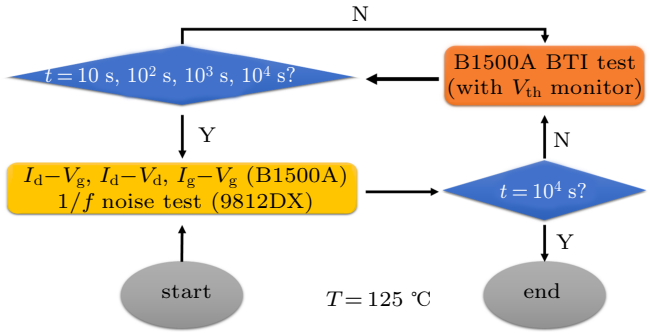


Fig. 2. Flowchart of experimental tests of n-FinFETs, with t representing accumulated PBTI stress time.

3. Results and discussion

As shown in Fig. 3, the normalized $1/f$ noise of the test devices shows a Lorentzian-like shape, implying that the traps are not uniformly distributed in the gate dielectric layer.[12,23,24] What is more, the Lorentzian-like shape of the noise is also affected by the variation of the device as shown in Fig. 4. The three n-FinFETs with the same size under tests show different noise patterns. To quantitatively characterize the $1/f$ noise and eliminate measurement errors and device variation as much as possible, the experimental data are fitted by $WLS_{id}/I_d^2 = A \cdot f^{\beta}$. The 10 Hz is commonly used as the indicator of noise level.[11,13,25] Therefore, in this work, the 10 Hz value of the fitted lines ($A \cdot 10^{\beta}$) is taken as the value of the noise power spectrum as shown in Fig. 4. The selected data are compensated for by channel area (WLS_{id}/I_d^2) to compare the noise levels between long- and short-channel device as shown in Fig. 5.

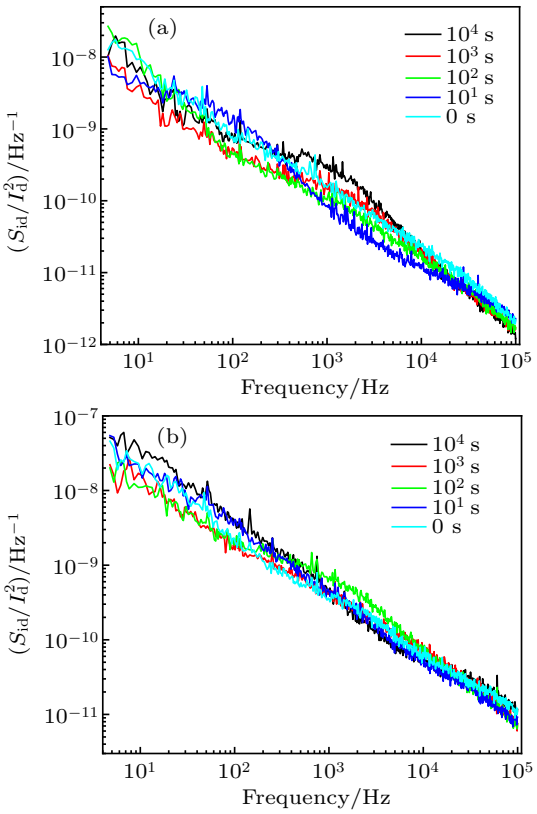


Fig. 3. Normalized $1/f$ noise power spectrum of the n-FinFETs during PBTI stress for $L = 240$ nm (a) and 16 nm (b), where experimental data are fitted by $WLS_{id}/I_d^2 = A \cdot f\beta$ and fitted data at 10 Hz are taken as noise power spectrum value.

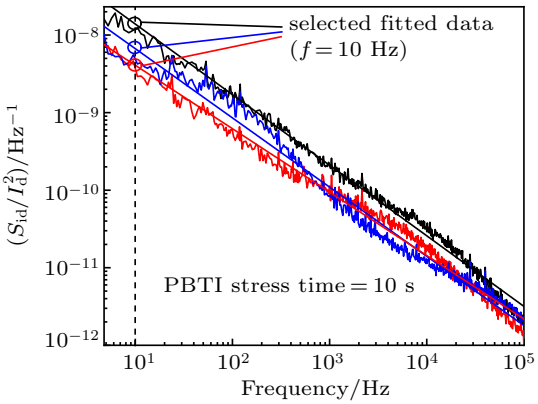


Fig. 4. Normalized $1/f$ noise of three n-FinFETs under tests compensated for by channel area when accumulated PBTI stress time reaches 10 s ($L = 240$ nm). It can be seen that their individual differences are obvious.

Figure 5 shows the normalized $1/f$ noise compensated for by the channel area (WLS_{id}/I_d^2) during PBTI stress. It is observed that the compensated normalized noise spectrum of the test devices first decreases and then increases during the PBTI stress, indicating that two competing physical processes contribute to the PBTI effect. The noise power of the short-channel device is always lower than that of the long-channel device.

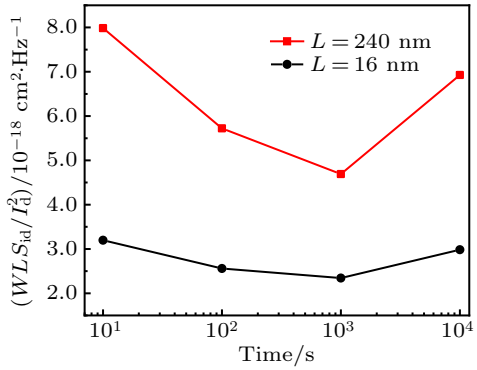


Fig. 5. Normalized $1/f$ noise of the n-FinFETs compensated for by channel area during PBTI stress, showing that noise spectrum first deceases and then increases during PBTI stress.

However, the short-channel device should have higher noise level because the poor reliability region at the edge of the channel exerts a greater effect on the $1/f$ noise characteristic in short-channel device than in long-channel device as shown in Fig. 6. However, this expectation is not matched by the obtained experimental data.

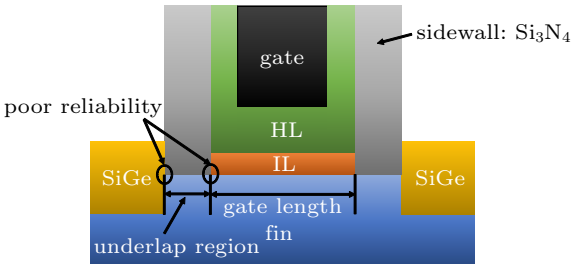


Fig. 6. Illustration of poor reliability region at channel edge. The influence of these regions become weaker with gate length increasing.

To understand the origin of this phenomenon, the unified model proposed by Hung *et al.*[14] is used to calculate the trap density in the tested devices during PBTI stress. This model is referred to as the Hung model hereinafter and expressed as follows:

$$\frac{WLS_{id}}{I_d^2} = \frac{kT}{f\gamma}\left(\frac{1}{N} + \alpha\mu\right)^2 N_t(E_{fn}), \tag{1}$$

where kT is the thermal energy, γ is the attenuation coefficient (10^8 cm^{-1}), W is the channel width, L is the channel length, and N is the surface density of the inversion carriers. In this work, N is calculated through the approximation of $N = C_{ox}(V_g - V_{th})/q$, where q is the elementary electron charge. μ is the effective mobility (117.2 cm/V·s for short-channel device and 304.4 cm/V·s for long-channel device), α is the scattering coefficient (2.7×10^{-13} V·s), and $N_t(E_{fn})$ is the trap density (N_t) at a quasi Fermi level (E_{fn}).

The trap density $N_t(E_{fn})$ is calculated through Eq. (1) on the data which are shown in Fig. 5. As shown in Fig. 7, both the trap density and gate leakage current first decrease and then increase during PBTI stress, which is similar to the trend observed for the $1/f$ noise spectrum, indicating that the TP and TG process mentioned above are present, respectively. The I_g–V_g test during PBTI stress can be considered as the stress induced leakage current (SILC) test. It is generally believed that the gate leakage current is generated by the carrier tunneling with the assistance of the traps inside the gate dielectric. Therefore, the gate leakage current can be used as an indicator of the quality of the gate dielectric.[18] That is to say, the type of traps involved in the $1/f$ noise and the gate leakage are the same as shown in Fig. 8. At the same time, it is observed that the trap density of the short-channel device is always higher than that of the long-channel device, which may be due to the poor reliability at the edge of the channel mentioned above.

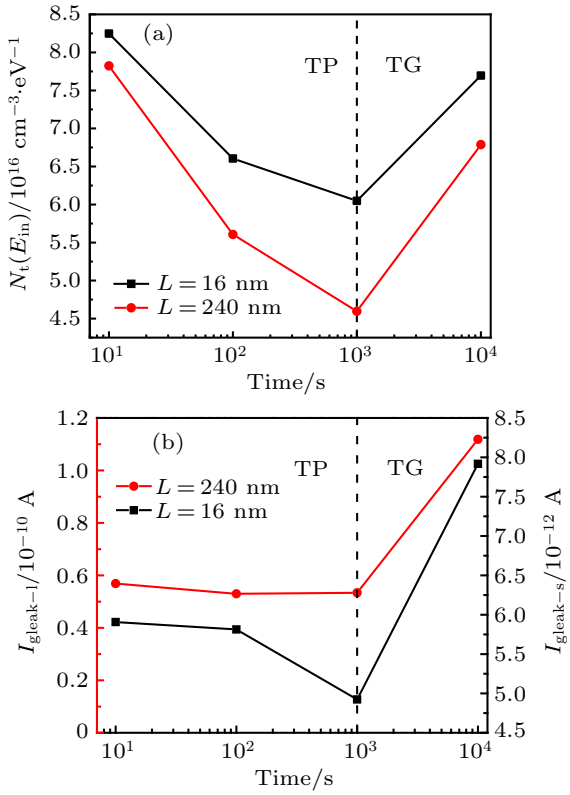


Fig. 7. (a) Trap density ($N_t(E_{fn})$) and (b) gate leakage current ($V_g = 0.8$ V) of n-FinFETs with different channel lengths during PBTI stress. Both of them first decease and then increase during PBTI stress.

However, it is still unclear why the noise spectrum is lower in the short-channel device. To determine the origin of this phenomenon, the contributions of the different physical sources of the $1/f$ noise in the test device are compared with each other to understand the internal conditions of the device during the tests. In the Hung model, when the channel mobility fluctuation mechanism has no effect on $1/f$ noise at

all, α equals 0, and $(1/N+\alpha\mu)^2$ can be reduced to $(1/N)^2$. Equation (1) can be transformed into

$$\frac{WLS_{\rm id}}{I_{\rm d}^2}=\frac{kTN_{\rm t}(E_{\rm fn})}{f\gamma N^2}. \tag{2}$$

In this work, the $1/f$ noise spectra are measured in a linear region. N is calculated by $C_{\rm ox}\left(V_{\rm g}-V_{\rm th}\right)/q$. Equation (2) can be transformed into

$$\frac{WLS_{\rm id}}{I_{\rm d}^2}=\frac{q^2kTN_{\rm t}(E_{\rm fn})}{f\gamma C_{\rm ox}^2\left(V_{\rm g}-V_{\rm th}\right)^2}, \tag{3}$$

which is also the expression of the McWhorter model. That is to say, when $\alpha\neq 0$, $kTN_{\rm t}(E_{\rm fn})/f\gamma N^2$ can be seen as the contribution of the carrier number fluctuation mechanism, which will be referred to as Δn in the following and can be calculated by substituting the data in Fig. 7(a) into Eq. (3). For example, the trap density of the short-channel device under 10^4 s, the PBTI stress is 7.6949×10^{16} cm$^{-3}\cdot$eV^{-1}. N is 1.46814×10^{12} cm^{-2}, and

$$\begin{aligned}\frac{kTN_{\rm t}(E_{\rm fn})}{f\gamma N^2}&=\frac{0.026\times7.6949\times10^{16}}{10\times10^8\times\left(1.46814\times10^{12}\right)^2}\\&=9.282\times10^{-19}\ {\rm cm}^2\cdot{\rm Hz}^{-1}.\end{aligned}$$

The rest of the $1/f$ noise, which is considered as $WLS_{\rm id}/I_{\rm d}^2-kTN_{\rm t}(E_{\rm fn})/f\gamma N^2$, can be considered to be influenced by the channel mobility fluctuation mechanism, which will be referred to as $\Delta\mu$ in the following . It should be noted here that when the mobility fluctuation contribution is calculated, $WLS_{\rm id}/I_{\rm d}^2$ is the measurement value as shown in Fig. 5, the $N_{\rm t}(E_{\rm fn})$ is already shown in Fig. 7(a) and calculated by Eq. (1), and $kTN_{\rm t}(E_{\rm fn})/f\gamma N^2$ can be obtained.

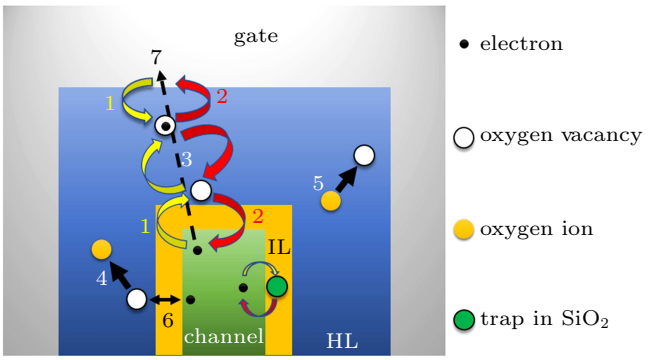


Fig. 8. Illustration of defect behaviors in gate dielectric, showing: 1 charge capture from channel/gate, 2 charge emission to channel/gate, 3 tunneling between two traps, 4 trap generation, 5 trap recombination, 6 $1/f$ noise, and 7 gate leakage current.

As shown in Fig. 9(a), the contribution of the channel mobility fluctuations ($\Delta\mu$) is greater than that of the carrier number fluctuations (Δn). The contribution of $\Delta\mu$ in the long-channel device is significantly larger than that in the short-channel device. The saturated drain current can be used as a measure of the saturated mobility of the device.[26] As shown in Fig. 9(b), the short-channel device suffers saturated mobility degradation due to the scaling down its channel length. The mobility can be expressed as[27]

$$\mu=\frac{\mu_0}{1+\varepsilon/\varepsilon_{\rm c}}, \tag{4}$$

where μ_0 is the low-field mobility, ε is the electric field in the channel, and $\varepsilon_{\rm c}$ is the critical field strength. In short-channel devices, the electric field is comparable to the critical field strength, thereby lowering the mobility. This undoubtedly gives rise to the phenomenon shown in Fig. 9(a) that the contribution of mobility fluctuation in long channel-device is higher than that in short-channel device. That is to say, the effect of the channel mobility fluctuations on the $1/f$ noise cannot be neglected, and even plays a major role in some cases. In this case, the $1/f$ noise characteristics should be affected by the mobility degradation caused by PBTI stress. However, the measurement result shown in Fig. 5 does not show obvious effects. This is because the mobility degradation caused by PBTI stress is too small. As shown in the inset of Fig. 9(b), the mobility of the test device shows little change in PBTI stress time. Therefore, the $1/f$ characteristics do not seem to be affected by mobility degradation.

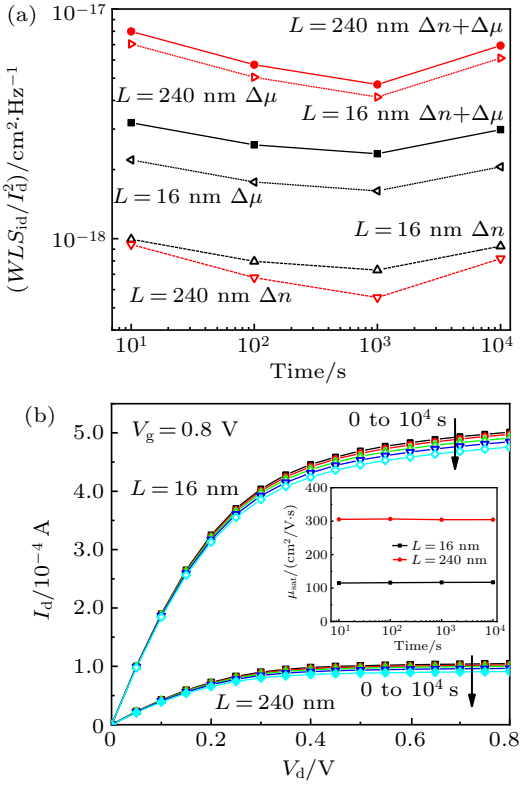


Fig. 9. (a) Contributions of different $1/f$ noise mechanisms and (b) $I_{\rm d}$–$V_{\rm d}$ characteristics of n-FinFETs with different channel lengths during PBTI stress, showing that mobility degradation during PBTI stress is not that obvious.

In all of the $1/f$ noise models discussed above, the power of the $1/f$ noise spectrum is considered to be inversely proportional to the frequency ($S_{\rm id}\propto f^{-1}$). However, in fact, neither of the noise spectrum power and frequency shows a strict

inverse relationship, but rather a slight deviation from this relationship is observed to be $S_{id} \propto f^{\beta}$,[13,23] where $|\beta|$ is in a range of 0.8–1.2. To describe the trap distribution along the depth of the dielectric, an exponential trap distribution model is proposed below[23] and given as follows:

$$N_{tr} = N_{T0}\, e^{\gamma(|\beta|-1)y}, \tag{5}$$

where N_{tr} is the trap density at the distance y from the interface, N_{T0} is the trap density at the silicon–oxide interface, and γ is the attenuation coefficient (10^8 cm^{-1}). For $\beta < -1$, the trap density increases from the substrate interface to the metal gate. By contrast, for $\beta > -1$, the trap density decreases. For $\beta = -1$, the traps are uniformly distributed.

The values of slope (β) of the fitted lines of the data in Fig. 3 are obtained as shown in Fig. 10. During PBTI stress, the slope (β) of the $1/f$ noise spectrum of the test device first increases then decreases, corresponding to the TP and TG process mentioned above, respectively. Combining together the analysis of the trap density in Fig. 7(a), these results show that the TP process and TG process in PBTI effect mainly occur in the oxide layer away from the substrate interface and affect the $1/f$ noise spectrum. That is to say, the oxide vacancies in the HfO_2 layer are the main origin of the $1/f$ noise induced by the PBTI stress. In addition, it is observed that the slope in the short-channel device (β_s) is higher than that in the long-channel device (β_l) during most of the test time. Considering these results in conjunction with the trap density shown in Fig. 7(a), it can be concluded that the short-channel devices have more traps near the interface than the long-channel devices. This may be due to the poor oxide quality in the edge of the channel.

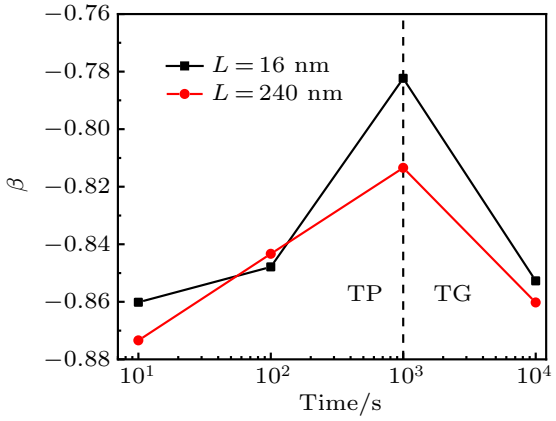


Fig. 10. Slopes of the $1/f$ noise spectrum of n-FinFETs with different channel lengths during PBTI stress, indicating that slopes first increase and then decreases during PBTI stress.

Sub-threshold swing (SS) calculated as $\partial V_g/\partial I_d$ in sub-threshold region is an indicator of the interface traps[28] as shown in Eq. (6). The sub-threshold swing is given by

$$\Delta SS = \ln(10)\, kT \cdot \frac{q}{C_{ox}} \Delta D_{it}, \tag{6}$$

where C_{ox} is the capacitance of the gate dielectric, and ΔD_{it} is the change of the interface traps. Figure 11 shows the SS of the long-channel device (left Y axis) and of the short-channel device (right Y axis) as a function of time. It is observed that the SS of the long-channel device shows relatively little changes, while the change in the SS of the short-channel device is more pronounced. This may be caused by an irregular crystal lattice existing near the substrate interface in the channel edge region that degrades under the PBTI stress. However, if the interface trap has a relatively obvious influence on the $1/f$ noise, the increase of the trap density in Fig. 7(a) in 10^2 s–10^3 s in short-channel device should be higher than in long-channel device and the decrease of the slope of the $1/f$ noise in Fig. 10 in 10^2 s–10^3 s in short-channel device should be lower than in long-channel device. Therefore, the influence of the interface traps is negligible.

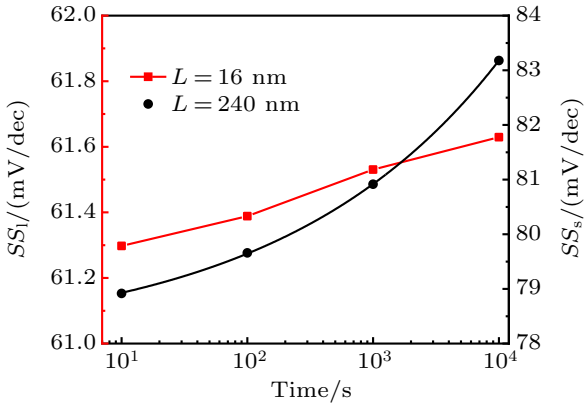


Fig. 11. Sub-threshold swing (SS) degradation of n-FinFETs with different channel lengths during PBTI stress. SS in short-channel device shows more obvious increase than in long-channel device.

4. Conclusions

In this work, we mainly study the effect of the PBTI stress on the $1/f$ noise characteristics of n-channel FinFETs. Through the study of $1/f$ noise characteristics, the changes in the density and distribution of the traps in the gate dielectric layer during the PBTI stress are explored. Based on the analysis of the $1/f$ noise and gate leakage current, it is found that the TP process and TG process successively dominate the degradation process of PBTI, and these processes mainly occur in the high-k layer. Meanwhile, the comparative analyses of n-FinFETs with different channel lengths indicate that mobility fluctuations cannot be ignored in the $1/f$ noise. The mobility degradation due to the short-channel length also has significant effects on the $1/f$ noise spectrum. Finally, the SS is introduced to analyse the characteristics of interface traps during PBTI stress. Although the short-channel device shows additional degradation during the PBTI stress due to the irregular lattice structure at the channel edges, the changes in the interface traps do not cause the $1/f$ noise spectrum to additionally degrade.

References

[1] Auth C, Allen C, Blattner A, Bergstrom D, Brazier M, Bost M, Buehler M, Chikarmane V, Ghani T and Glassman T 2012 *Symposium on VLSI Technology (VLSIT)*, pp. 131–132

[2] https://irds.ieee.org/roadmap-2017

[3] Wang W, Luo J, Jiang H and Feng J H 2019 *Ecs J. Solid State Sci. Technol.* **8** P30

[4] Kalpat S, Tseng H H, Ramon M, Moosa M, Tekleab D, Tobin P J, Gilmer D C, Hegde R I, Capasso C and Tracy C 2005 *IEEE Trans. Dev. Mater. Reliab.* **5** 26

[5] Dabhi C K, Roy A S and Chauhan Y S 2019 *IEEE Trans. Electron Dev.* **66** 2892

[6] Gorchichko M, Cao Y, Zhang E X, Yan D, Gong H, Zhao S E, Wang P, Jiang R, Liang C and Fleetwood D M 2019 *IEEE Transactions on Nuclear Science*

[7] Kang S C, Kim S M, Jung U, Kim Y, Park W and Lee B H 2019 *Solid-State Electron.* **158** 46

[8] Patra D, Reza A K, Katoozi M, Cannon E H, Roy K and Cao Y 2018 *IEEE International Reliability Physics Symposium (IRPS)*, pp. 5C.5-1–5C.5-4

[9] Claeys C, He L, O'Sullivan B J, Veloso A, Horiguchi N, Collaert N and Simoen E 2018 *Ecs J. Solid State Sci. Technol.* **7** Q26

[10] Balestra F, Ghibaudo G and Jomaah J 2015 *Int. J. Numer. Model.-Electron. Netw. Device Fields* **28** 613

[11] De Oliveira A V, Veloso A, Claeys C, Horiguchi N and Simoen E 2020 *IEEE Electron Dev. Lett.* **41** 317

[12] Kushwaha P, Agarwal H, Lin Y K, Dasgupta A, Kao M Y, Lu Y, Yue Y, Chen X N, Wang J, Sy W, Yang F, Chidambaram P R C, Salahuddin S and Hu C M 2019 *IEEE Electron Dev. Lett.* **40** 985

[13] Ding Y M, Misra D and Srinivasan P 2017 *IEEE Trans. Electron Dev.* **64** 2321

[14] Hung K K, Ko P K, Hu C and Cheng Y C 1990 *IEEE Trans. Electron Dev.* **37** 654

[15] Simoen E and Claeys C L 2016 *Random telegraph signals in semiconductor devices*, Vol. 357 (Bristol: IOP Publishing)

[16] Chen W Y, Cai L L, Li Y, Wang K L, Zhang X, Liu X Y and Du G 2019 *IEEE Trans. Nanotechnol.* **18** 385

[17] Samnakay R, Balandin A A and Srinivasan P 2017 *Solid-State Electron.* **135** 37

[18] Joishi C, Ghosh S, Kothari S, Parihar N, Mukhopadhyay S, Mahapatra S and Lodha S 2018 *IEEE Trans. Electron Dev.* **65** 4245

[19] Yang J, Masuduzzman M, Kang J and Alam M *2011 International Reliability Physics Symposium*, pp. 3A.3.1–3A.3.6

[20] Vandelli L, Larcher L, Veksler D, Padovani A, Bersuker G and Matthews K 2014 *IEEE Trans. Electron Dev.* **61** 2287

[21] Cartier E and Kerber A 2009 *IEEE International Reliability Physics Symposium*, pp. 486–492

[22] Cheng Y H 2019 *IEEE* 32*nd International Conference on Microelectronic Test Structures (ICMTS)*, pp. 126–131

[23] Zhang T 2009 *Electrical Engineering and Computer Sciences*, University of California at Berkeley UCBIEECS-2009-18

[24] De Andrade M G C, Martino J A, Simoen E and Claeys C 2015 *Microelectronic Engineering* **147** 122

[25] Wu W R, Wu H, Sun W F, Si M W, Conrad N, Zhao Y and Ye P D 2018 *IEEE Trans. Electron Dev.* **65** 2573

[26] Xu Y, Li Y, Li S L, Balestra F, Ghibaudo G, Li W W, Lin Y F, Sun H B, Wan J, Wang X R, Guo Y F, Shi Y and Noh Y Y 2019 *Adv. Funct. Mater.* **1904508** 23

[27] Celik Z and Hsiang T Y 1985 *IEEE Trans. Electron Dev.* **32** 2797

[28] Franco J, Kaczer B, Mukhopadhyay S, Duhan P, Weckx P, Roussel P J, Chiarella T, Ragnarsson L Å, Trojman L and Horiguchi N 2016 *IEEE International Electron Devices Meeting (IEDM)*, pp. 15.3.1–15.3.4