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Evaluation of stress voltage on off-state time-dependent breakdown for GaN MIS-HEMT with SiN_x gate dielectric*

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Stress voltages on time-dependent breakdown characteristics of GaN MIS-HEMTs during negative gate bias stress (with $V_{GS} < 0$, $V_D = V_S = 0$) and off-state stress ($V_G < V_{Th}$, $V_{DS} > 0$, $V_S = 0$) are investigated. For negative bias stress, the breakdown time distribution (β) decreases with the increasing negative gate voltage, while β is larger for higher drain voltage at off-state stress. Two humps in the time-dependent gate leakage occurred under both breakdown conditions, which can be ascribed to the dielectric breakdown triggered earlier and followed by the GaN layer breakdown. Combining the electric distribution from simulation and long-term monitoring of electric parameter, the peak electric fields under the gate edges at source and drain sides are confirmed as the main formation locations for per-location paths during negative gate voltage stress and off-state stress, respectively.

Keywords: gallium nitride, LPCVD-SiN_x MIS-HEMT, time-dependent breakdown, negative gate bias, off-state stress

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1. Introduction

GaN-based electronic materials are considered as excellent candidates for power switching applications, owning to their outstanding properties such as high electrical breakdown field and high saturated electron mobility.[1,2] As for AlGaN/GaN metal–insulator–semiconductor high electron mobility transistor (MIS-HEMT), silicon nitride (SiN_x) dielectric deposited by low pressure chemical deposition (LPCVD) technique offers the absence of the Ga–O bonds and a large conduction band offset ($\Delta E_c = 2.3$ eV), yielding an effectively suppressed gate leakage and a large gate swing.[3–5] In addition, the free plasma-induced damage and high deposition temperature (780 °C) provide a high quality dielectric film with low defect density,[6] thus offering excellent thermal stability and large forward breakdown electric field (14 MV/cm).[7] However, long term stability and reliability for GaN MIS-HEMT with LPCVD SiN_x gate dielectric still need extensive evaluation before commercial deployment.

The GaN MIS-HEMT is often adopted in cascode configuration, requiring a negative gate bias to deplete the two-dimensional electron gas (2DEG) channel and sustain the off-state high drain voltage.[8,9] Marcon *et al.*[10] have revealed that the off-state breakdown is time-dependent and even a small voltage stress can trigger hard breakdown after a sufficient time stress. Furthermore, the effects of ultraviolet light and substrate bias on the time-dependent breakdown (TDB) were also evaluated previously.[11,12] Generally, the absolute value of negative gate bias is relatively smaller than that of drain voltage under off-state stress condition. However, both negative gate bias and drain voltage are accelerated factors which will inevitably bring defects inside the gate dielectric and GaN materials, and eventually cause catastrophic failure of devices.[9,10] In the enhance-mode LPCVD-SiN_x/GaN MIS-FET, Hua *et al.*[13] found that the threshold voltage stability shows an obvious dependence on the negative gate bias under reverse-bias step-stress. Until now, researchers have been mainly focusing on electron detrapping process in the gate dielectric induced by moderate negative gate stress with the overdrive voltage ($V_{GS} - V_{Th}$) smaller than -80 V.[14] The negative gate stress condition can be regarded as special off-state stress with a certain large drain to gate voltage (V_{DG}) bias, which is also able to cause breakdown of gate dielec-

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tric or GaN materials. However, there are no reports on comparing time-dependent breakdown between off-state stress and negative bias stress, which is obviously beneficial for further understanding the inherent physical mechanism.

In this paper, rapid breakdown of GaN MIS-HEMT with LPCVD SiN_x gate dielectric under negative gate bias stress ($V_{GS} < 0$ V, $V_{DS} = 0$ V) and off-state stress ($V_G < V_{Th}$, $V_{DS} > 0$) is investigated by using static constant voltage stress (CVS) tests. The substrate and source in both stress cases are grounded ($V_S = V_{Sub} = 0$). The purpose of setting the two type stress conditions is to analyze the influence of V_{GS} and V_{DS} on breakdown process under a fixed drain to gate voltage (V_{DG}) separately. Simulation method is utilized to further analyze the underlying degradation mechanism of the two type stress conditions. After rapid breakdown tests mentioned above, a large drain to gate voltage stress (in this paper, $V_{DG} = 200$ V) sufficient to generate large numbers of defects but not enough to cause rapid breakdown of device is selected to monitor the long-term evolution of electric parameters, which is beneficial for further underlying the inherent mechanism of the two stress conditions.

2. Device details

The devices used in this paper are manufactured on the standard CMOS production line. The metal–organic chemical vapor deposition (MOCVD) GaN epitaxial layer was grown on a 6-inch (111) Si substrate (1 inch = 2.54 cm), from bottom to top is a 4-μm GaN buffer, a 300-nm/25-nm AlGaN/GaN heterojunction and a 2-nm GaN cap. A 0.7-nm AlN interlayer is sandwiched between the AlGaN/GaN heterojunction. The device features a dimension of $L_g/L_{gs}/L_{gd}/W_g$ at 3-μm/3.5-μm/3.5-μm/100-μm. A 35-nm SiN_x was deposited by LPCVD as the the gate dielectric as well as the first passivation layer. More process details are illustrated in our previous works.[15]

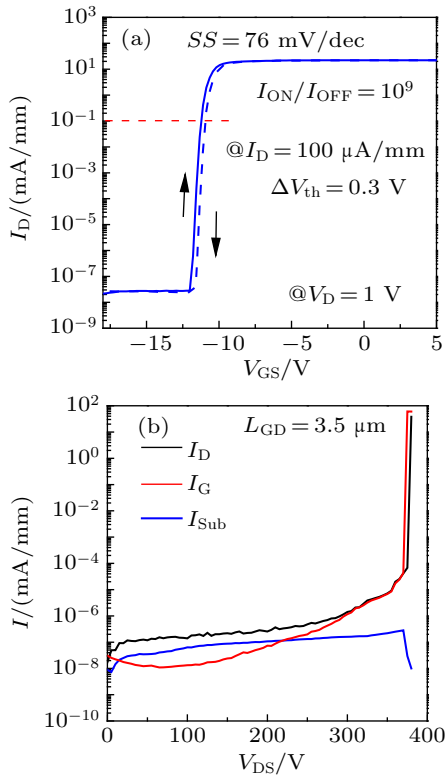


Fig. 1. (a) Transfer and (b) off-state blocking voltage characteristics of the GaN MIS-HEMT.

Figure 1 shows the transfer and off-state breakdown characteristics of devices used in this work. The devices deliver excellent gate control ability with a small subthreshold swing of 87 mV/decade and a high on/off current ratio of 10^9. The threshold voltage (V_{Th}) is approximately −10 V, which is defined at drain current of 10 μA/mm with drain voltage (V_{DS}) of 1 V. The hysteresis of V_{Th} is small at the maximum sweep gate voltage (V_{GS}) of 10 V. The drain to gate breakdown voltage (V_{DG_max}) is 360 V with $V_G = V_{Th} - 5$ V and $V_S = V_{Sub} = 0$. It worth noting that the drain current is mainly determined by the gate leakage current.

3. Results and discussion

3.1. Time-dependent breakdown during negative gate bias and off-state stress

The selection of drain to gate breakdown voltage (V_{DG}) is around 80% of V_{DG_max}, and seven devices per group of breakdown voltage are adopted. The TDB during negative bias stress is shown in Fig. 2(a), time to breakdown (t_{BD}) is defined at the point when I_{GS} exceeds 10^{-2} mA/mm, lifetime extrapolation of absolute V_{GS} for 20 years based on $1/E$ model[7] with failure rate of 63.2% and 0.01% are 209 V and 162 V, respectively (Fig. 2(b)). Therefore, SiN_x dielectric deposited by LPCVD delivering excellent long-term negative bias breakdown property. For off-state stress condition with a fixed drain to source voltage ($V_{DG} = 295$ V, same as the negative bias stress), t_{BD} is approximately 1 order of magnitude shorter for $V_{DS} = 280$ V than that of $V_{DS} = 270$ V (Fig. 3), which is mainly account of the more sever ionizing collision of hot electron effect in gate to drain access region.[16] Furthermore, the comparison between negative gate voltage stress ($V_{GS} = -295$ V, $V_{DS} = 0$ V) and off-state stress ($V_{GS} = -15$ V, $V_{DS} = 280$ V) on time-dependent breakdown indicates that the mean t_{BD} is just 0.5 order of magnitude shorter for off-state stress (Fig. 4(a)). The possible reason of this phenomenon is ascribed to that the external voltage under both bias conditions is sustained by the dielectric and depletion region in GaN layers between gate and drain electrodes. Besides, unlike the forward bias time-dependent breakdown process,[7,17–20] two sudden increasing trend in I_{GS} occurs during both off-state and negative bias stress conditions (Fig. 4(b)). The lower I_{GS} for off-state stress (Fig. 4(a)) reflects the difference of leakage paths between the two stress conditions, the inherent mechanism will be discussed in Subsection 3.2. We previously con-

firm that the forward breakdown voltage of GaN MIS-HEMT with LPCVD SiN_x dielectric used in this paper is 45 V. When the maximum of electric field applied in the dielectric exceeds 11.4 MV/cm, the breakdown will be triggered in dielectric first. Then, most of the voltage is sustained by the GaN epitaxial layer and causes the second breakdown.

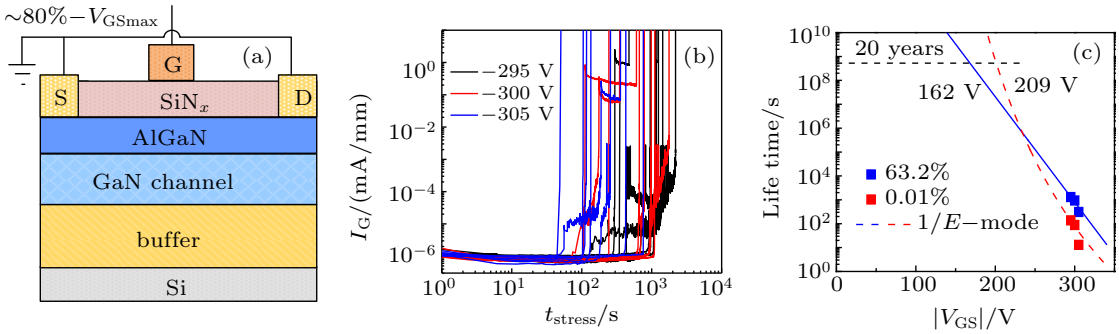


Fig. 2. (a) Test diagrams of negative bias stress and (b) time-dependent breakdown with $V_{GS} = -295$ V, -300 V, -305 V, respectively, and (c) lifetime extrapolation for 20 years based on $1/E$ model with failure rate of 63.2% and 0.01%.

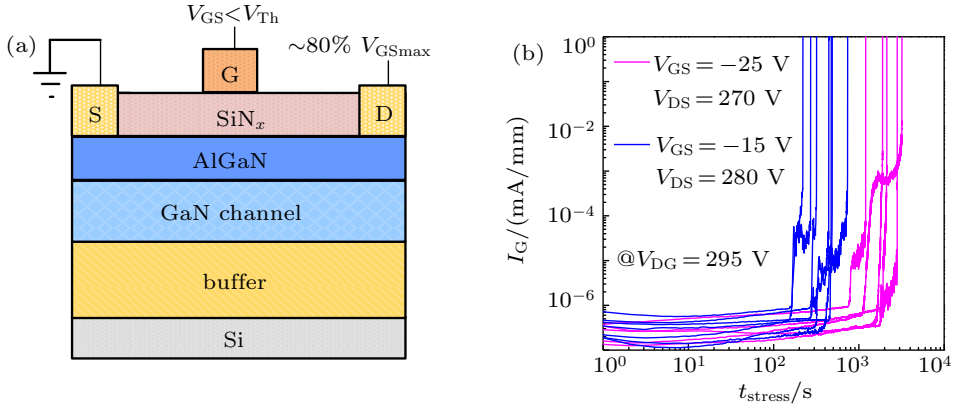


Fig. 3. (a) Test diagrams of off-state stress and (b) time-dependent breakdown during off-state stress with $V_{DS} = 280$ V and $V_{DS} = 270$ V @$V_{DG} = 295$ V.

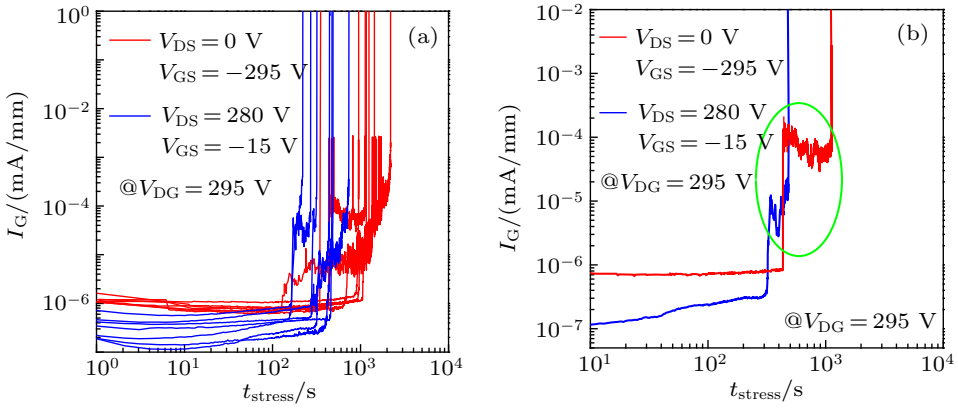


Fig. 4. (a) The comparison of time-dependent breakdown between negative gate voltage stress and off-state stress. (b) Two sudden increasing trends of gate leakage occur during both stress conditions.

The t_{BD} of MIS-HEMT for the two stress conditions both follow a Weibull failure distribution, which can be described as

$$F(t) = 1 - \exp\left[-\left(\frac{t-\gamma}{\eta}\right)\right], \tag{1}$$

where t is the time, β is the shape parameter, η is the scale factor of 63.2% value, is defined as burn-in time or time delay, assuming $\gamma = 0$, equation (1) can be expressed as

$$\ln[-\ln(1-F(t))] = \beta \ln(t) - \beta \ln(\eta) \tag{2}$$

in the semi-log plot of $\ln[-\ln(1-F(t))]$ *versus* t_{BD}, β and $\ln(\eta)$ represent slope and intercept, respectively. The shape parameter β is an indicator of breakdown time distribution, which has strong relationship with the number of new defects needed for the formation of per-location paths along the device width in the material.[11,19] Indeed,

$$\beta = m \times N, \tag{3}$$

where m is the defects generation rate and N represents number of traps needed for the formation of a per-location

paths.[8,21] For negative gate bias stress, β decreases with the increase of negative gate voltage (as shown in Fig. 5(a), $\beta = 4.1$ for $V_{GS} = -295$ V, $\beta = 3.9$ for $V_{GS} = -300$ V and $\beta = 2.1$ for $V_{GS} = -305$ V, respectively). The negative gate bias can fully deplete the 2DEG and GaN layers, then the generation rates of different bias voltages are nearly constant.

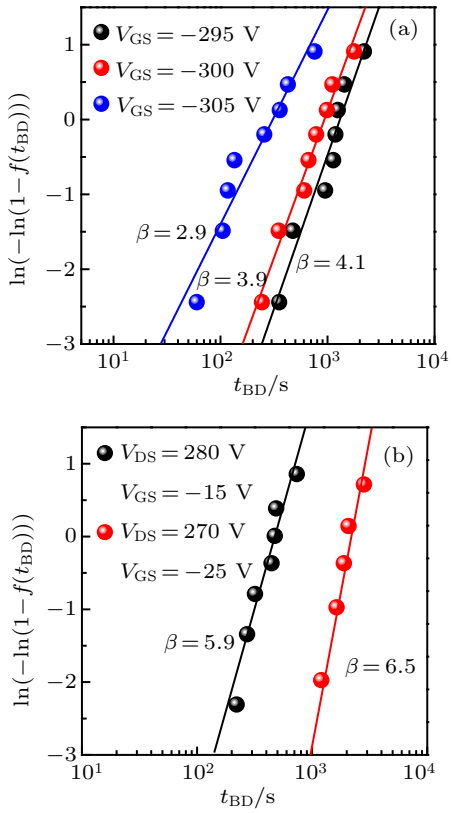


Fig. 5. Breakdown time distribution (β) of (a) negative gate bias with $V_{GS} = -295$ V, -300 V, -305 V, respectively and (b) off-state stress with $V_{DS} = 280$ V and $V_{DS} = 270$ V @$V_{DG} = 295$ V.

However, more electrons will inject into the dielectric and introduce more defects under a higher bias, which means that fewer formed defects are needed for the per-location paths for higher negative gate bias stress. While in the case of off-state stress, β is larger for higher V_{DS} (as shown in Fig. 5(b), $\beta = 5.9$ for $V_{DS} = 280$ V and $\beta = 6.5$ for $V_{DS} = 270$ V @$V_{DG} = 295$ V). The higher V_{DS} will bring more electron from 2DEG channel into the GaN layers, resulting in an increasing defects generation rate and larger β value. Compared to off-state stress, β for negative gate bias stress is definitely smaller which means that the breakdown time is much dispersion. This is in consistence with the first breakdown in dielectric due to the more crowding of electric field around the gate under negative gate bias as reflected in the simulation results below.

3.2. Insight into the breakdown mechanism of the two types of stress conditions

Simulations for rapid breakdown conditions (@$V_{DG} = 295$ V) verify that negative bias stress will induce significant peak electric field under both edges of gate–drain edge and gate–source, and the peak electric field for gate–source is slightly higher than that of gate–drain even for the device with $L_{gs} = L_{gd}$ (Figs. 6(a) and 6(c)), which implies that the formation of per-location paths is most likely to occur under the edge of gate–source. While peak electric field for off-state stress is mainly localized at the edge of gate–drain (Figs. 6(b) and 6(c)). In the whole, the peak electric field of both edges of gate–drain edge and gate–source for negative bias stress are higher than that of the edge of gate–drain for off-state stress (Fig. 6(c)).

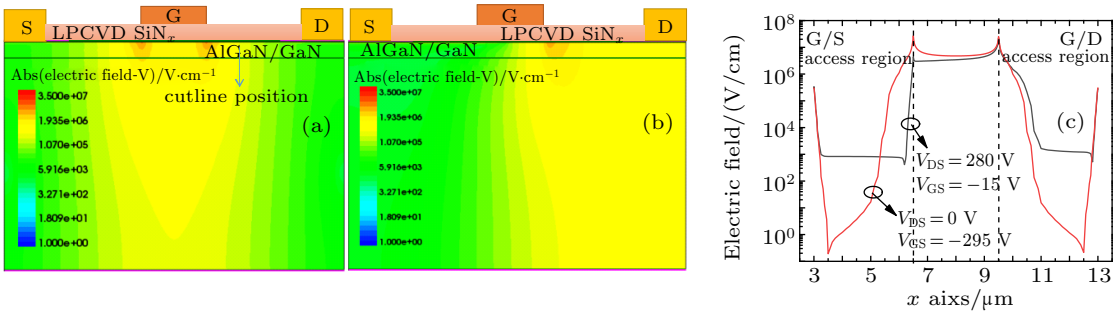


Fig. 6. Simulation of electric field distribution for rapid breakdown under (a) negative bias stress @$V_{DG} = 295$ V and (b) off-state stress @$V_{DG} = 295$ V. (c) Extraction of electric field distribution at the cutline of 10 nm below SiN_x/AlGaN interface for both of the two stress conditions.

For further underlying the time-dependent breakdown mechanism of negative bias and off-state stress for GaN MIS-HEMT with LPCVD SiN_x dielectric, a large drain to gate voltage stress (in this paper, $V_{DG} = 200$ V is adopted) sufficient to generate large numbers of defects but not enough to cause rapid breakdown of device is selected to monitor the long-term evolution of electric parameters.

During negative bias stress ($V_{GS} = -200$ V, $V_{DS} = 0$ V, @$V_{DG} = 200$ V as shown in Fig. 7(a)) process, the threshold voltage shift to the positive ($\Delta V_{Th} = 2.45$ V after stressed for 10000 s), and on-resistance (R_{on}) continues to increase (Fig. 7(b)) in the whole time stress window. Under negative bias, the injection of electron from gate will be trapped by the pre-existing defects in SiN_x dielectric, AlGaN barrier and buffer layers.[14,22] Those electrons will deplete the 2DEG channel and shift the threshold voltage positively. Moreover, the leakage monitoring (Fig. 8(a)) shows that from 100 s to 10000 s, the leakage of gate (I_{GS}) and drain to gate (I_{DG}) in-

crease about 0.3 and 0.5 order of magnitude gradually. Strikingly, the leakage of source to gate (I_{SG}) increases about 1.0 order of magnitude and exceeds I_{DG} gradually, which further indicates that despite the existence of two peak electric under the gate edges of source and drain for the MIS-HEMT with $L_{gs} = L_{gd}$, breakdown for negative bias stress occurs mainly concentrated below the edge of gate–source. After adequate recovery process (after the static storage of 10^6 s and then illuminated under ultraviolet light for 10^4 s), significant negative shift of V_{th} ($\Delta V_{Th} = -2.2$ V as shown in Figs. 7(c) and 10(a)) and about 0.5 order of magnitude (Fig. 8(a)) increasing of I_{GS} underlying that the newly generated defects occurs in the SiN_x and SiN_x/AlGaN interfaces. Besides, the negligible degradation of on-resistance (R_{on}) after adequate recovery process (Fig. 7(f)) reflects the fact that the newly generation of defects are mainly located at the gate edges of source and drain. Therefore, combined with simulation results as Figs. 6(b) and 6(c), the formation of per-location paths will be first formed in SiN_x dielectric and then in AlGaN barrier below the edge of gate–source (as shown in Figs. 9(a)–9(c)).

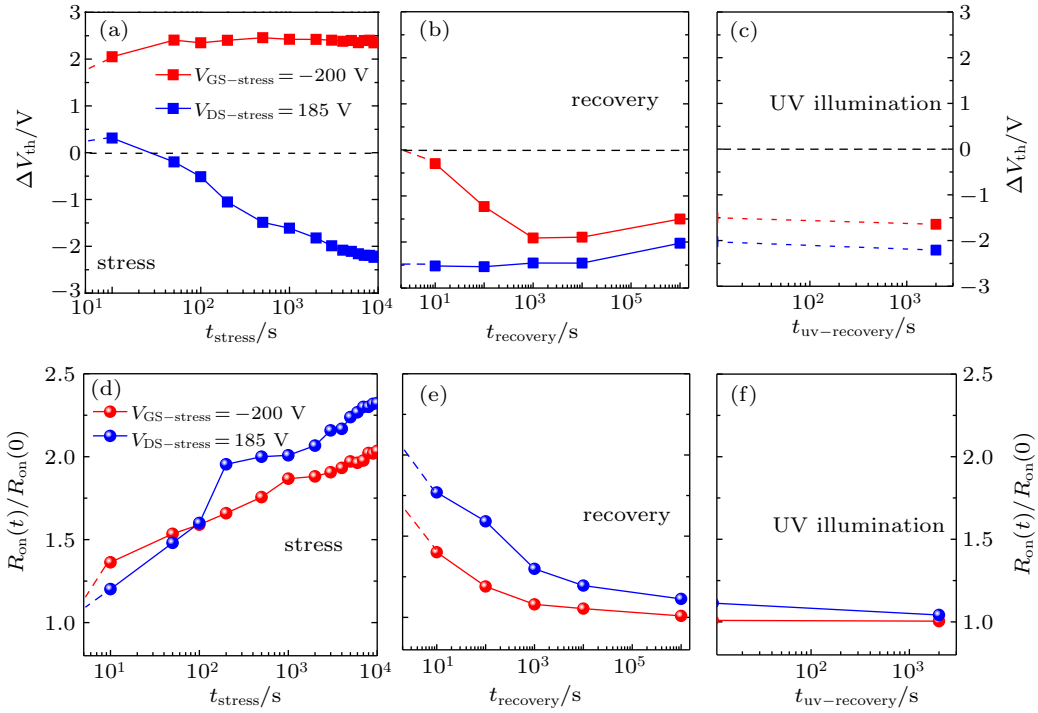


Fig. 7. The evolution of threshold voltage and on resistance during stress and recovery conditions of $V_{GS} = -200$ V, $V_{DS} = 0$ V, and $V_{GS} = -15$ V, $V_{DS} = 185$ V @$V_{DG} = 200$ V.

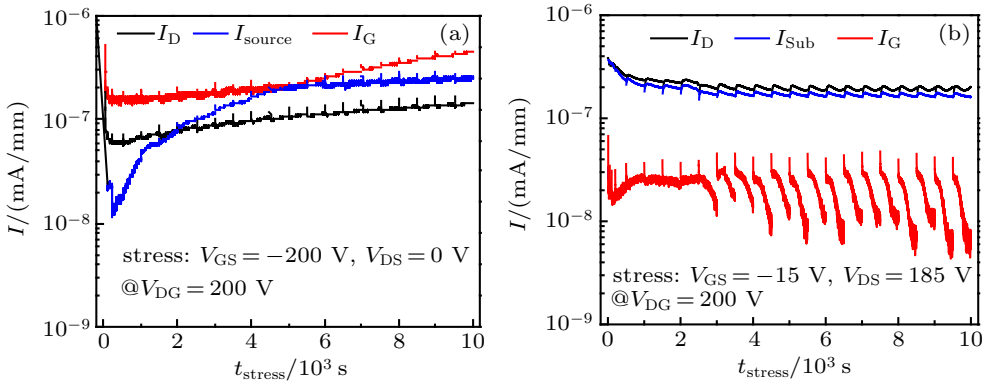


Fig. 8. The evolution of leakage during (a) negative gate bias at $V_{GS} = -200$ V, $V_{DS} = 0$ V @$V_{DG} = 295$ V and (b) off-state stress at $V_{GS} = -15$ V, $V_{DS} = 185$ V @$V_{DG} = 200$ V.

While the negative shift of V_{th} ($\Delta V_{Th} = -2.35$ V after stressed for 10^4 s as shown in Fig. 7(a)) for off-state stress ($V_{GS} = -15$ V, $V_{DS} = 185$ V, @$V_{DG} = 200$ V) is mainly on account of the gradually generation of new defects of dielectric, more inherent mechanisms are related to gate to source leakage (I_{GS}) as shown in Fig. 8(b), the correlation analysis will be given below. The continued increase of R_{on} (Fig. 7(b)) during time stress reflects the trapping process in gate to drain access region. Similarly to negative bias stress, after adequate recovery process, the exhibited negative shift of V_{th} ($\Delta V_{Th} = -1.85$ V for off-state stress as shown in Figs. 7(f) and 10(b)) and about 0.5 orders of magnitude (Fig. 10(b)) increas-

ing of I_{GS}underlying that new defects were initially generated in the SiN_x dielectric. In addition, the negligible change of on-resistance (R_{on}) after adequate recovery process (Fig. 7(f)) reflects the fact that the newly generations of defects are mainly located under the edge of gate to drain (as shown in Figs. 9(e)–9(g)).

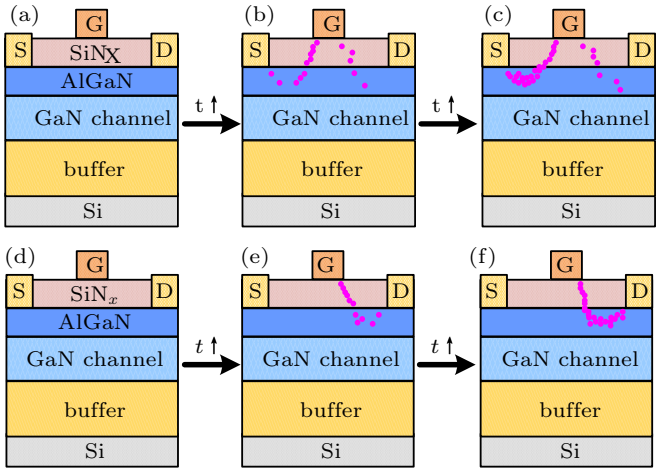


Fig. 9. The schematic mechanism for the negative bias stress (a)–(c) and off-state time-dependent breakdown process (e)–(g).

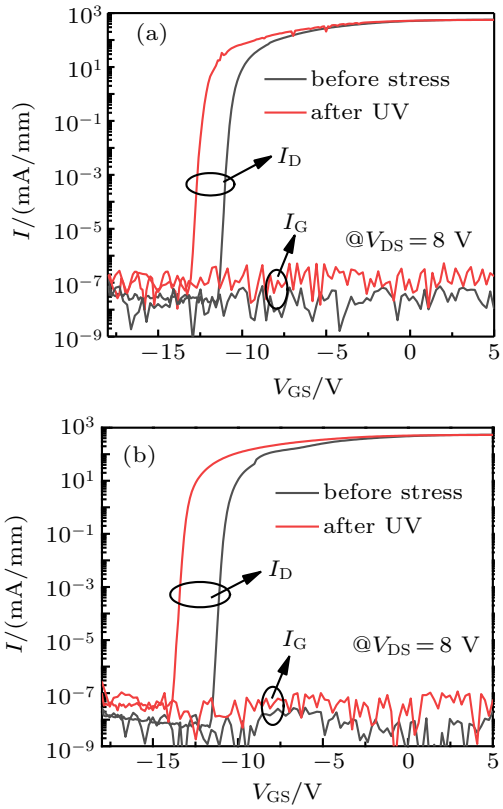


Fig. 10. Transfer characteristics and I_{GS} before stress and after adequate recovery of (a) negative bias stress at $V_{GS} = -200$ V, $V_{DS} = 0$ V @$V_{DG} =$ 200 V and (b) off-state stress at $V_{GS} = -15$ V, $V_{DS} = 185$ V @$V_{DG} = 200$ V.

During off-state stress period of 10^4 s (Fig. 8(b)), the drain leakage current is dominated by drain to substrate current (I_{Sub}), while the change of I_{Sub} during the whole stress period is negligible. When the stress time exceeds 2500 seconds, I_{DG} gradually decreases during each stress period from beginning to the end, which is attributed to electrons trapped by the localized defects inhibiting the trapping process. Then I_{GS} recovers to the initial value at the beginning of next stress period by the reason of electron–electron de-trapping. Moreover, I_{GS} is smaller than the previous one after each stress period, which is apparently account of the newly generated defects in SiN_x dielectric capturing more electrons and further inhibiting the trapping process.

4. Conclusion

In conclusion, the evaluations of stress voltage on the time-dependent breakdown characteristics for GaN MIS-HEMT with LPCVD SiN_x gate dielectric are investigated by combining experiment and simulation. SiN_x dielectric deliveres excellent long-term negative bias breakdown property. The lifetime extrapolation for 20 years based on $1/E$ model with failure rate of 63.2% and 0.01% are 209 V and 162 V, respectively. Furthermore, the time-dependent breakdown was investigated under both negative gate bias and off-state stress. For negative bias stress, the breakdown time distribution (β) decreases with the increase of negative gate voltage, because more electrons will inject into the dielectric and introduce more defects under a higher bias, thus fewer formed defects are needed for the per-location paths for higher negative gate bias stress. While β is larger at higher drain voltage for off-state stress, which means that higher V_{DS} will bring more electrons from 2DEG channel into the GaN layers, resulting in an increasing defects generation rate and larger β value. Two humps in the time-dependent gate leakage occurred during both breakdown conditions, which can be ascribed to the different newly generated leakage paths at different locations. Combining experiment and simulation results, the catastrophic breakdown of SiN_x dielectric will be triggered first, and then the GaN layer breakdown will occur subsequently. The peak electric field under the gate edges of source and drain is confirmed as main locations for the breakdown of negative gate voltage stress and off-state stress, respectively.

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