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Optimization of terahertz monolithic integrated frequency multiplier based on trap-assisted physics model of THz Schottky barrier varactor

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The optimization of high power terahertz monolithic integrated circuit (TMIC) is systemically studied based on the physical model of the Schottky barrier varactor (SBV) with interface defects and tunneling effect. An ultra-thin dielectric layer is added to describe the extra tunneling effect and the damping of thermionic emission current induced by the interface defects. Power consumption of the dielectric layer results in the decrease of capacitance modulation ration ($C_{\max}/C_{\min}$), and thus leads to poor nonlinear *C*–*V* characteristics. The proposed Schottky metal-brim (SMB) terminal structure could improve the capacitance modulation ration by reducing the influence of the interface charge and eliminating the fringing capacitance effect. Finally, a 215 GHz tripler TMIC is fabricated based on the SMB terminal structure. The output power is above 5 mW at 210–218 GHz and the maximum could exceed 10 mW at 216 GHz, which could be widely used in terahertz imaging, radiometers, and so on. This paper also provides theoretical support for the SMB structure to optimize the TMIC performance.

Keywords: *C*–*V* characteristic, physics-based model, terahertz monolithic integrated circuit (TMIC), Schottky barrier varactor

PACS: 42.65.Ky, 73.61.Ey, 85.30.De, 85.30.Kk **DOI:** 10.1088/1674-1056/abab74

1. Introduction

In recent decades, terahertz science has developed rapidly, and this has promoted the use of THz radiation in many high requirement fields, such as astrophysics and earth science, safety imaging, and communication.[1–5] A local-oscillator (LO) signal source with sufficient output power is the core technology in THz systems. Frequency multipliers based on the Schottky barrier varactor (SBV) have been commonly employed due to their advantages of good functionality at room temperature, lower mass, and easy to design.[6–8] A precise description of the experimental nonlinear behavior of SBV is necessary for the application of high power and high efficiency multipliers, which can tremendously influence the design and optimization of the frequency multiplier circuits.[9]

According to the semiconductor physical theory, a Schottky barrier diode can be modeled as a nonlinear junction voltage-dependent current source, which is generated by the variation of depletion layer and thermal electron emission. So, the most important parameter for optimizing the performance of high-power and high-efficiency frequency multipliers is the nonlinearity of the *C*–*V* characteristic and the *I*–*V* characteristic of the diodes.[10,11] The total series resistance and *I*–*V* curve have already been correctly studied.[12,13] In recent research, Diego *et al.* proposed a physics-based capacitance–voltage model by using a two-dimensional (2-D) ensemble Monte–Carlo simulator to analyze the edge capacitance characteristics of sub-micrometer anode diodes.[14] Ren *et al.* provided a compact model for describing the non-linear *C*–*V* characteristics of the Schottky barrier diode worked in the terahertz band.[15] Compared with the classical *C*–*V* model used in circuit design automation software, the terahertz *C*–*V* characteristic could optimize the design of frequency multipliers by modifying the *C*–*V* curve function at low forward bias. When enhancing input power and reducing the size of the varactor for increasing the operating frequency, the emergence of non-ideal *C*–*V* phenomena induced by interface defects of Schottky junction and extra tunneling current can affect the accuracy of the models used in the multipliers design process and thus reduce the final performance of the multipliers. However, the degradation of frequency multiplier induced by interface defects and tunneling effect has not been reported.

In this paper, the main task is to analyze the rigorous modeling of non-linear *C*–*V* characteristics based on the physical SBV model with interface defects and tunneling effect and thus optimize the performance of high power terahertz monolithic integrated circuit (TMIC) with a proposed Schottky metal-brim (SMB) terminal structure. The SBVs with different terminal structures are fabricated. Through combining

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the measurement and simulation results of SBV to obtain the best fitting of *I*–*V* and *C*–*V* characteristics, the key model parameters (i.e., interfacial layer, interface state density, and capacitance ideal coefficient) are presented, and a simple *C*–*V* model is used for harmonic balance simulation. Finally, a 215 GHz tripler TMIC with the SMB structure is fabricated to evaluate the modified *C*–*V* model based on interface defects and tunneling effect.

2. Experiment

The proposed SBV with different terminal structure is illustrated in Fig. 1. Based on our previous studies,[16] the SMB structure which has the advantages of reducing leakage current and eliminating edge capacitance effect is designed to enhance the power handling capability and conversion efficiency in multiplier applications. The varactors are fabricated on n-type GaAs epitaxial wafers, containing a 1.5 μm-thick buffer layer with a Si doping concentration of 5×10^{18} cm^{-3}, and a 0.3 μm-thick epi-layer with a doping concentration of 2×10^{17} cm^{-3}. A monolithically integrated Schottky diode process is adopted for the production of devices. Forward and reverse breakdown *I*–*V* measurements are performed using Agilent 4200 semiconductor device parameter analyzer at room temperature. The *S*-parameters are measured by Agilent E8363B network analyzer with ground-signal-ground RF probes to extract the junction capacitance. The test frequency range is 0.1–40 GHz.

3. Device modeling

3.1. Description of the simulation process

A series of physical effects could affect the behavior of real Schottky diodes, which include interfacial disorder, interface state densities, and extra tunneling effect.[17,18] To further explore the influence of this issue on *C*–*V* characteristics, a deeper understanding of the carrier transport mechanism is required. Therefore, we simulated the diode characteristics with the TCAD simulation tools, where a drift-diffusion equation set coupled with the Poisson equation is solved. For its realization, the structure size, contacts, and doping concentration consistent with the actual ones are specified. The structure is shown in Figs. 1(b) and 1(c). A good mesh distribution is required to evaluate the electrical behavior and the distribution of physical parameters, such as electrostatic potential, current and charge densities, and so on, which is as important as physics model specification.[19] So, the depleted region subjected to abruptly electric potential changes should be covered by a thin mesh.

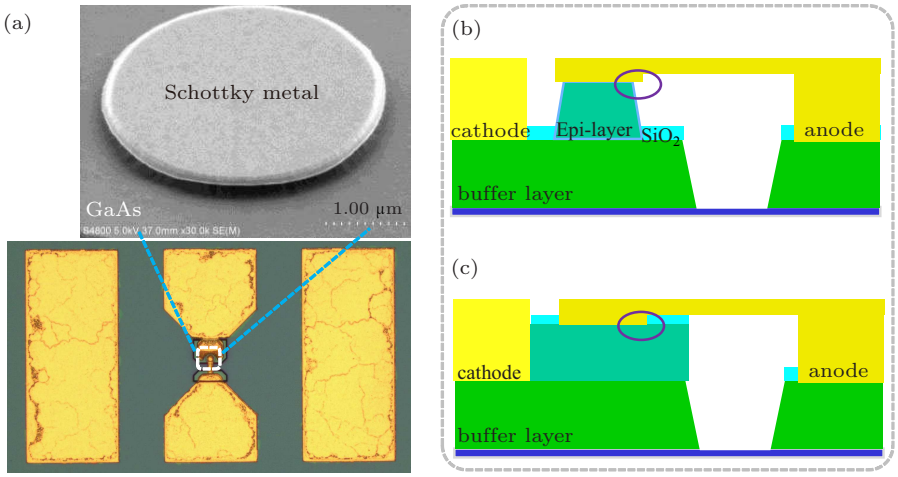


Fig. 1. (a) Optical microscopy image of a fabricated SBV. The SEM photographs of Schottky metal-brim structure details are added. (b) SBV with Schottky metal-brim. (c) Conventional SBV.

In addition to the basic model which contains mobility with doping dependence and high velocity saturation model, the carrier recombination, nonlocal tunneling, metal-induced gap states, dangling bond at the metal/epilayer interface, and traps in the bulk are considered to explain the damping of the thermionic emission current and the high ideality factor.[20] Metal-induced gap states could be described by the wave functions of the metal electrons tail into the semiconductor in the energy range, and induce the fracture of chemical bond due to charge transfer at the metal–semiconductor contacts. Metal-induced gap states and dangling bond which could change the distribution of the built-in electric field are treated as an ultrathin dielectric layer in our simulations, and the dielectric constant is 4.0.[21] Therefore, the hypothetical dielectric-layer between the Schottky contact and epi-layer and acceptor defects at the interface are added. The width of the space charge region is thus slightly adjusted.

3.2. Model parameters extraction

The quasi metal–interfacial layer–semiconductor (MIS) energy band diagram shown in Fig. 2 is used to solve the interface state density and the dielectric-layer thickness.

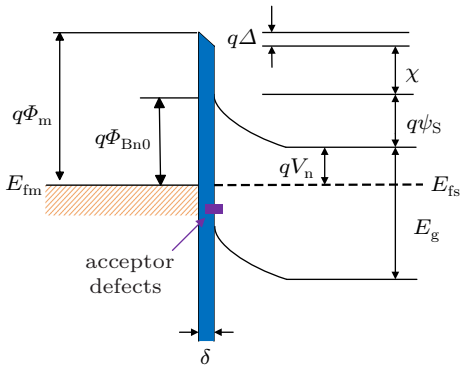


Fig. 2. Energy band diagram of MIS structure.

In Fig. 2, Δ is the potential drop across the dielectric-layer, λ is the electron affinity, $\psi_S(V)$ is the surface potential, V_n is the potential difference between the Fermi level and the conduction band level in the neutral region, E_{fs} is the Fermi level of the semiconductor, E_{fm} is the metal Fermi level, E_g is the band gap, Φ_{B0} is the Schottky barrier height, $q\Phi_m$ is the metal work function, and δ is the thickness of the dielectric-layer.[22,23]

By Gauss theorem, the equation of the electric potential and surface charge of the interface layer is obtained as

$$\Delta = -\frac{\delta Q_m}{\varepsilon_i}, \tag{1}$$

where ε_i is the electrical permittivity of the dielectric-layer, and Q_m is the charge density on the metal side. From the MIS energy band diagram, we obtain

$$q\Phi_m = q\Delta + \chi + q\Phi_{B0}, \tag{2}$$

$$q\Phi_{B0} = q\psi_S(V) + qV_n - qV. \tag{3}$$

The electric potential of the dielectric-layer is obtained from Eqs. (2) and (3) as

$$\Delta = \Phi_m - \frac{\chi}{q} - \psi_S(V) - V_n + V. \tag{4}$$

From the conservation of charge, we have

$$Q_m = Q_{sc}(V) + Q_{it}, \tag{5}$$

where q is the electron charge, $Q_{sc}(V)$ is the space charge density in the depletion layer, and Q_{it} is the interface state charge density at the interface of the semiconductor and dielectric layer. Based on the surface potential theory, the interface states are given by

$$Q_{it} = -qD_{it}\left(E_g - q\varphi_0 - q\psi_S(V) - qV_n\right), \tag{6}$$

where φ_0 is the neutral energy level of interface states. Under thermal equilibrium, the space charge density is given by

$$Q_{sc}(V) = qN_D W_D$$

$$= \sqrt{2q\varepsilon_s N_D\left(\Phi_{B0} - \varphi_n - \frac{kT}{q}\right)}$$

$$= \sqrt{2q\varepsilon_s N_D\left(\psi_S(V) - V - \frac{kT}{q}\right)}, \tag{7}$$

where N_D is the concentration of ionized donors, W_d is the depletion width, ε_s is the electrical permittivity of the semiconductor, k is the Boltzmann constant, and T is the temperature. From Eqs. (4)–(7), we find

$$\frac{\delta\left(Q_{sc}(V) + Q_{it}\right)}{\varepsilon_i} = \Phi_m - \frac{\chi}{q} - \psi_S(V) - V_n + V. \tag{8}$$

For the ultrathick MIS structure, the ideal factor $n(V)$ can be expressed as

$$n(V) = \frac{\varepsilon_i + q\delta D_{it}(V)}{\varepsilon_i}, \tag{9}$$

where $D_{it}(V)$ is the density of the acceptor interface states. From Eqs. (8) and (9), the interface state density and the dielectric-layer thickness can be obtained.

3.3. The *C*–*V* model

The physical model has been validated with measurements for a large number of varactors in different terminal structures (SMB and conventional structure) and with different Schottky diameters (3 μm and 5 μm). The simulated data and measured forward *I*–*V* characteristic are shown in Fig. 3(a) and they are in good agreement, while the ideal model (i.e., SBV model without dielectric-layer) could not accurately describe the degradation of the ideal factors. In Fig. 3(b), the simulated reverse breakdown characteristics of conventional SBV fit well with the measured data, while the simulated results of SMB structure are larger than the measurement results, which is because larger roughness of the side-wall caused by the wet etching process of forming SMB terminal structure increases the leakage current and reduces the breakdown voltage.

It implies that the analysis of the physics model is rational and the extracted parameters are shown in Table 1. Generally, the typical *C*–*V* model is used for the harmonic balance (HB) simulation, which is described as

$$C = C_{j0} \times \sqrt{\left(1 - \frac{V}{V_j}\right)}, \quad (V < f \cdot V_j), \tag{10}$$

where C_{j0} is the zero-bias junction capacitance, V_j is the Schottky junction potential, and f is the forward-bias depletion capacitance coefficient.[24] It describes the behavior of an ideal diode, and is no longer suitable when the leakage current increases. Next, a simple analytical model for the *C*–*V* dependence is proposed based on the physics-based model, accounting for the influence of interface defects and tunneling effect.

Table 1. Key parameters of the modified model.

Parameter	Value
Dielectric-layer thickness δ/nm	0.256
Interface acceptor density D_{it}/cm^2·eV	2.7×10^{12}
Dielectric constant[21]	4.0
Capacitance ideal coefficient η	0.7
Correction term D_1	0.36

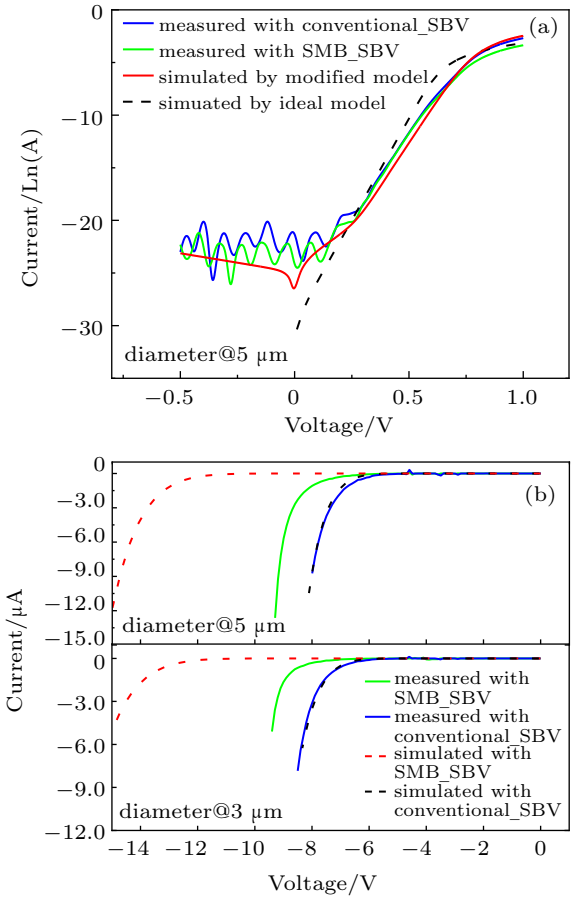


Fig. 3. (a) Forward *I*–*V* characteristics with different structures in log scale (similar with diameter @3 μm). (b) Reverse breakdown characteristics with different structures.

Figure 4 shows the *C*–*V* characteristic of the SMB-SBV obtained by different models, as well as the measured curve extracted by *S*-parameters. Obviously, the simulated results with trap-assisted physics model fit well with the measured one at the reverse bias stage. Compared with the physics model based on ideal Schottky contact, the *C*–*V* simulated by the trap-assisted model has a lower capacitance modulation ration (C_{max}/C_{min}). This is because the ultrathin dielectric-layer will produce a slightly potential drop, and thus effective input power provided to the multiplier would be reduced. On the other hand, the increased electron tunneling probability at the interface caused by defects leads to additional leakage of the input power.

Combining with the open report of interface state capacitance in Refs. [14,25], we can straightforwardly extend our analysis to the behavior of tunneling effect in the SBV capacitance, and then provide a simple analytical expression to describe the capacitive behavior of the actual varactor with conventional terminal structure, as follows:

$$C=\frac{A\varepsilon_s}{\sqrt{\dfrac{2\varepsilon_s(V_j-\eta\cdot V)}{qN_D}}}+2D_1\varepsilon_i L\beta(\Delta), \tag{11}$$

where η is the capacitance ideal coefficient, D_1 is the correction term, $\beta(\Delta)$ is the surface potential capacitance, and L is the diameter of the Schottky junction. In Eq. (11), the first term is the result of actual intrinsic capacitance associated with power consumption caused by the tunneling effect. The second term is the fringing capacitance which is dependent on the surface potential. When the interface defect effect is considered, the effective barrier height of the depletion layer is slightly lower than the theoretical value, which is also verified in the *S*-parameter measurement, and thus leads to a larger zero bias junction capacitance.

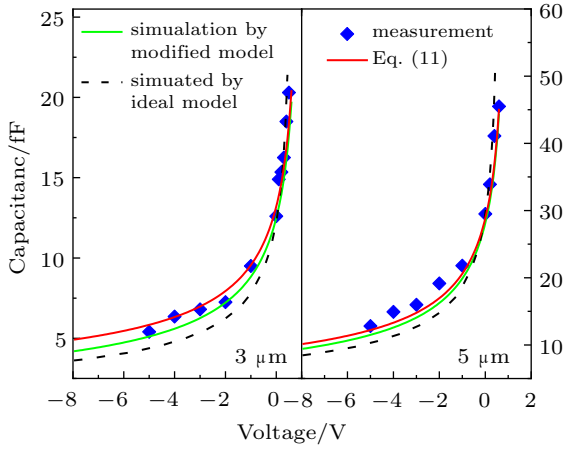


Fig. 4. Comparison of the measured *C*–*V* curves of the SMB-SBV structure and simulated curves based on different models.

The proposed SMB terminal structure could eliminate the fringing capacitance effect and thus reduce the influence of interface defects, which is beneficial for high efficiency multiplier applications. So, the *C*–*V* model of the actual varactor with SMB structure is described as

$$C=\frac{A\varepsilon_s}{\sqrt{\dfrac{2\varepsilon_s\left(V_j-\eta\cdot V\right)}{qN_D}}}. \tag{12}$$

Table 1 shows the common parameters of the trap-assisted physical model. Equation (11), which is plotted in Fig. 4, accurately describes the obtained results, and can be readily included in commercial nonlinear HB simulators by symbolically-defined device (SDD) components.[26]

4. Multiplier performance

In order to evaluate the modified *C*–*V* curves, a 215 GHz unbalanced tripler based on the SMB terminal structure SBV with 5 μm diameter was also designed and fabricated by a monolithically integrated Schottky diode process.

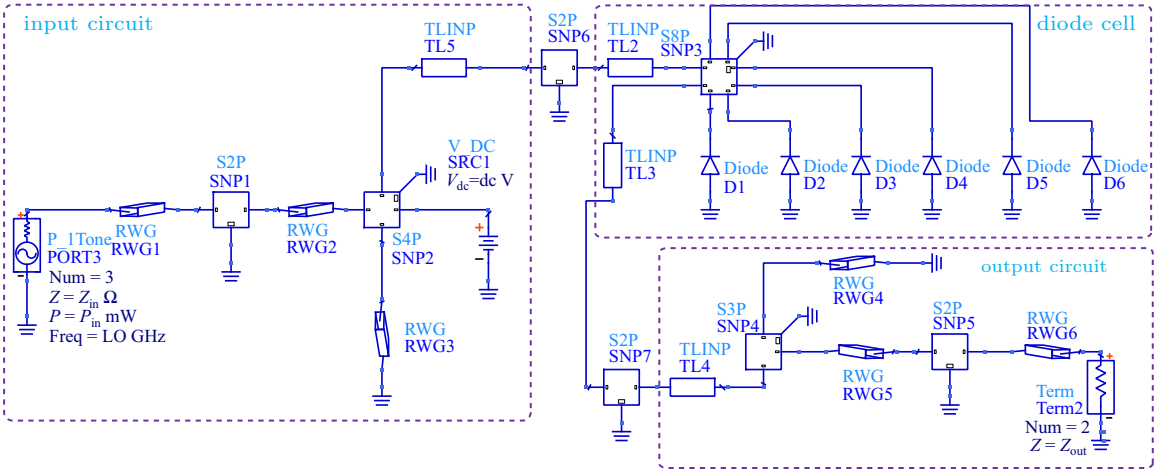


Fig. 5. Equivalent circuit of the 215 GHz TMIC tripler.

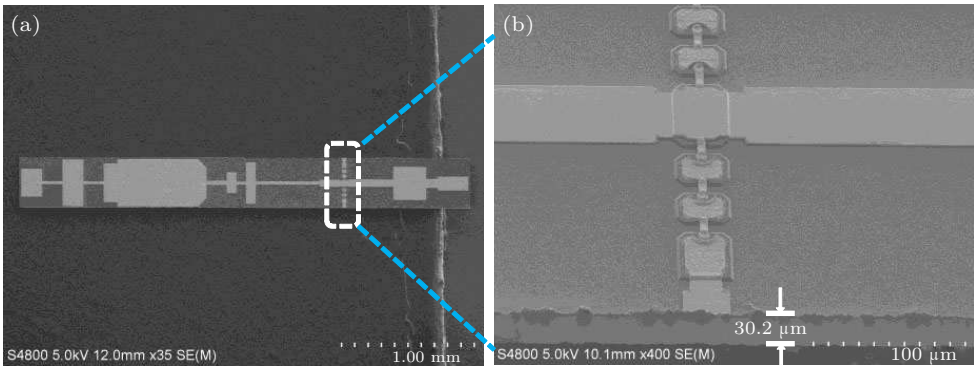


Fig. 6. (a) SEM image of a fabricated tripler TMIC chip. (b) SEM image of a pair of varactors in parallel.

The fabrication process began with a wet etching process to form mesa isolation. Schottky and ohmic metals were deposited by electron-beam evaporation. The SMB structure was then formed by specified etching and a planarization process. Then, samples were passivated with 300 nm-thick SiO_2 by plasma enhanced chemical vapor deposition (PECVD) and the dielectric layer existing on top of the metal contacts was removed by SF_6 plasma dry etching. Next, a 1.5 µm-thick gold layer was electroplated to form air bridge fingers and microstrip circuit. Finally, the GaAs substrate was thinned to 30 µm by lapping and polishing, and the TMIC chips were separated using a laser wafer scriber.

The equivalent linear and nonlinear models of the tripler TMIC are shown in Fig. 5. The passive part of the tripler is divided into three parts, i.e., the input circuit, the output circuit, and the diode cell. The input circuit includes a low pass DC bias filter and a fundamental frequency low pass filter. The out circuit and the input circuit both include waveguide-microstrip transition and matching circuit.

Figures 6(a) and 6(b) show the SEM image of the overall tripler TMIC and the details of the unbalanced structure with a pair of varactors in parallel, respectively.

The block diagram of the measurement setup is illustrated in Fig. 7. An Agilent analog signal generator E8257D (Santa Clara, CA, USA) was followed by the W-band power source which includes a sextupler and an amplifier to generate the signal in the 67–77 GHz band with a power exceed 300 mW. The sextupler employed commercially available GaAs chip fabricated by UMS company, and the power amplifier used the MMIC chip, fabricated by Hittite microwave corporation. An attenuator was added between the source and the tripler to control the input power. The output power of the frequency multipliers was measured by a PM4 power meter (Charlottesville, VA, USA). Moreover, a reverse direct voltage connected the SMA port so as to bias the varactor in tripler TMIC.

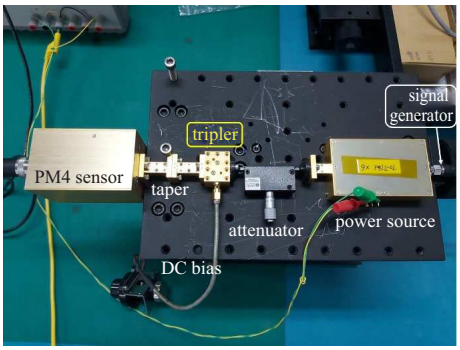


Fig. 7. Photo of test-site about 215 GHz tripler TMIC.

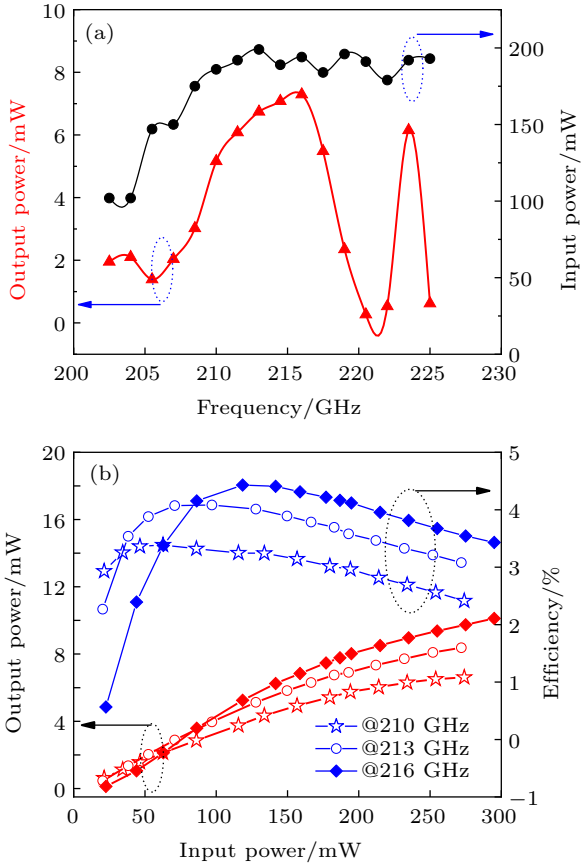


Fig. 8. (a) Measured input and output power as a function of frequency. (b) Measured output power and efficiency as a function of input power at different frequency.

Figure 8(a) shows the measured output and input power of the 215 GHz tripler at the external reverse bias of 6.5 V. It is obvious that the output power is more than 5 mW in 210–218 GHz. Based on our previous study, the tripler can achieve excellent power handling capabilities. The output power changing with the increase of the input power is plotted in Fig. 8(b) and the maximum output power is higher than 10 mW at 216 GHz. To the author's knowledge, the development of frequency multiplier TMICs based on Schottky-diode has been rarely reported in China.

Table 2 illustrates a simple comparison of some reported frequency multiplier MMICs. It can be found that the SMB terminal structure-based tripler presented in this paper has larger power handling capability. The comparison between the simulated efficiencies of this tripler using different *C–V* models and the measured efficiency is shown in Fig. 9. The simulated result using the modified model has better agreement with the measured data. This is because the decrease of capacitance modulation ration (C_{max}/C_{min}) caused by interface defects and tunneling effect is considered in the modified model. It illustrates that the modified *C–V* characteristics are rational and necessary during the optimization of the multiplier TMIC.

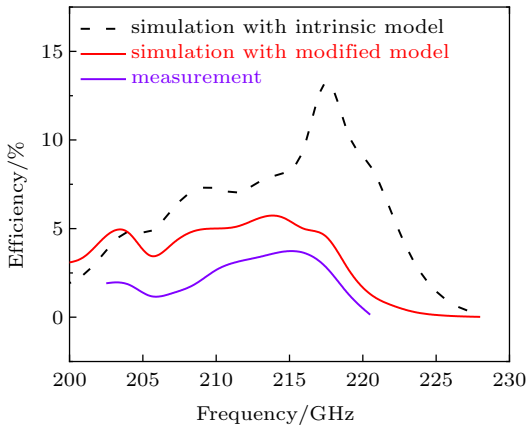


Fig. 9. Comparison of the measured efficiency and simulated curves based on different physics-based *C–V* models.

Table 2. Performance comparison of the frequency multipliers based on TMIC.

References	Technology	Frequency/GHz	Max output power/mW	Efficiency
UESTC[27]	Tripler TMIC	330–500	0.19	2%(max)
ICET[28]	Membrane tripler TMIC	430	0.215	4.3%(max)
VDI[29]	Tripler TMIC	140–220	–	3%(typical)
CETC[30]	Tripler TMIC	325–500	0.45	4.4%(max)
This paper	SMB-structure tripler TMIC	215	10.2	4.5%(max)

5. Summary

An analytical physics-based model for non-linear *C–V* characteristics of the THz SBV has been studied, accounting for the influence of interface defects and tunneling effect. Combined with the analysis by means of TCAD simulations, extra tunneling effect caused by interface defects could reduce the capacitance modulation ration under reverse bias. This is because interface defects and tunneling effect reduce the utilization of input power, which shows poor nonlinear *C–V* characteristics. In addition, the capacitance edge effect which is determined by interface defects could also influence the conversion efficiency of nonlinear capacitance in frequency multiplier applications. The SMB terminal structure is used to eliminate the fringing capacitance effect and reduce the influence of the interface charge. Finally, a 215 GHz tripler TMIC with the SMB terminal structure has been fabricated, and the maximum output power is higher than 10 mW at 216 GHz. The modified *C–V* model could reasonably explain why the SMB terminal structure can realize the optimization of high power TMIC.

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