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Temperature-switching logic in MoS_2 single transistors*

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Due to their unique characteristics, two-dimensional (2D) materials have drawn great attention as promising candidates for the next generation of integrated circuits, which generate a calculation unit with a new working mechanism, called a logic transistor. To figure out the application prospects of logic transistors, exploring the temperature dependence of logic characteristics is important. In this work, we explore the temperature effect on the electrical characteristic of a logic transistor, finding that changes in temperature cause transformation in the calculation: logical output converts from 'AND' at 10 K to 'OR' at 250 K. The transformation phenomenon of temperature regulation in logical output is caused by energy band which decreases with increasing temperature. In the experiment, the indirect band gap of MoS_2 shows an obvious decrease from 1.581 eV to 1.535 eV as the temperature increases from 10 K to 250 K. The change of threshold voltage with temperature is consistent with the energy band, which confirms the theoretical analysis. Therefore, as a promising material for future integrated circuits, the demonstrated characteristic of 2D transistors suggests possible application for future functional devices.

Keywords: molybdenum disulfide (MoS_2), logic, temperature dependence, mobility

PACS: 72.20.Pa, 81.05.Zx, 81.07.−b **DOI:** 10.1088/1674-1056/aba9cf

1. Introduction

The successful exfoliation of monolayer graphene[1] initiated large-scale studies of two-dimensional (2D) materials, which have no dangling bonds, atomic thickness,[2] and van der Waals interactions.[3] To extend Moore's law, 2D materials with these characteristics have been applied to a variety of applications in integrated circuits, such as logic gates,[4] memories,[5] and central processing units.[6] However, these applications generally rely on traditional CMOS-based structures and follow the development methods of silicon-based circuits, which cannot take full advantage of the natural properties of 2D materials. Recently, a work innovatively constructed a 2D logic transistor with a new working principle,[7] implementing logic calculation in one single transistor, which saves 50% area in one unit. The logic gate of the traditional structure requires at least two transistors to realize the same logic calculation. This new working mechanism transistor not only shows a promising solution for future 2D electronic devices and circuit architectures, but also increases 2D integrated circuit density. For further application of this 2D logic transistor, further research is required on logical function modulated by multiple physical fields, especially the working temperature.

In this work, a full 2D logic transistor with a sandwich structure (h-BN/MoS_2/h-BN) is fabricated and its logic output at various environmental temperatures is measured. As the temperature changes, the logic output of the transistor switches between two output functions ('AND' and 'OR'), which means 2D logic transistors have application potential in extreme environments. This temperature switchable phenomenon is attributed to the modulation of temperature to energy band, specifically to mobility and threshold voltage. To confirm this explanation, detailed experimental data and theoretical calculations are provided.

2. Experiment

To study the temperature dependent characteristic of a MoS_2 logic transistor, a device was fabricated on an Al_2O_3 substrate, and measured by cryogenic probe station with a temperature range of 7 K to 250 K. Firstly, multilayer MoS_2 and h-BN were exfoliated with tapes on a sacrificial layer. Then, wet transfer method was used to stack the sandwich structure layer by layer. Next, electron beam lithography was applied to define the location of electrodes, especially the full alignment of the bottom and top gates, in case of non-overlapping region appearance. Finally, a 5 nm Cr (adhesion layer) and a 30 nm Au (metal) layer were deposited as electrodes by electron beam

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evaporator. The temperature dependence of the electrical characteristic was measured in a vacuum, while fabrication processes were realized in the normal atmosphere. The thickness of h-BN was confirmed by atomic force microscope (Fig. A1): top dielectric was 6 nm; bottom dielectric was 8 nm; thickness of channel material MoS_2 was around 5–6 nm; channel width and length were 3 μm and 8.5 μm, respectively.

3. Results and discussion

Figure 1(a) presents a three-dimensional schematic structure of the MoS_2 logic transistor: MoS_2 is the channel layer, connecting with the drain and source electrodes; h-BN is the dielectric layer, blocking the connection between the gate and channel; the gates serve as the terminals of signal input, IN 1 for the top gate and IN 2 for the bottom gate. When inputs of IN 1 and IN 2 are low voltages, the input signal of the device is defined as IN-00. When either input of IN 1 and IN 2 is a high voltage, the input signal of the device is defined as IN-10 or IN-01. When inputs of IN 1 and IN 2 are high voltages, the input signal of the device is defined as IN-11. The high output current of the MoS_2 logic transistor is defined as '1' state, while low output current is '0' state. The false-colored scanning electron microscope (SEM) image of the real device is shown in Fig. A2, which shows an accurate alignment of the two gates. A previous study[8] showed that MoS_2 exhibits high electron mobility[9] and a large band gap,[10] which indicates that MoS_2 has the potential to meet the requirements of logical application. The components of channel and dielectric are confirmed by Raman spectroscopy (Fig. 1(b)), which shows two characteristic peaks (A_{1g}, E_{2g}) of MoS_2[11] and one characteristic peak of h-BN.[12] When a series of identical input signals are applied to a logic transistor (IN-00, IN-01, IN-10, IN-11, voltage amplitude of 2 V), the channel current exhibits outputs of logic 'AND' at low temperature (10 K) and 'OR' at high temperature (250 K), revealing the temperature-switching characteristic of the MoS_2 logic transistor, as shown in Fig. 1(c). Due to the structure and working principle of the transistor, the directly measured output signal of the MoS_2 logic transistor is current. The circuit of the voltage-in current-out test system is plotted in Fig. A3. To transfer the current signal into a voltage signal, an additional resistor is introduced into the testing system and transforms the channel current into its partial voltage, as shown in Fig. A4. Figure A5 is the partial voltage of the resistor ($R = 220$ kΩ), showing a recognizable voltage-in voltage-out 'OR' logic gate function. Since the current output can be simply transferred into voltage, we take the current signal as evaluation criteria in the following part of this article.

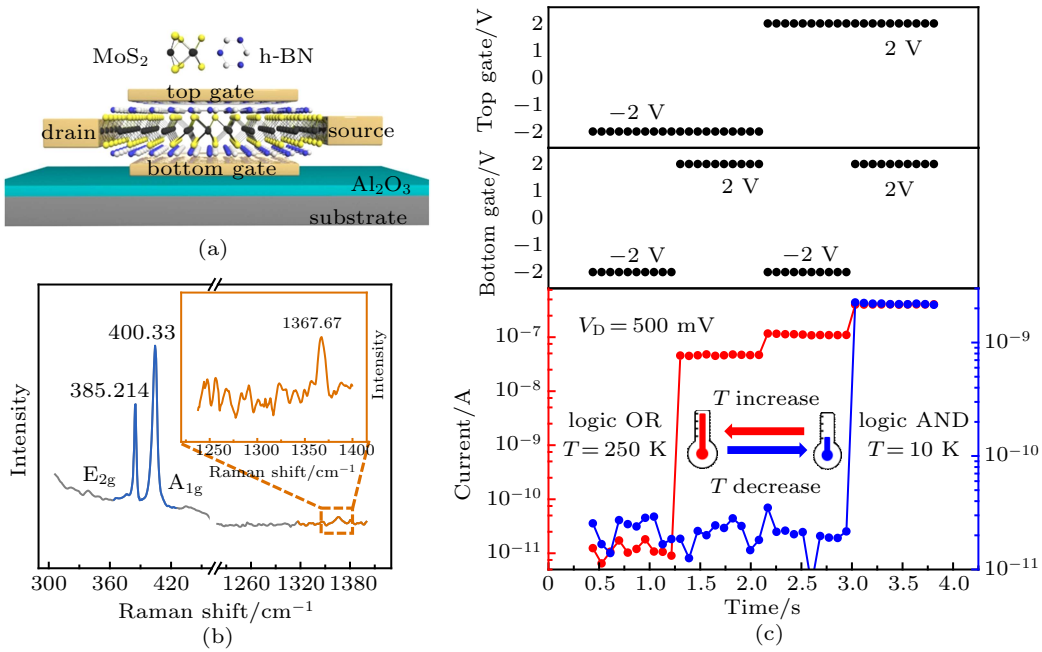


Fig. 1. Device structure and characterization of MoS_2 logic transistor. (a) Three-dimensional sectional view of MoS_2 logic transistor. MoS_2 serves as channel material; h-BN serves as dielectric material; top and bottom gates are used to input logic signal (voltage); drain and source are used to collect output signal (current). (b) Raman spectra of MoS_2 logic transistor, obtained by laser with 532 nm wavelength and 50 μW energy. The overlapped region shows characteristic peaks of the two materials (MoS_2 and h-BN). (c) Temperature switchable logic output of MoS_2 logic transistor. Continuous ±2 V is provided as input signal through top and bottom gates; channel current is collected as an output signal through drain and source; the drain voltage is 500 mV. The output characteristic of this device can be transformed into voltage by load resistance which is shown in Figs. A3–A5.

When the input voltages of the bottom gate (V_{BG}) and top gate (V_{TG}) are plotted as x- and y-axis, respectively, the output of current distribution density mapping can be divided into four regions, IN-00, IN-01, IN-10, and IN-11, obtained by drain voltage (V_D) of 500 mV. The mean value of the output channel current is selected as the output state and is used as the parameter to transform output state into a color squire, and four color-squires are composed together as one part to illus-

trate the logic function of the MoS_2 logic transistor at different temperatures. The basic color squires are blue ($R = 0$, $G = 0$, $B = 255$) and red ($R = 255$, $G = 0$, $B = 0$), representing the current values 1 pA and 1 μA. At 10 K, only the IN-11 region is in red, corresponding with logic 'AND', which means the channel can only be opened when both gates input high voltages. With the increase of temperature (at 150 K), the color of region IN-10 begins to turn red, which means the device is in a transition state of logical function. When the temperature rises to 250 K, the color of three regions (IN-01, IN-10, IN-11) turns to red, corresponding with logic 'OR', which means the channel can be opened by either gate (Fig. 2(a)). Extracting the average value of current in four stages at different temperatures, we plot Fig. 2(b). When the temperature increases, the output current of regions IN-00 and IN-11 is stable, whereas the output current of regions IN-10 and IN-01 changes, which leads to the transformation of logic output. This shows a dynamic change process of temperature-switching phenomenon.

Figure 2 indicates that the key element of logical transformation is the output transformation of regions IN-01 and IN-10. The transformation mechanism can be demonstrated by the Fermi–Dirac distribution function. Figure 3(a) shows that the occupy probability of electrons, symbolized as $f(E)$, increases with the increase of temperature. In $f(E) = 1/\{\exp[(E - E_F)/kT] + 1\}$, $f(E)$ is affected by two factors: one is $E - E_F$, standing for the band gap variation, the other is kT, standing for the extra carrier energy provided by temperature. With the increase of temperature, the increase of kT leads the increase of $f(E)$, which means the probability of electron occupation in E_c is higher. Besides kT directly affected by temperature, $E - E_F$ is also impacted by temperature. Previous studies showed that the band gap of MoS_2 decreases with the increase of temperature.[13,14] Figure 3(b) is the photoluminescence spectrum of the MoS_2 logic transistor at different temperatures, which shows a significant indirect band gap shift from 1.581 eV at 10 K to 1.535 eV at 250 K and direct band gap shift from 1.939 eV at 10 K to 1.862 eV at 250 K (Fig. 3(c)). Based on the band gap variation phenomenon, $E - E_F$ shows a decreasing tendency with the increase of temperature, which also leads to an increase of $f(E)$. So the two aspects have the same increase tendency for $f(E)$, which means higher temperature generates a higher probability of electron occupation in the bottom of conduction band E_c, corresponding to Fig. 3(a). Therefore, the temperature switchable phenomenon is caused by the band gap variation and carrier energy directly provided by temperature. Furthermore, figure A6 presents the dual-sweep transfer curves of the top and bottom interfaces, which shows negligible hysteresis of electrical characteristics caused by charge trapping. So, the influence of charge trapping/releasing effect on channel current can be ignored.

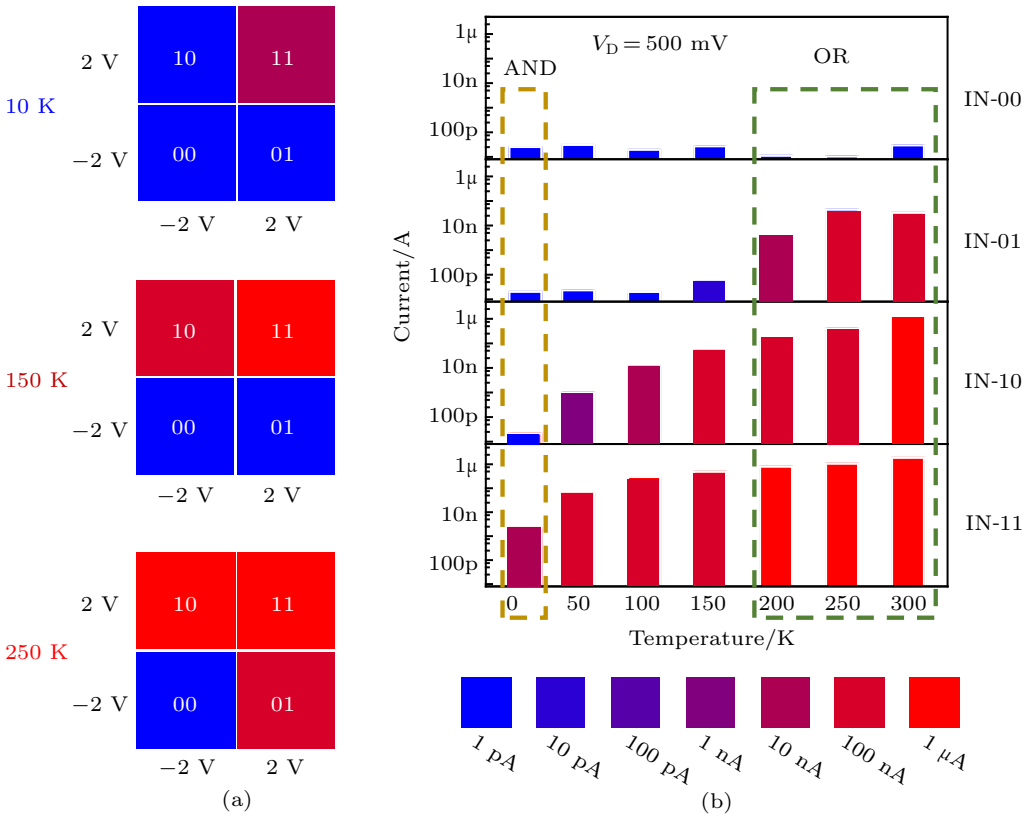


Fig. 2. Temperature dependence of MoS_2 logic transistor. (a) The current density distribution diagram at different temperatures. (b) The current distribution histogram of four states at different temperatures. The asymmetric performance of IN-01 and IN-10 is caused by different thickness of h-BN, which leads to the abnormal logic function (neither 'OR' nor 'AND') at 50 K, 100 K, and 150 K. Both (a) and (b) have the same input voltage (V_{TG}, $V_{BG} = \pm 2$ V), $V_D = 500$ mV, and color bar.

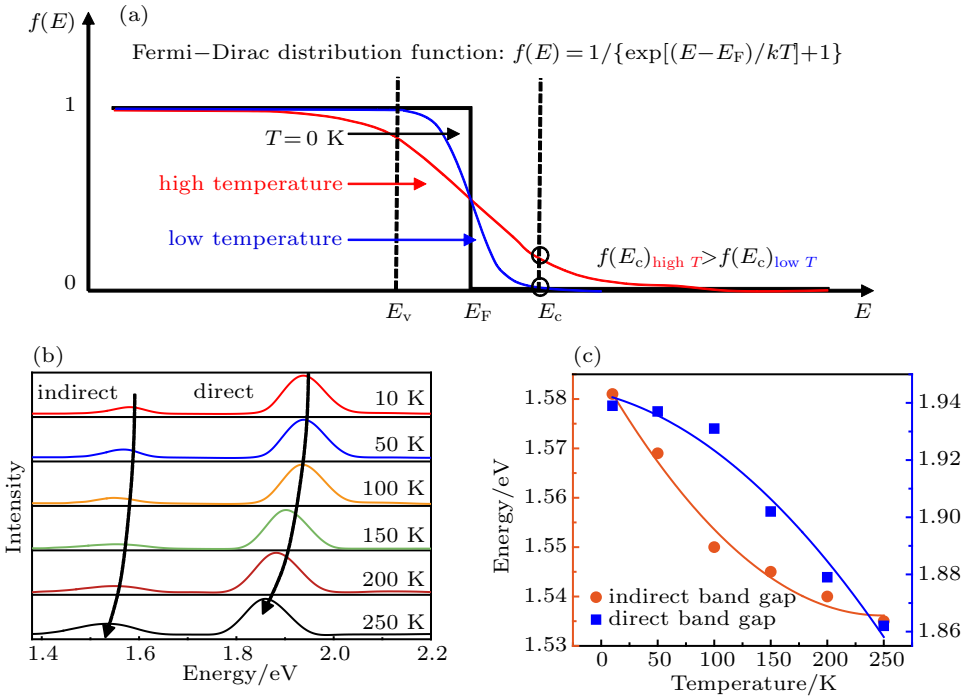


Fig. 3. The temperature dependence of Fermi–Dirac distribution function of MoS_2 logic transistor. (a) Schematic diagrams of temperature influence on the Fermi–Dirac distribution function. The schematic diagram shows the change process of Fermi–Dirac distribution function with temperature intuitively. (b) Photoluminescence spectrum of MoS_2 logic transistor at different temperatures (10–250 K). The excitation wavelength is 532 nm; power is 40 μW; integration time is 10 s. (c) The decrease tendency of direct and indirect band gaps of MoS_2 logic transistor with increasing temperature.

After analyzing the transition principle of logical output in a dual gate MoS_2 transistor, figure 4 further illustrates the temperature-dependent current characteristics with detailed experimental data. The channel current is calculated by theoretical equations under different drain voltage conditions. The following equations (1) and (2) apply to the linear region and saturated region, respectively:

$$I_{\mathrm{D}} = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W}{L}\left[2\left(V_{\mathrm{G}}-V_{\mathrm{T}}\right)V_{\mathrm{D}}-V_{\mathrm{D}}^{2}\right],\ 0<V_{\mathrm{D}}<V_{\mathrm{G}}-V_{\mathrm{T}}, \quad (1)$$

$$I_{\mathrm{D}} = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W}{L}\left(V_{\mathrm{G}}-V_{\mathrm{T}}\right)^{2},\quad V_{\mathrm{D}}>V_{\mathrm{G}}-V_{\mathrm{T}}, \quad (2)$$

where μ is the carrier mobility, C_{ox} is the gate capacitance, W is the channel width, L is the channel length, V_{G} is the gate–source voltage, and V_{T} is the threshold voltage of the transistor. In these equations, both V_{T} and μ are relevant to temperature, resulting in the temperature dependence of the channel current and logical output.

The transistor mobility is extracted from

$$g_{\mathrm{m}} = \mu C_{\mathrm{ox}}\frac{W}{L}V_{\mathrm{D}}, \quad (3)$$

where g_{m} is the transconductance, defined as $g_{\mathrm{m}} = \mathrm{d}I_{\mathrm{D}}/\mathrm{d}V_{\mathrm{G}}$ and extracted from Figs. 4(a) and 4(b); the gate capacitance $C_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/d_{\mathrm{ox}}$, $\varepsilon_{\mathrm{ox}} = 3.5416\times10^{-11}$ F/m is the dielectric constant of h-BN, and d_{ox} is the thickness of h-BN. Note that the maximum values of g_{m} were used to extract the channel mobility values.[15] Figure 4(c) shows the dependence of the threshold voltage on temperature, extracted from Figs. 4(a) and 4(b). The threshold voltage is obtained by the intercept generated by the tangent line of $I_{\mathrm{D}}V_{\mathrm{G}}$ and the x-axis. As the temperature increases, two surface channels controlled by the bottom gate and top gate show a visible negative shift, which means the increase of temperature reduces the energy required for electron transition. At the same time, the decrease of V_{T} shows a reduction of band gap, which is consistent with Fig. 3(b). Figure 4(c) also shows the temperature dependence of surface channel mobility extracted from transfer characteristic curves at various temperatures (Figs. 4(a) and 4(b)). As can be seen from the picture, the channel mobility of both the bottom gate and top gate is increased with temperature and the highest value is 15.8 $\mathrm{cm^2\cdot V^{-1}\cdot s^{-1}}$ at 300 K, which means the mobility is limited by scattering from charge impurities.[16] According to the physics of semiconductor devices, the higher the temperature is, the faster the carrier moves. Therefore, the carrier is less affected by the same attraction and repulsion, which means the effect of charge-impurities scattering is weaker at higher temperatures.[17] For μ and $-V_{\mathrm{T}}$ showing an increased relationship with temperature, the channel saturation current is positively correlated with temperature, which is consistent with Fig. 4(d) (the channel current extracted from Figs. 4(a) and 4(b) at 2 V).

With 2D materials, the logic function ('OR' and 'AND' gates) can be achieved in a single transistor. Compared with traditional transistor technology which needs at least two transistors to build a logic gate, this logic transistor architecture shows obvious area-efficiency strength. Furthermore, the tem-

perature switchable phenomenon opens up the potential for tailor-made 2D circuits, such as reconfigurable circuits. In reconfigurable circuits, one circuit design can achieve more than one function in different temperature configurations. Therefore, temperature-switchable behavior will be helpful in tailor-made reconfigurable circuits based on 2D materials in the future. In this work, a colorful logic map (Fig. 2(a)) is proposed, which is helpful in the construction of a reconfigurable circuit.

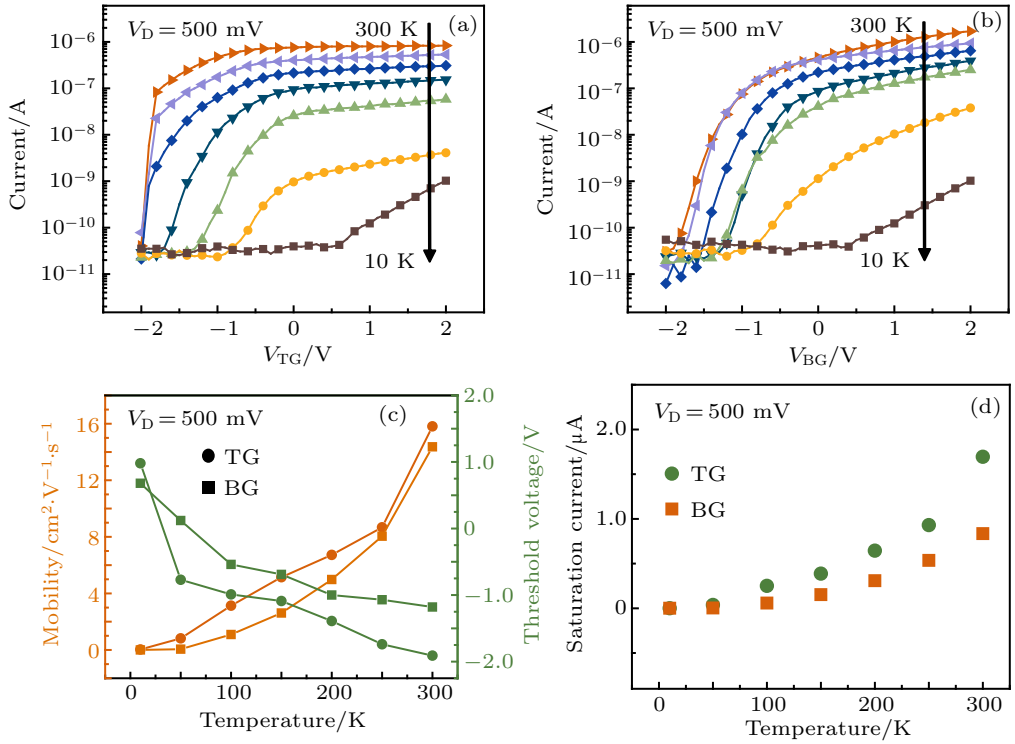


Fig. 4. Temperature dependence of mobility, threshold voltage, and saturation current. (a) and (b) The transfer characteristics of the top gate and bottom gate in MoS_2 logic transistor. Panels (a) and (b) use the same graphic symbol. (c) The extracted mobility and subthreshold voltage at various temperatures. (d) The saturation current extracted from (a) and (b) at 2 V under various temperatures.

4. Conclusion and perspectives

In this work, we study the temperature dependence of an MoS_2 logic transistor, finding that the logical output result changes from 'AND' to 'OR' with the increase of temperature. The transformation of output between 'AND' and 'OR' at different temperatures is caused by the energy band gap decreasing and extra energy provided by temperature. With the increase of temperature, both direct and indirect band gaps of MoS_2 show a remarkable decrease, which is confirmed both by the photoluminescence spectrum and threshold voltage shift. The temperature switchable phenomenon of MoS_2 logic transistors has application prospects for extreme environments.

Appendix A

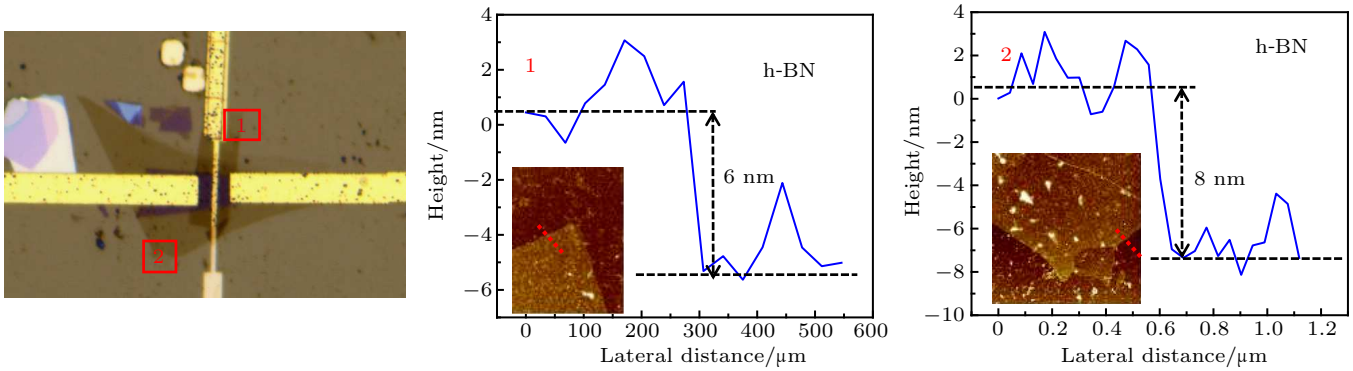


Fig. A1. The thickness of the top and bottom h-BN layers in the MoS_2 logic transistor confirmed by the atomic force microscope. The top h-BN is 6 nm and bottom h-BN is 8 nm.

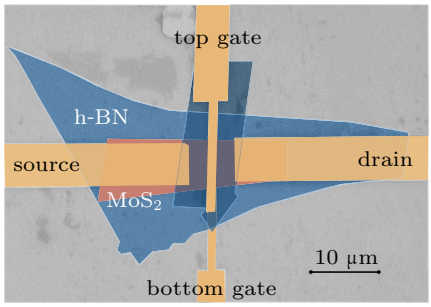


Fig. A2. The false-colored SEM image of MoS_2 logic transistor. The blue represents h-BN; red represents the MoS_2; yellow represents electrodes.

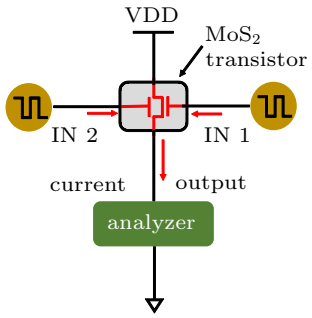


Fig. A3. The circuit of MoS_2 logic transistor that outputs the current signal. IN 1 and IN 2 separately represent the input signal from the top gate and bottom gate. The input voltage is generated by Keithley 4200 A semiconductor parameter analyzer. And output current is measured by the same instrument.

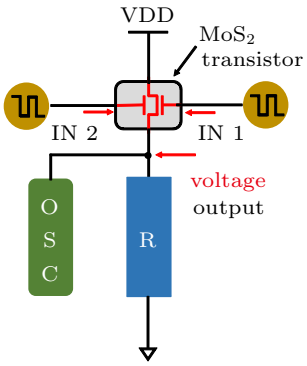


Fig. A4. The circuit of MoS_2 logic transistor that outputs voltage signal. To transfer output current into voltage, a resistor (220 kΩ) is induced into the circuit. An oscilloscope is used to measure the partial voltage of the resistor.

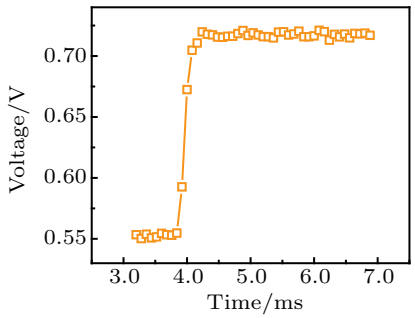


Fig. A5. Diagram of the voltage output of MoS_2 logic transistor. The resistance is 220 kΩ and the measuring instrument is oscilloscope (internal resistance = 1 MΩ). However, the oscilloscope internal resistance is not large enough for two-dimensional material devices, which makes the branch current of the oscilloscope very big. Therefore the voltage output of the device has a low on–off ratio after transformation.

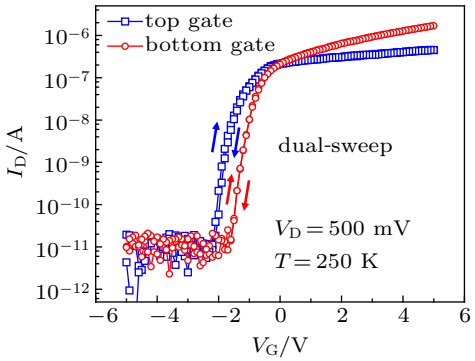


Fig. A6. The dual-sweep transfer curves of MoS_2 logic transistor. The zero hysteresis indicates that the interface charge trapping is negligible; $V_D = 500$ mV, $T = 250$ K.

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