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SPECIAL TOPIC — Physics in neuromorphic devices

A synaptic transistor with $NdNiO_3$*

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Recently, neuromorphic devices for artificial intelligence applications have attracted much attention. In this work, a three-terminal electrolyte-gated synaptic transistor based on $NdNiO_3$ epitaxial films, a typical correlated electron material, is presented. The voltage-controlled metal–insulator transition was achieved by inserting and extracting H^+ ions in the $NdNiO_3$ channel through electrolyte gating. The non-volatile conductance change reached 10^4 under a 2 V gate voltage. By manipulating the amount of inserted protons, the three-terminal $NdNiO_3$ artificial synapse imitated important synaptic functions, such as synaptic plasticity and spike-timing-dependent plasticity. These results show that the correlated material $NdNiO_3$ has great potential for applications in neuromorphic devices.

Keywords: synaptic transistor, electrolyte gating, artificial synapse, $NdNiO_3$, pulsed laser deposition

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1. Introduction

Modern computers are based on the von Neumann architecture, where the computing speed has a great advantage over that of the human brain.[1] However, the human brain is more powerful than any computer in fuzzy processing, pattern recognition, and other fields.[2] Because of the synapse connections of the brain's neural network, human brains can process information on a large scale in a parallelized and non-linear manner.[3] The understanding of the brain's learning and memory functions can be realized by studying the dynamic changes of the strength of the biological synaptic connection.[4] The research of brain-like devices and computers has always been a research hotspot,[5–10] and designing hardware with a behavior similar to the synapses in human brains is very important to realize brain-like computing. Using traditional CMOS technology, dozens of transistors are required to simulate synapses. This requires a large area on a chip and consumes a large amount of power, which hinders further development.[11]

Recently, emerging two-terminal devices such as resistive random access memory (ReRAM),[12,13] magneto-resistive random access memory (MRAM),[14,15] phase-change memory devices (PCM),[16,17] and ferroelectric tunnel junctions[18] have been demonstrated to emulate artificial synapses. A variety of tunable non-volatile resistance states in these devices are required to store the synaptic weight for emulating the synaptic plasticity. Three-terminal devices such as electrolyte-gated transistors[19] and ferroelectric field effect transistor (FeFET)[20] have also been proposed. Compared to two-terminal devices, three-terminal devices utilize an additional gate terminal to decouple the write/read operations. Three-terminal devices seem to realize the functions of biological neural devices with lower energy consumption and higher linearity.

For electrolyte-gated transistors, the gate electrode can be regarded as the pre-synaptic neuron, the channel between source and drain can be regarded as the post-synaptic neuron, and the conductance of the channel is equivalent to the weight of the synapse. When a gate voltage is applied, a huge electric field is generated at the interface through the formation of a double electric layer inside an ionic liquid,[21] which leads to the extraction and insertion of functional ions. This in turn leads to a change of the channel conductance, which simulates synaptic plasticity. IGZO,[22,23,27] $SrFeO_{2.5}$,[24] $SrCoO_{2.5}$,[25] VO_2,[26] WO_3,[19] etc. have been utilized to realize the operation of the synaptic transistor through electrolyte gating.

The rare-earth nickelate $NdNiO_3$ is a metal at room temperature, and exhibits metal–insulator transition at about 110 K.[28,29] The Hall result of the metal phase of $NdNiO_3$ is consistent with p-type carriers.[30] There is a hysteresis loop in the temperature-dependent resistance curve when cooling and heating, and its metal–insulator transition can

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be modulated through electrolyte gating.[30] Recently, several works have reported the conductance change of $NdNiO_3$ film through inserting protons, implying its potential application in synaptic transistors.[31,32] The recent work presented the direct evidence of the existence of $HNdNiO_3$ under positive electrolyte gating through SIMS measurements.[31] In the present work, we report on an artificial synapse based on $NdNiO_3$ films. By employing the ionic liquid N, Ndiethyl-N-(2-methoxye-thyl)-N-methylammoniumbis-(trifluoromethyl-sulphonyl)-imide (DEME-TFSI) as the gating medium, a three-terminal synaptic device with $NdNiO_3$ is implemented, and several important synaptic functions are realized. Our results indicate that these related materials have potential applications in brain-like devices.

2. Experimental detail

$NdNiO_3$ thin films were fabricated on a $\langle 001 \rangle$-orientated $LaAlO_3$ substrate using pulsed laser deposition. The deposition temperature was 650 °C, and the deposition oxygen pressure was 25 Pa. $NdNiO_3$ thin films with four different thicknesses 7 u.c., 11 u.c., 13 u.c., and 16 u.c. were deposited. The transport property was measured using a Physical Property Measurement System (PPMS). Then, we fabricated an electrolyte gated transistor via the standard micro-fabrication process. We utilized the ionic liquid DEME-TFSI due to its strong regulation ability. All electrical measurements were performed in a probe station connected with a Keithley 4200-SCS semiconductor parameter analyzer.

3. Results and discussion

The atomic structure schematic of $NdNiO_3/LaAlO_3$ is shown in Fig. 1(a). The measured R–T curves of the $NdNiO_3$ thin films at the four different thicknesses are shown in Fig. 1(b). As the film thickness increases, the hysteresis loop becomes more obvious, and the phase transition point gradually decreases. The larger the switch ratio, the wider the loop, and the more suitable the film is for this device. Because the R–T curve of the $NdNiO_3$ film of 16 u.c. has the most typical metal–insulator phase transition characteristics, and has the largest high and low temperature switch ratio, it is expected to obtain the best switch ratio in the regulation of ionic liquid. Thus, we chose the 16 u.c. thick film to fabricate the transistor. The device schematic is shown in Fig. 1(c). The channel size was 210 μm × 50 μm. The ionic liquid was dropped between the side gate electrode and the channel.

Figure 1(d) shows the transfer curve of the device. The sweeping rate was 2.5 mV/s, and the voltage between source and drain V_D was 0.4 V. The transfer curve shows a clear loop. The gate leakage current I_G is about 2–6 orders of magnitude smaller than the source–drain current I_D, indicating a negligible effect on the device performance. The transfer curve shows a clockwise hysteresis loop. The channel can be reversibly switched between the low and high conductance states through electrolyte gating. The channel conductance decreases as $V_G > 0$, while the channel conductance increases when $V_G < 0$. The transfer curve is consistent with the occurrence of the phase transition of $NdNiO_3$ films. When we apply a positive V_G, the hydrogen ions are injected into the channel film and the conductive $NdNiO_3$ becomes insulating $HNdNiO_3$.[31] Under negative gate bias, $TFSI^-$ ions accumulate near the interface between the channel and electrolyte. Thus, the induced EDL could pull protons out of the channel. Then, the $HNdNiO_3$ phase is transformed to the pristine $NdNiO_3$ phase.

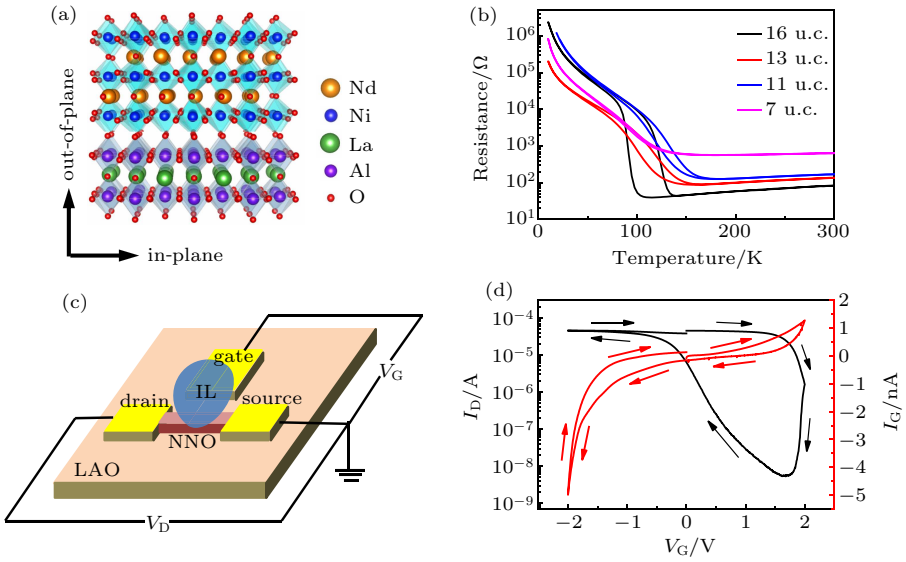


Fig. 1. The structure and property of electrolyte gated $NdNiO_3$ transistor. (a) The crystal structure of $NdNiO_3$ film grown on $LaAlO_3$ substrate. (b) The R–T measurements for different thickness $NdNiO_3$ films on $LaAlO_3$ substrates. (c) Schematic diagram of the electrolyte-gated transistor. (d) The transfer curve. The source–drain current I_D and the gate current I_G are shown as a function of the gate voltage. Arrows indicate the gate bias sweeping direction.

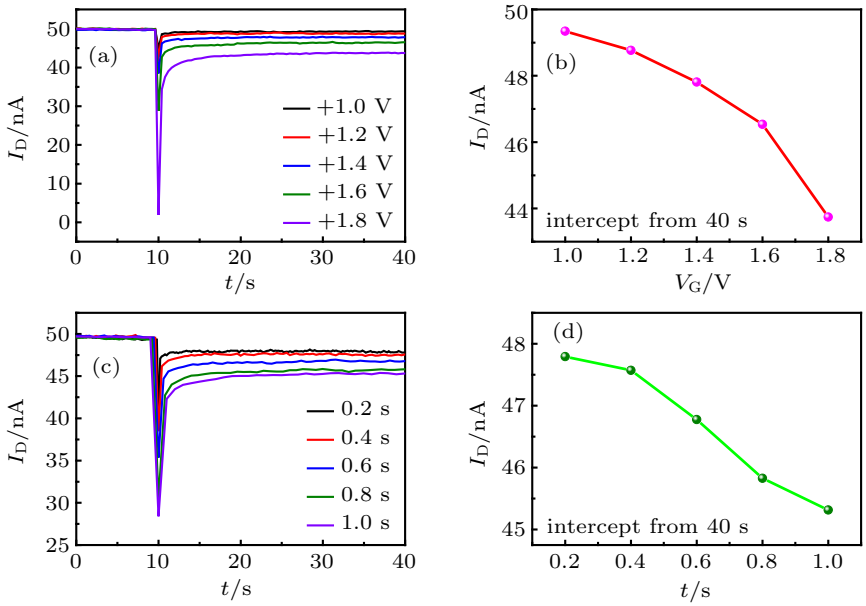


Fig. 2. The dependence of the channel current on the gate spikes. (a) The same spike time (0.4 s) with different spike voltages. (b) The source–drain current I_D of (a) intercepted from 40 s is shown as a function of gate voltage. (c) The same spike voltage (+1.4 V) with different spike time. (d) The source–drain current I_D of (c) intercepted from 40 s is shown as a function of spike time. Here, the V_D was 5 mV.

The formation of long-term memory in the human brain is based on the long-term associations between neurons. In order to simulate synaptic behavior, the devices must have the ability to emulate essential synaptic functions. The long-term test results of the device are shown in Fig. 2, with a source–drain voltage V_D of 5 mV. Figure 2(a) shows the results of different gate bias voltages with a constant pulse time of 0.4 s. It can be seen that the larger the gate voltage is, the more the current drops. Figure 2(b) shows the channel current I_D of Fig. 2(a) intercepted at 40 s. Figure 2(c) shows the result of different durations with the same pulse voltage 1.4 V. The longer the pulse time is, the more the current in the channel will decrease. Figure 2(d) shows the channel current I_D of Fig. 2(c) at 40 s. The device maintains a lower channel current under pulses of higher gate voltage, which shows that it has good long-term characteristics. Nowadays, artificial intelligence algorithms utilizing synaptic devices generally require the latter to have multi-level states. To demonstrate the multi-level states required for synaptic functions, the proposed electrolyte-gated $NdNiO_3$ transistor was operated by sending a series of voltage trains to the gate electrode. The result is shown in Fig. 3(a), where the positive gate voltage was 1.8 V, and the negative gate voltage was −1.6 V. For both positive and negative biasings, the pulse time was 200 ms and the interval was 50 ms. Here, the channel conduction was measured with $V_D = 5$ mV. The voltage trains consisted of "write" operations, where a series of pulses was sent to the gate. During the voltage trains, "read" operations were always performed. When we applied 5 pulses of 1.8 V, the conductance of the $NdNiO_3$ channel decreased from about 10 μS to 9 μS. Then, we applied 10, 15, and 20 spikes, causing a step reduction of the channel conductance to 7 μS. In each positive write operation, the channel conductance decreases due to the insertion of hydrogen ions into the $NdNiO_3$ channel causing a phase transition from conducting $NdNiO_3$ to insulating $HNdNiO_3$. More pulses cause larger channel modulation. Thus, we applied 20 pulses of −1.6 V, and the conductance of the $NdNiO_3$ channel increased from about 7 μS to about 8 μS. The channel conductance remained constant when $V_G = 0$, indicating that there is no chemical reaction at zero bias. Thus, after 15, 10, and 5 negative pulses, the channel conductance increased gradually. The channel conductance remained constant after each negative write operation, implying intrinsic non-volatile behavior. This shows that the electrolyte-gated $NdNiO_3$ transistor with V_G-controlled multi-level conduction states is suitable for synaptic devices.

Synaptic plasticity, that is, the ability to change the excitability of synapses through stimulation, is also an important basic characteristic. Long-term plasticity is mainly the long-term learning capability and memory that exists in biological synapses, and consists of long-term potentiation (LTP) and long-term depression (LTD), which are respectively considered as the continuous increase and decrease of a synaptic weight. These properties can be realized by applying a series of continuous gate pulses to adjust the conductivity of the device. In biology, LTP is widely considered as the basis of learning and memory in biological systems. Figure 3(b) shows our device's relationship between LTP and the number of pulses, where the pulse amplitude and width were −1.4 V and 0.2 s, respectively. Under the negative gate voltage, the insulating $HNdNiO_3$ changes to a conductive $NdNiO_3$ phase. This behavior can emulate LTP in biological synapses effectively. In contrast, LTD is used to selectively weaken synaptic connections. An electrochemical reaction occurs when a pos-

itive synaptic spike is applied to the gate. In order to prove that the device has characteristics similar to biological nervous systems, we applied 50 continuous pulses to the synaptic transistor, with a voltage of +1.2 V, a pulse width of 0.2 s. and an interval of 0.6 s (Fig. 3(b)). The gate tends to inject hydrogen ions into the $NdNiO_3$ channel, leading to a transition from metallic $NdNiO_3$ to insulating $HNdNiO_3$. As a result, the continuous gate spike reduces the excitatory postsynaptic current (EPSC). The increase and decrease of synaptic weight can be continuously simulated through applying continuous negative and positive spikes with good reproducibility and non-volatility.

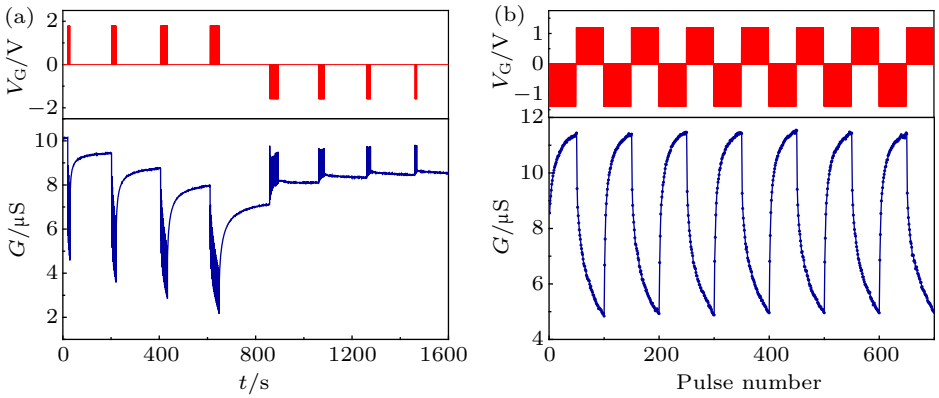


Fig. 3. The conductance modulation of $NdNiO_3$ transistor. (a) The channel conductance changes with pulse groups. Firstly, the positive gate voltage +1.8 V with pulse width 200 ms was applied, and the pulse number is 5, 10, 15, 20, respectively. Then, the negative gate voltage −1.6 V sequence was applied, and the pulse number is 20, 15, 10, 5, respectively. All the pulse groups were spaced about 180 s. (b) Repeatability of long-term synaptic potentiation and depression.

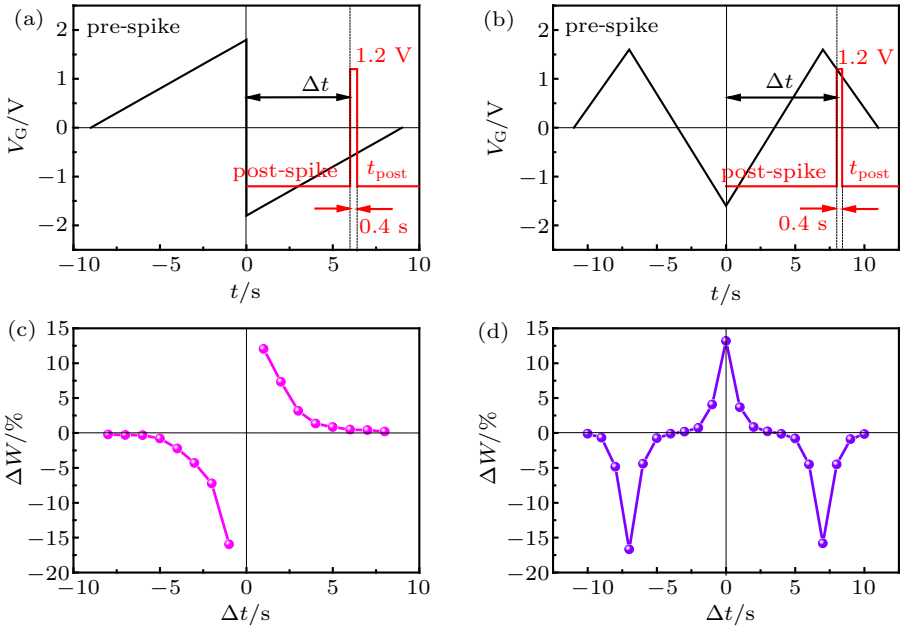


Fig. 4. STDP characteristics of $NdNiO_3$ transistor device. The applied pre- and post-spikes for the (a) asymmetric and (b) symmetric STDP functions. (c) Asymmetric and (d) symmetric STDP implemented in the $NdNiO_3$ electrolyte-gated synaptic transistors.

Among the Hebbian learning rules in simulating synaptic function, spike-timing-dependent plasticity (STDP) is considered as an important rule.[33] The regulation of synaptic weight is largely dependent on the difference Δt between the pre- and post-synaptic neurons, which helps to control the weight of the synapses accurately. By controlling the channel conductance in electrolyte-gated $NdNiO_3$ synaptic transistors, we have successfully realized the STDP function. To simulate this function, the output multiplexer was connected to the gate of the transistor to convert the voltage spike before and after the neuron. Figure 4(a) shows the test configuration of the circuit. The percentage change in the channel conductance in an $NdNiO_3$ transistor with a series of Δt from −8 s to 8 s suggests a typical asymmetric STDP function. For asymmetric STDP, LTP will occur if the pre-neuron spike arrives before the post-neuron spike ($\Delta t > 0$); conversely, LTD will occur if the pre-neuron spike arrives after the post-neuron spike ($\Delta t < 0$). The obtained asymmetric STDP curve can be approximated using an exponential decay function, which fully simulates the behavior of biological synaptic systems. Our experimental results show that the $NdNiO_3$ channel can indeed emulate such a behavior (Fig. 4(c)). Similarly, the STDP function can also

be achieved by selecting an appropriate source spike shape (Fig. 4(b)), which is called symmetric STDP, and the corresponding test results are shown in Fig. 4(d). For symmetric STDP, the change of the channel conductance only depends on the absolute value of Δt.

4. Conclusions

In summary, we utilized an $NdNiO_3$ thin film to simulate the function of biological synapse through electrolyte gating. Switching between memory states was achieved through the switching between the metallic state of $NdNiO_3$ and the insulating state of $HNdNiO_3$. The transfer curve demonstrated a change of approximately three orders of magnitude. The STDP experiment also demonstrated a performance completely consistent with that of biological synapses. The gating controlled phase transformation in nickelates is very stable, which could be helpful for designing artificial synapses for neuromorphic computing.

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