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Electrostatic gating of solid-ion-conductor on InSe flakes and InSe/h-BN heterostructures*

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We report the electrical transport properties of InSe flakes electrostatically gated by a solid ion conductor. The large tuning capability of the solid ion conductor as gating dielectric is confirmed by the saturation gate voltage as low as ∼1 V and steep subthreshold swing (83 mV/dec). The p-type conduction behavior of InSe is obtained when negative gate voltages are biased. Chemical doping of the solid ion conductor is suppressed by inserting a buffer layer of hexagonal boron nitride (h-BN) between InSe and the solid-ion-conductor substrate. By comparing the performance of devices with and without h-BN, the capacitance of solid ion conductors is extracted to be the same as that of ∼2 nm h-BN, and the mobility of InSe on solid ion conductors is comparable to that on the SiO_2 substrate. Our results show that solid ion conductors provide a facile and powerful method for electrostatic doping.

Keywords: solid ion conductors, electrostatic gating, InSe, van der Waals heterostructure

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1. Introduction

Principles of field-effect transistors (FETs) are the core of modern logic and memory devices, in which electrostatic doping provides unprecedented opportunities to modify electronic properties of materials through controllable and reversible tuning of carrier densities.[1–5] The range of carrier densities tuned in conventional structures of metal-insulator-semiconductor FETs is limited by the small capacitance of the insulating oxides with a maximum of $\sim 10^{13}$ cm^{-2} in compromise with the breakdown voltage.[6,7] The adoption of electric double layers (EDL), which construct Helmholtz's interface between electrodes and ionic electrolytes in electrochemistry, has greatly increased the tuning capability of carrier density.[2,8] Ionic electrolytes together with two-dimensional materials[9–12] constructing an EDL provide an important method for controlling various physically ordered states.[7,13–15] The prominent example is the gate-induced superconductivity in various two-dimensional (2D) materials, such as MoS_2,[16,17] $TiSe_2$[13] and TaS_2.[7] Some physical orders are intrinsically related with carrier density, such as superconductivity,[14,18] charge density wave,[7,13] and itinerant ferromagnetism.[15] Ionic electrolytes in the form of liquid or gel usually suffer from issues of chemical reaction and serious mechanical mismatch between inorganic and organic materials due to their distinct thermal expansion coefficients.[2,19] Resembling the principles of lithium-ion battery, Li^+ ions in the solid ion conductor (SIC) are able to move reversibly within a solid framework without introducing severe damage to host materials.[20] The effectiveness of an SIC ($Li_{1+x+y}Al_x(Ti_{2y}Ge_y)P_{3-z}Si_zO_{12}$) on tuning the carrier density has been recently demonstrated in FeSe by revealing the optimal doping for superconductivity.[21,22] Superconductivity has been also induced on $SnSe_2$ by using the SIC gate ($Li_2Al_2SiP_2TiO_{13}$),[23] similar to that using the ionic-liquid gate.[24] Yet the gating on WSe_2 has only been effective for hole doping.[25]

In recent years, indium selenide (InSe) has attracted tremendous research interest due to its high mobility and optical properties, fully competitive with atomically thin dichalcogenides and black phosphorus.[26,27] It has shown excellent electrical performance in FETs and logic inverters,[28] and electrostatically defined quantum point contact and quantum dots.[29] However, with the conventional gating dielectrics, the ambipolar behavior and transport behavior of InSe at extreme doping remain elusive. The SIC gating method is promising for InSe device applications, where the chemical doping and better interface quality need to be specially and carefully ad-

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dressed.

In this work, we demonstrate the tuning effect of a lithium solid ion conductor (Li-SIC) on γ-type InSe FETs. Moreover, we adopt the InSe/h-BN heterostructure to improve the interface quality. The large improvement on the capability of electrostatic doping is clarified in the low saturation gate voltage ($\sim$1 V) and steep subthreshold swing (SS) (83 mV/dec). We use h-BN worked as the buffer layer against chemical doping and its lifetime is improved. Li-SIC is complementary to the existing ionic liquid/gel to provide better stability.

2. Device fabrication and measurement

The Li-SIC ($Li_2Al_2SiP_2TiO_{13}$) used in our experiments was all purchased from Hefei MTI Corp. and produced by Ohara Inc., with the thickness of 150 μm. Both surfaces were polished. A conducting metal film was deposited on the back surface of Li-SIC specifically Ti/Au (5 nm/ 50 nm) to realize uniform gate voltage distribution.

The h-BN and InSe flakes were firstly mechanically exfoliated by cleaving a bulk single crystal (HQ graphene) on polydimethylsiloxane (PDMS), and then transferred to prepatterned Li-SIC. The InSe/h-BN heterostructure was fabricated by a dry-transfer process via sequentially stacking the InSe flakes onto the h-BN flake on the prepatterned Li-SIC. The entire process described above was carried out in a glove box filled with pure argon to avoid undesirable contaminations or material reactions. The h-BN flake thickness is specifically chosen to be $\sim$10 nm and the InSe flake to be $\sim$15 nm. The highly uniform and clean interfaces were demonstrated in our previous work.[28]

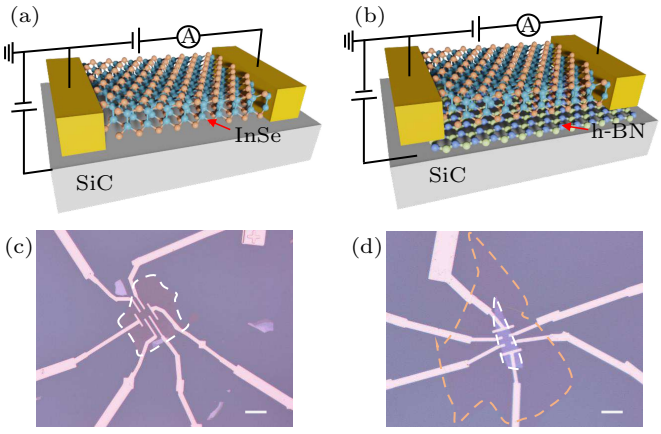


Fig. 1. Schematic and optical images of the Li-SIC devices. (a) and (b) Schematic of the Li-SIC gated InSe field-effect transistor (a) and InSe/h-BN heterostructured transistor (b) with Ti/Au as the contact electrodes and the measurement setup. (c) and (d) Optical microscope images of a typical device on an InSe thin flake (c) and on an InSe/h-BN heterostructure (d), respectively. The white and yellow dashed lines indicate the outline of the InSe flake and the h-BN flake, respectively. The scale bar is 10 μm in (c) and (d).

The device structure is similar to that of the conventional metal-oxide-semiconductor FETs, as schematically shown in Figs. 1(a) and 1(b), respectively. InSe FETs in the Hall bar geometry are fabricated with the standard electron beam lithography technique, followed by electron beam evaporation of Ti/Au (5/50 nm) metal stacks as contact electrodes. The optical images of the devices are shown in Figs. 1(c) and 1(d). The measurement of electrical transport property is performed in the physical property measurement system (PPMS, Quantum Design Inc.) with the Keysight B2902A as source/measure unit. The measurement precision of current is in the pico-Ampere range in our setup. To reduce possible electrochemical reactions between Li-SIC and InSe, all measurements are performed at 260 K.[21] The scanning speed of gate voltage is kept at 3 mV/s.

3. Device characterization of InSe on Li-SIC

The characterizations of Li-SIC gated InSe FETs are started with measuring the transfer curve under positive gate voltage (V_g). Transfer curves in Fig. 2(a) are measured in the two-probe geometry for different drain-source voltages V_{ds} (0.1, 0.3 V), which shows similar behaviors. As shown in Fig. 2(a), when the gate voltage reaches $\sim$0.2 V, the drain-source current is $\sim 10^{-12}$ A, and then the drain-source current I_{ds} in logarithmic scale increases linearly with V_{ds}. Therefore, the threshold voltage for electron conduction can be determined to be $\sim$0.2 V. The current becomes saturated when V_g is over $\sim$1.0 V, while in the case of 300-nm-thick SiO_2 normally it takes above $\sim$40 V for the current to get saturated,[30,31] indicating that the tuning efficiency of the Li-SIC gate is $\sim$40 times larger than that of 300-nm-thick SiO_2. The saturation current reaches $\sim$1 μA and the current ON/OFF ratio (ON/OFF ratio $= I_{ON}(\max.)/I_{OFF}$) is $\sim 10^5$. The SS value is 83 mV/dec, which is extracted from the logarithmic plot of I_{ds} as a function of V_g in Fig. 2(a), similar to the values found for ionic-liquid gated devices.[8] It is much lower than that of InSe FETs using conventional dielectrics and very close to the theoretic limit of 52 mV/dec at 260 K.

The devices show excellent reproducibility and stability with V_g below 2 V. With further increasing V_g in the saturation regime, the I_{ds} grows slowly. The intercalation of Li-ion could be seen from the apparent increase in leakage current with V_g over $\sim$1.0 V in Fig. 3(d). In the case of ionic liquid gating, the doped charge accumulation layers occupy only a few topmost layers due to electric field screening.[6,7] While for Li-SIC, the doping effect shows uniform distribution over the whole sample because the metal electrodes and dielectric are attached to opposite surfaces of the channel material.

Even though InSe has attracted intensive studies, the ambipolar transport behavior remains a challenge, the p-type behavior of which has only been revealed with band engineering.[32] It is unexpected that a Ti/Au contact could realize the p-type behavior, considering the rather high Schottky

barrier. The Li-SIC has shown very strong electric doping behavior, which could effectively reduce Schottky barrier height at high doping density.

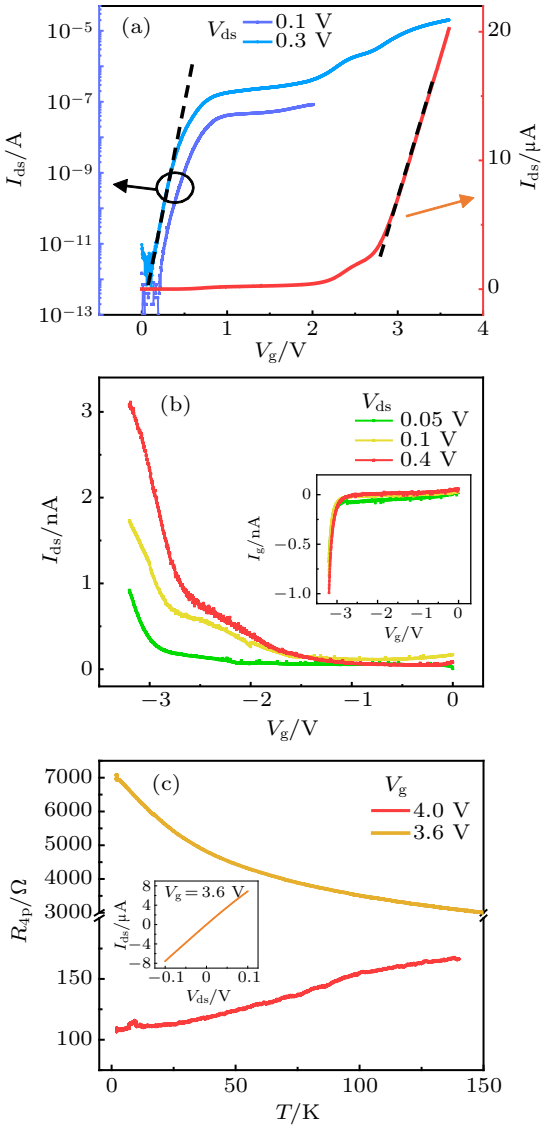


Fig. 2. Device performance of Li-SIC gated InSe thin flakes. (a) Transfer curves (I_{ds} vs. V_G) of the device in Fig. 1(c), measured at 260 K for $V_{ds} = 0.1$ V (dark blue line) in logarithmic scales and 0.3 V in logarithmic (light blue line) and linear (red line) scales. The two black dotted lines are linearly fitted in the linear region of red line and in the subthreshold region of light blue line to extract μ_{FE} of 129 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and SS of 83 mV/dec, respectively. (b) Transfer curves of negative V_G for $V_{ds} = 0.05$, 0.1 and 0.4 V. Inset: the accompanying gate-dependent leakage current I_g. (c) The temperature-dependent resistance at $V_G = 3.6$ V and 4.0 V, which shows the semiconducting to metallic transition when further increasing V_G to 4.0 V. Inset: the linear output curve (I_{ds} vs. V_{ds}) for $V_G = 3.6$ V at 260 K.

As shown in Fig. 2(b), when sweeping the gate voltage at the negative bias side, i.e., hole doping, the channel current is much smaller compared to that of electron-doping and no current saturation is observed with the hole current limited in the range of a few nA. The current ON/OFF ratio is only $\sim 10^3$. During the Li-SIC gate sweeping process, the gate leakage current is carefully monitored. As shown in the inset of Fig. 2(b), the leakage current almost remains the same level for different values of V_{ds}, which is of the order of 1 nA or less, similar to the result in Ref. [25]. This all confirms that the hole current does not come from the gate leakage. The rise of leakage current over −3 V is possibly due to the enhancement of electrochemical reactions at higher voltages. To further improve the ambipolar transport in Li-SIC gated InSe FETs, contact engineering to optimize the hole conduction through balanced band alignment with that of electrons needs to be performed.

The temperature-dependent resistivity is obtained in the 4-probe configuration under constant current of 1 μA. Semiconductor-to-metal transition is observed when V_G increases from 3.6 V to 4.0 V, as shown in Fig. 2(c). The transition is due to the giant doping capability with charge filling from valance band to conduction band, similar to the insulator-to-metal transition in MoS_2 gated with ionic liquid.[16] Overall the gating effect of Li-SIC follows the principles of FETs and the capability of electrostatic doping is much stronger than conventional dielectrics.

4. Device characterization of InSe/h-BN heterostructure on Li-SIC

High surface roughness and trapped interface charges in the SiO_2/Si substrate have introduced additional carrier scattering to degrade the intrinsic electrical performance of the atomically thin 2D materials. The Li-SIC substrate bears these drawbacks as that in SiO_2/Si. It has been found that h-BN can form atomically flat interface between 2D materials and greatly reduce the charge trapping.[33] On the other hand, the chemical intercalation induced by ionic liquid is not desired. The effectiveness of h-BN to protect target materials from chemical reactions of ionic liquid has also been reported.[13,34] This conceptual success intrigues us to fabricate the h-BN/InSe heterostructures on Li-SIC for better electrical performance. Transfer curves shown in Fig. 3(a) are obtained at $V_{ds} = 0.3$ V. The drain-source current I_{ds} scales logarithmically with V_g in the subthreshold region. The current saturation is still not observed with V_g up to 3 V, larger than that in the InSe/SIC device. The device performance keeps almost the same even after one year, while for that without h-BN the performance would gradually be degraded in a few weeks (Figs. S1 and S2 in the Supporting Information). The current ON/OFF ratio is $\sim 10^5$. The saturation current is the same order of magnitude while the OFF current is one magnitude larger than that in Fig. 2(a).

Notably the SS value has increased to 204 mV/dec due to the reduction of total capacitance contributed from the series capacitance of Li-SiC and h-BN. From the theoretical model of conventional semiconductor FETs,[35]

$$\mathrm{SS} = \frac{k_B T}{q} \ln 10 \left(1 + \frac{C_D}{C_G}\right), \quad (1)$$

where C_D is the depletion capacitance of the channel materials, C_G the capacitance of the gate, k_B the Boltzmann constant, and q the elementary charge. In the InSe/SIC devices, C_D is the depletion capacitance of InSe flakes, C_G is the capacitance of the SIC. While in the InSe/h-BN/SIC devices C_D remains the same, the change of SS comes from the change of C_G, which becomes the series capacitance of ~10 nm h-BN and SIC. With these relations, the capacitance of SIC is determined to be equal to that of ~2 nm h-BN (dielectric constant $\varepsilon = 4$),[36] which agrees with the model of the EDL in thickness of ~1 nm.[6] The field-effect mobility could be obtained from

$$\mu_{FE} = \frac{L}{W}\frac{1}{C_G}\frac{1}{V_{ds}}\frac{dI_{ds}}{dV_g}, \quad (2)$$

where L is the effective channel length, W the effective channel width, C_G the capacitance of the gate, V_{ds} the drain–source voltage, I_{ds} the drain-source current, and V_g the gate voltage. The calculated μ_{FE} is 129 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for the Li-SIC gated InSe FETs, with $L = 10.2$ μm, $W = 2.9$ μm and C_G of Li-SIC being 1.7 $\mu F/cm^2$, which is comparable to the largest value of 122 $cm^2 \cdot V^{-1} \cdot s^{-1}$ reported for the InSe FETs using 300-nm-thick SiO_2 as the dielectric substrate.[28,31] While in Li-SIC gated InSe/h-BN heterostructured FETs, μ_{FE} is 160 $cm^2 \cdot V^{-1} \cdot s^{-1}$, with L being 11.2 μm, W being 2.6 μm, and C_i being the series capacitance of 0.25 $\mu F/cm^2$. This is lower than that of InSe/h-BN heterostructure on the SiO_2 substrate,[28] which probably results from the large capacitance of Li-SIC compared to that of h-BN.

The output curves in Fig. 3(b) show almost linear relations between I_{ds} and V_{ds} in the saturation region, indicating that under gate modulation, the Schottky barrier between Ti contact and InSe is gradually reduced. With the increase of V_g, the conductivity of InSe grows better in Fig. 3(c), while it still remains a semiconducting behavior even when the V_g is as high as 5 V. The intercalation of Li^+ has been remarkably suppressed, which could be seen in the reduced leakage current below 1 nA in Fig. 3(d). It greatly enhances the device stability.

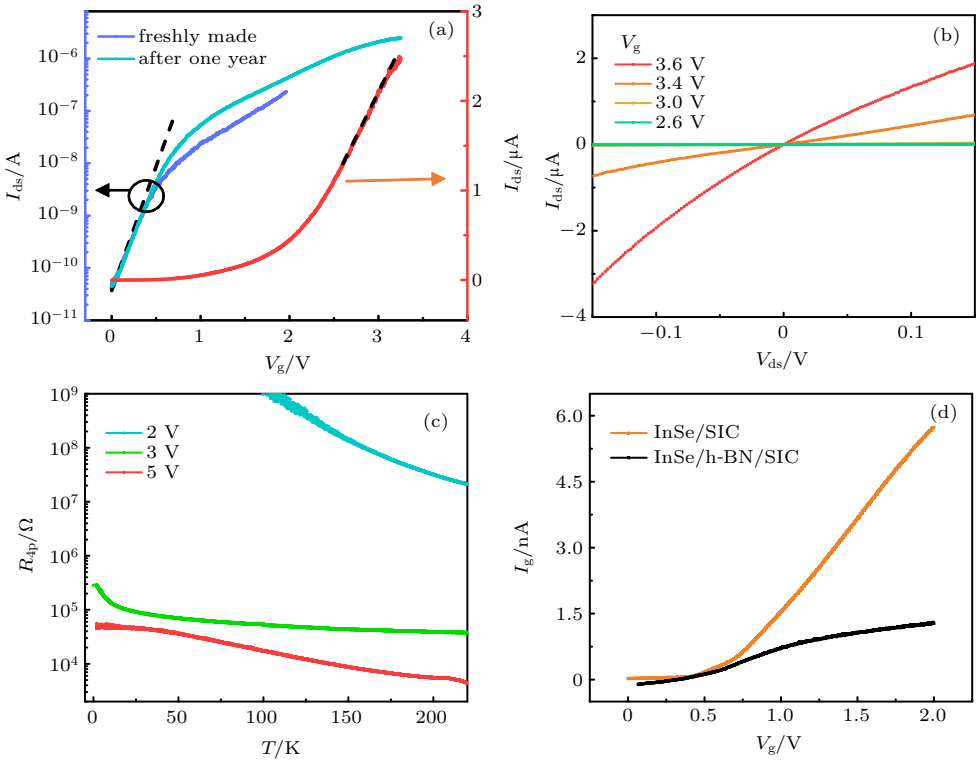


Fig. 3. Device performance of the Li-SIC gated InSe/h-BN heterostructure. (a) Transfer curves (I_{ds} vs. V_G) of the device in Fig. 1(d) on an InSe/h-BN heterostructure on Li-SIC, measured at 260 K for $V_{ds} = 0.3$ V in logarithmic (blue) and linear (red) scales. The device performance keeps stable after one year. The two black dotted lines are linearly fitted in the linear region of red line and in the subthreshold region of light blue line to extract μ_{FE} of 160 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and SS of 204 mV/dec, respectively. (b) Output curves (I_{ds} vs. V_{ds}) at different gate voltages. (c) The temperature dependent resistance at V_G of 2 V, 3 V and 5 V. It all shows semiconducting behavior. (d) Gate current for devices with/without h-BN in between InSe and Li-SIC when sweeping V_G from 0 to 2.0 V. The leakage current is suppressed with h-BN thin flakes.

Overall, to make full potential of the doping effects of Li-SIC while avoiding the deteriorating chemical reactions, the h-BN flakes make a perfect buffer layer in this sense. Careful trade-off should be considered between the relief of chemical reaction and the decrease of total series capacitance of the gate.

5. Summary

In summary, we have successfully demonstrated the electrostatic doping of SIC on InSe flakes and InSe/h-BN heterostructures, which shows competitive performance with that on SiO_2 substrates. The SIC has shown large doping ability

for both positive and negative gate voltages and comparable performance compared to ionic liquid/gel in electrostatic doping, while it provides superior advantages for tuning carrier density and physical properties at low temperatures. Moreover, the SIC provides an alternative method for improving electrostatics on the roadmap for semiconducting devices and systems. The large doping density could overcome critical issues at ease such as electric contacts and interface quality in the exploration of semiconducting materials and devices.

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